DAQ design consistency and plan

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- One of the purposes of this B2GM is to list up the possible conflicts/competitions in the design and to think about how to resolve them.

- We went through all the components in DAQ and discussed how to resolve the conflicts/competitions at last extended TRG/DAQ meeting.

- This report is the summary of the discussion at the meeting, but let's go through again to have more opinions from more people.

1. Frontend Readout

- Gary is trying to “unify” the FE+digitizers using BLAB and TARGET chips (full waveform sampling).

- Detector groups are seeking for their own design.
  Pixel-> not yet fixed
  SVD -> APV25
  CDC -> FPGA-TDC + slow ADC, comparison with TARGET
  PID -> custom ASIC, BLAB
  ECL -> BINP electronics
  KLM-> considering BLAB.

- Gary is continuing the effort to discuss with detector groups and some are considering to use the unified FE.

  -> Competition exists in some sense, but the decision of the FE is basically up to each detector group.

2. Unified data link

- Three approaches exist : Gary's, Liu-san's and Nakao-san's

- We had a meeting in IHEP in May to solve the conflict.
  Conclusion at the meeting:
  * At the stage of R&D, different hardware approaches can co-exist. The hardware is basically very similar consisting of Xilinx Virtex 5 + Rocket I/O with optical tranceiver.
  * The most important thing in the data link is to establish the the data transfer protocol.
    -> supposed to be IHEP's responsibility. They have rich experience in BES III trigger.
  * The hardware is supposed to be converged to IHEP's design also and we seek for the possibility of mass-production in China. (There might be some exceptions like iTOP case where their own design of data transfer link is considered. But it is forced to use the same transfer protocol.)

- We are now going along with this strategy. Final decision will be made in August meeting. -> No competitions/conflictions now

3. COPPER system

- Basically the system is already well defined and no competing design.

- Upgrade of CPU card on board is planned for the sustainability of COPPER system over 10 years.

- We will recycle COPPERs (COPPER-II) now in hand (~250). New production is ~250 in coming three years (COPPER-III).
  ** Consideration about how to maintain the damaged COPPER is necessary. At least, procedure to pin point the problematic component should be established*

- The data transfer link for COPPER-III to Readout PCs is upgraded to GbE. -> COPPER-III will be used for the readout where high-speed data transmission is necessary.

  -> Design is already concrete and no competions/conflictions

4. Timing Distribution

- Timing distribution from Trigger to COPPERs is already established and concrete.

- The design of timing distribution from COPPERs (or other detector-basis dedicated distributer) to FE is not yet fixed including the handshake scheme (hopefully deadtime-less scheme).

- Nakao-san is now doing R&D on this. He is the only person working on this system and there is no competition for now. (I remember Gary was proposing sophisticated system, but it could be too sophisticated.....)

- Comment from Liu-san(IHEP): needs some additional signal lines to manage the handshake. -> Nakao-san will think about it.

5. Event Builder

- Two designs exist.
  1) Barrel shifter switch implemented on PCs connected point-to-point by the network.
  2) Conventional network switch technique

- Higuchi-san and Yamagata-san are working on both to compare the performance using test benches.

- This FY is dedicated to the R&D for the comparison. We will have the final design by the end of this FY.

  -> Competition exists, but the same developers are trying both to choose final design.

6. HLT/Storage and data flow

- Hardware-wise, we will basically recycle the current design of RFARM.

- Modularized system. 1 unit is expected to process L=2.0x10^34. We will have ~5 units at the beginning and increase the number of units gradually to keep up with the luminosity increase.

- The data processing framework will be renovated:
  * New analysis framework “roobasf” is supposed to be the core.
  * Data flow based on ROOT I/O which enables OO data handling from the level of readout modules(COPPERs).
  * “roobasf” will be implemented both in COPPERs and HLT farms.
  * MPI based parallel processing over network is a part of roobasf development.

-> Confliction DO exists : choice of Belle II analysis framework
  - If ILC framework is chosen, it imposes quite tough works to “interface” and “parallelize” it for HLT usage, and to implement data flow in LC data model.....
    -> Who can really work for them??

7. Pixel integration

- Need a huge data reduction before feeding the data flow into storage.
- Two approaches:
  1) Level 2 data reduction using SVD Z readout (aka SVD L1.5 trigger)
  2) 2 step HLT. First HLT provides the precise track info obtained using SVD+CDC to Pixel readout, data reduction performed there by hit-track association, and the reduced data flow from Pixel is merged at the second level HLT.

-> just started to think about both approaches.
  * Pixel people will pursue approach 1)
  * DAQ people will think about 2).

-> 2) is considered to be more robust and could be the baseline. Relying only on 1) is quite risky considering our experience with SVD L1.5 trigger.....

8. System control (Slow control)

- Basically we are planning to continue using NSM for global control. No proposals on the competing design is raised up to now.

- Inside each subsystem, the control scheme can be different from NSM.
  ex. Event builder : use “80's technology” for the control
  HLT : MPI based control scheme equipped in “roobasf”

- But the “master” node of each subsystem is supposed to interface with NSM.

  -> No conflicts up to now.

II. Plan

- Our plan is basically unchanged from last meeting:

FY2009:	Prototype of data link (tx + rx) : hopefully by CDC beam test in autumn Prototype of timing distribution Final decision on the FFE unification (by the end of this FY) Development of new CPU card for COPPER Event builder prototype : choice of technology HLT framework + data flow software prototype (<- framework decision by autumn) Radiation test of components placed near detector E-hut: Planning of new layout + detector side layout, power/cooling estimation
FY2010:	Massive purchase of COPPER3+CPU (1) (~100) Finalize unified data-link. Delivery of FPGA core to subdetector group Finalize timing distribution scheme Test batch production of unified data receiver FINESSE (~10-20) Event builder full scale prototype HLT + data flow : partial system test (COPPER->EVB->HLT) E-hut: Clean-up, installation of new infrastructure (power, network, cooling, etc.) installation of new racks/crates (1)

FY2011: Massive purchase of COPPER3+CPU (2) (~100)
Mass production of unified receiver FINESSE (1)
Massive purchase of Event builder/HLT PCs (1) (~ 5 units)
Start global system test (readout->COPPER->EVB->HLT)
E-hut: Installation of new racks/crates (2)

FY2012: Massive purchase of COPPER3+CPU (3) (~50)
Mass production of unified receiver FINESSE (2)
Massive purchase of event builder/HLT PCs (2) (~ 5 units)
Global system test w/ trigger + Cosmic with available subdetectors

FY2013: Tuning in cosmic
- Summer : commissioning(?)

Milestones in the FY:

- We would like to have a working prototype of unified data link before CDC beam test so that it can be tested with CDC new readout electronics.
  -> But it is not a “must”. We can test it on test bench.
  -> We will have a meeting with IHEP tomorrow to discuss about the unified data link. We will discuss the schedule also.

- FE unification: have to be solved before starting TDR writing.

- HLT and framework .....

  * We planned to have a DAQ workshop sometime in May or June, but we couldn't because of various reasons.....(sorry...)
    -> Let's try to have it before next B2GM and discuss the detail of each component!