Data Reduction for the DEPFET Pixel Detector (PXD)

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Excellence Cluster
Universe

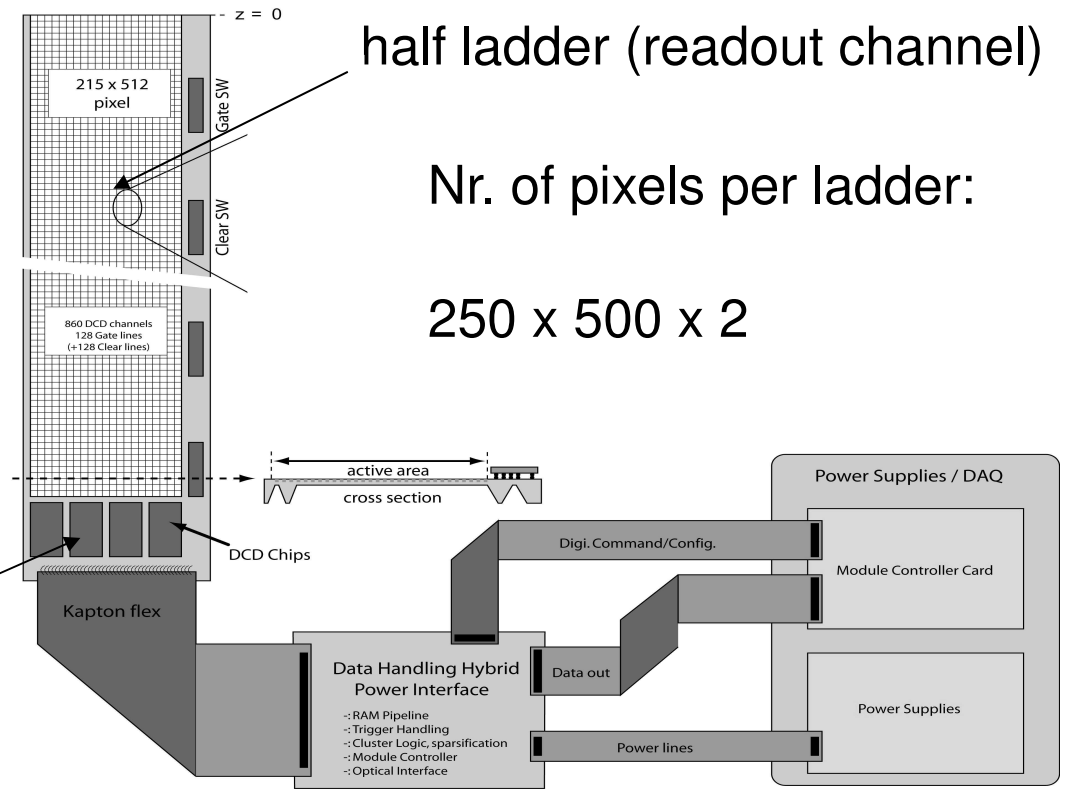
Overview

- DEPFET readout schematics
- Proposal for a Data Reduction algorithm
- First simulations
- Summary

Rate Estimates for the PXD

250

500
1000



half ladder (readout channel)

Nr. of pixels per ladder:

250 x 500 x 2

DHP:
zero-suppression
readout buffers (10 MByte)
slow control …

Digitzation (DCD)

DHH: module controller
data link

- 44 half ladders:
  5.5 Million pixels (px)
  For a 10µs readout
- 1-2% occupancy:
- 55 kpx on at any time
- about 10^5 px in each event
- Trigger rate: 10-30 KHz
- Total rate: 3×10^9 px/s
- 4 bytes per px (pos + ADC)

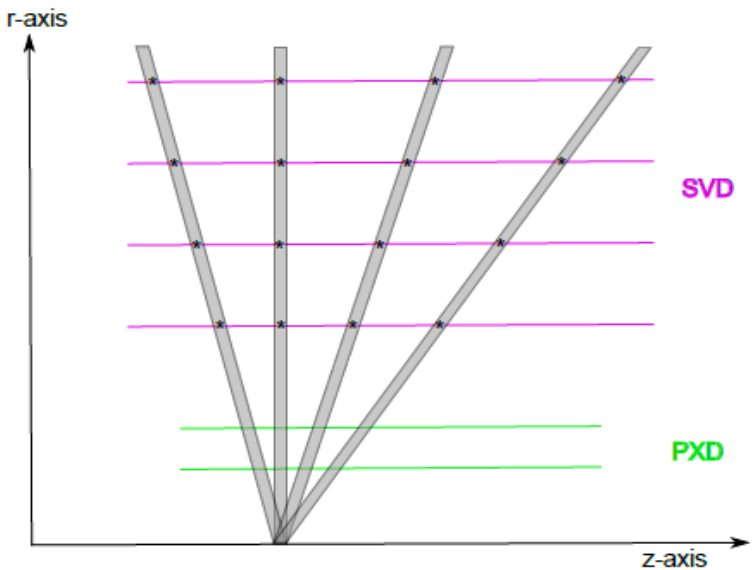
Total rate: 100 GBits/s

2.5 GBits/s
per R/O channel

PXD data volume must be reduced at least by a factor of 10

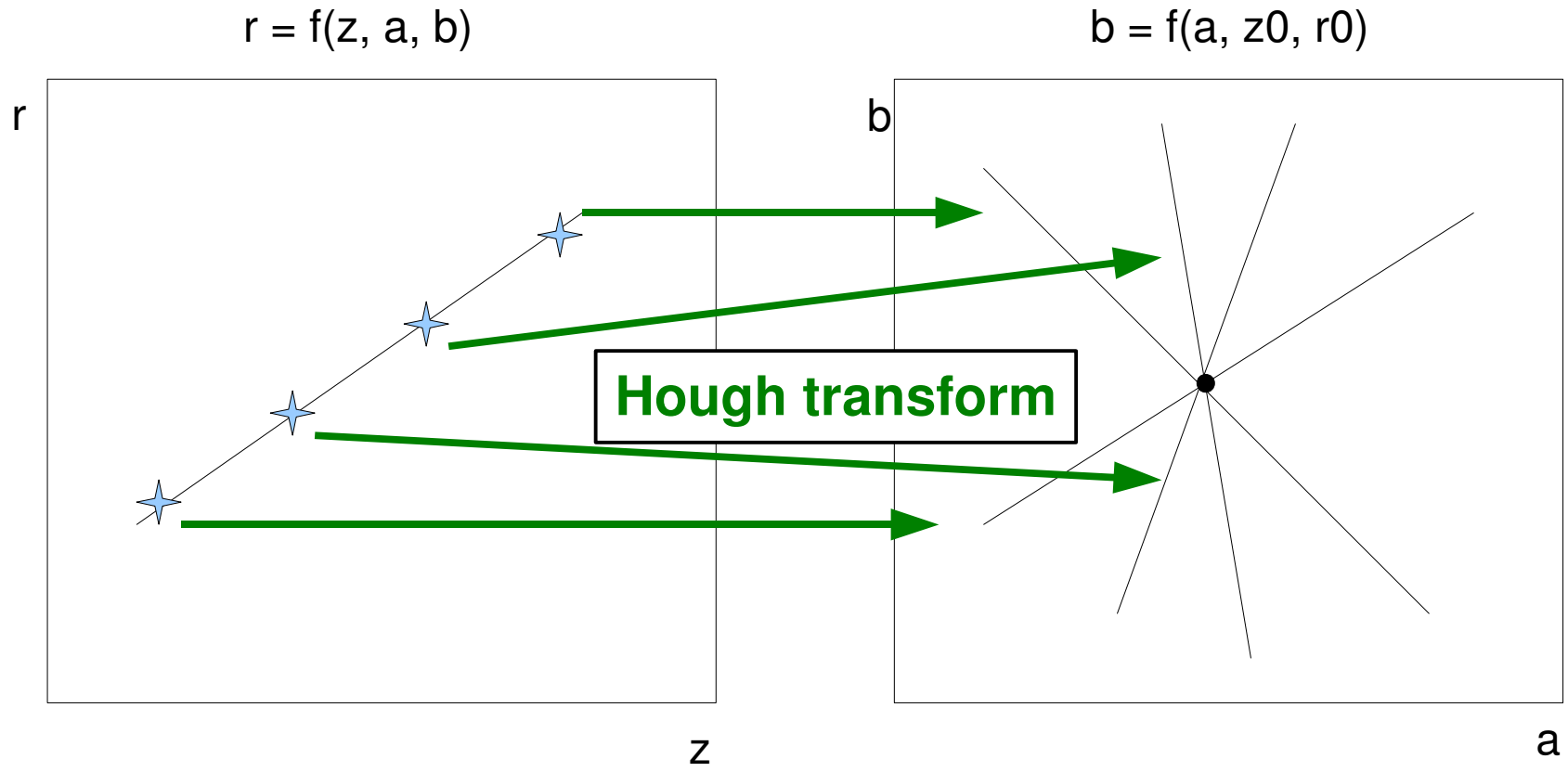
Data Reduction algorithm: 2D Tracking

- use SVD strip data (no CDC)
- z-r-projection of SVD hits
- fast 2D Tracking
- have a fast algorithm <u>before</u> the event builder
- Potentially a Z-vertex trigger
- build roads in z-r-space through PXD
- remove PXD data outside of the roads



Hough transform

Every point in r-z space is mapped to a straight line in parameter space



Tracking problem is transformed into a peak finding problem

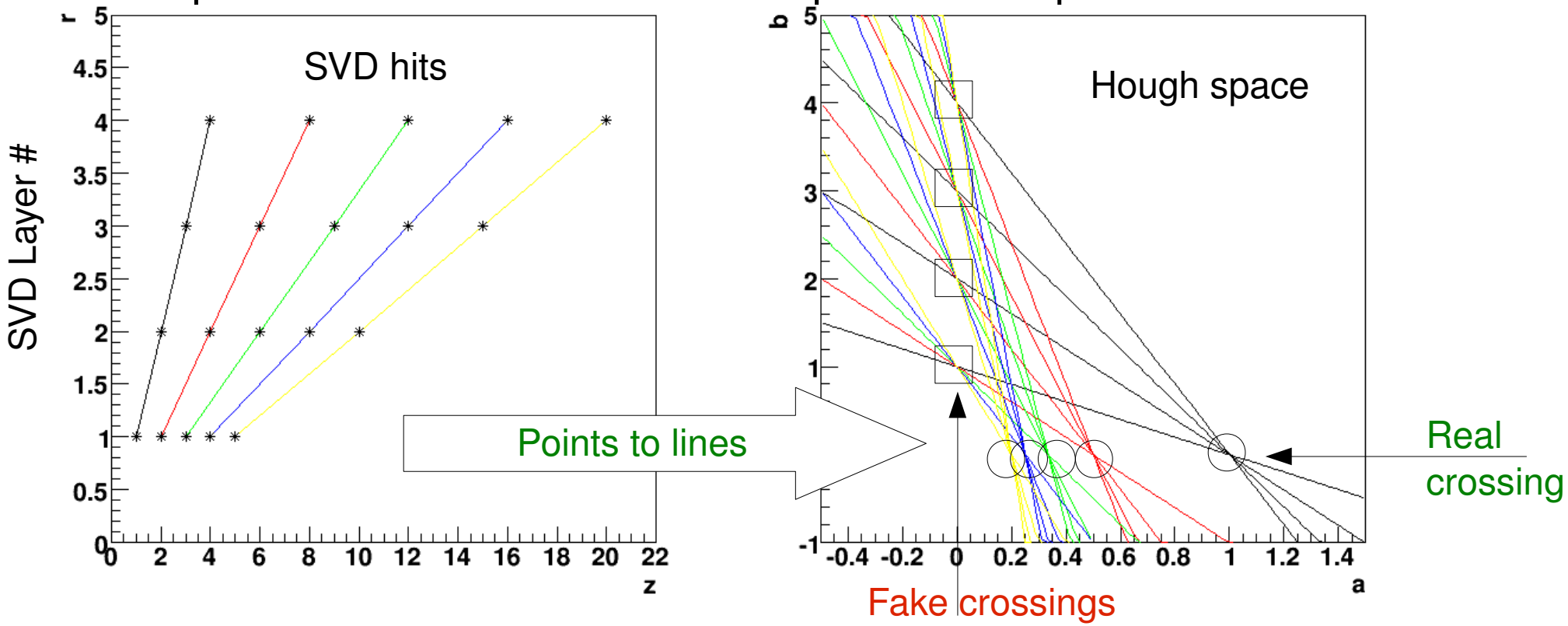
Tracking in 2D: Hough transform

Line: r = a z + b

Hough transform: b = r – a z

r-z space

parameter space

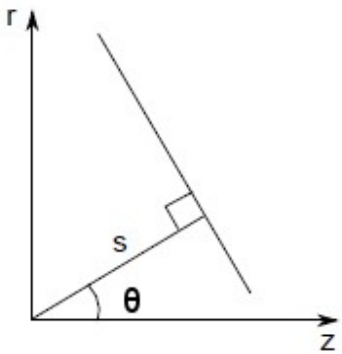


Problem of straight line parametrization:

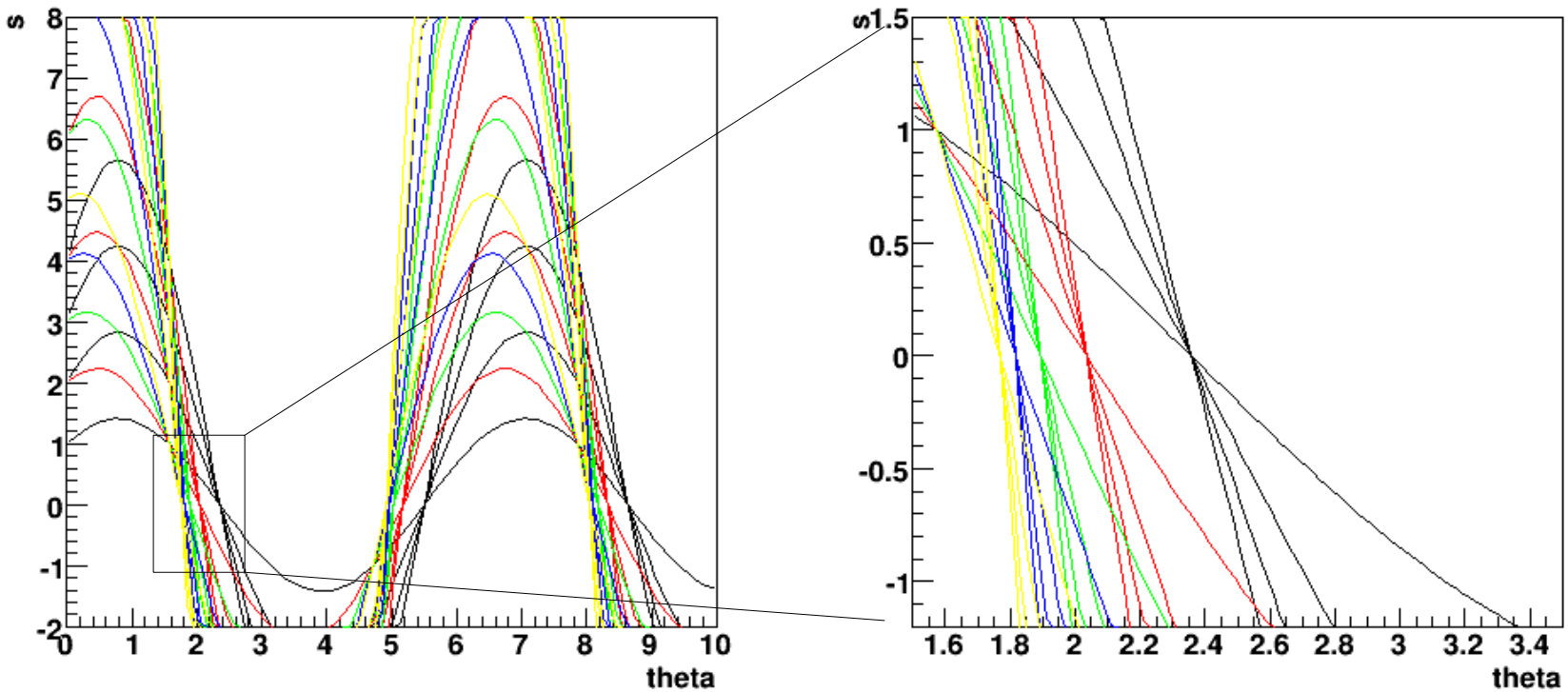
Large Hough space: $a\ (=\tan(\theta)) \rightarrow \infty$ for $\theta = 90°$

Solution: change the parametrization

line: $s = z\cos(\theta) + r\sin(\theta)$



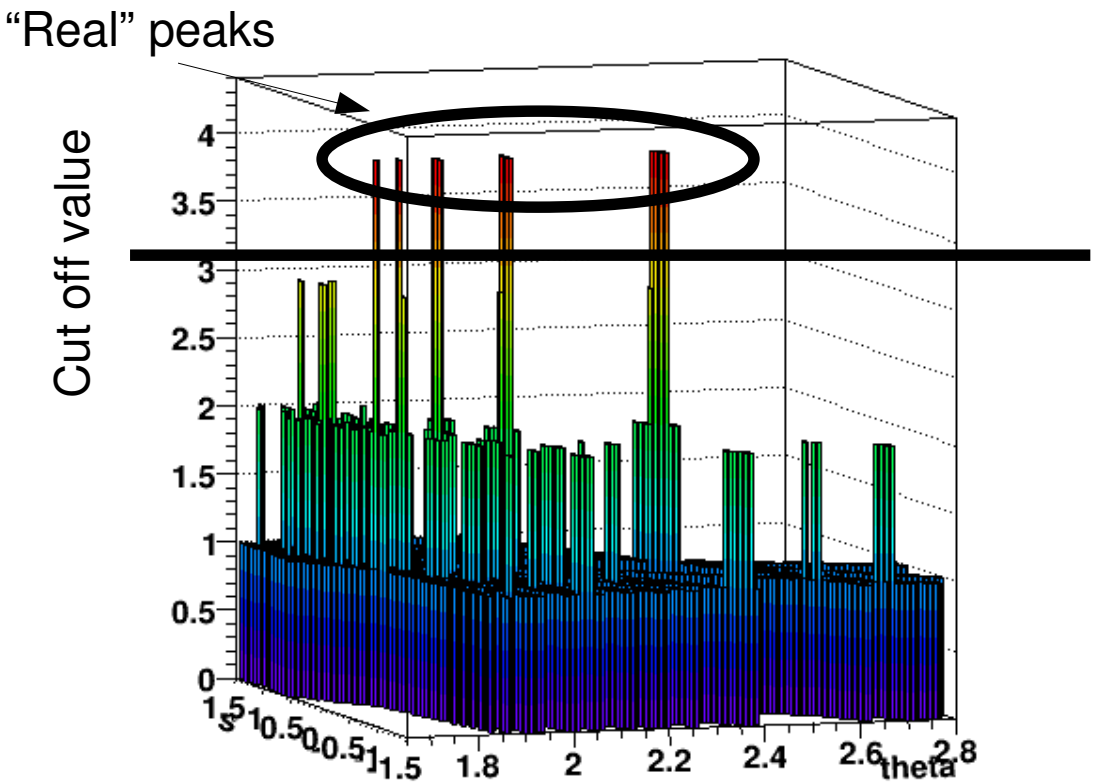
Parameter space becomes periodical in θ



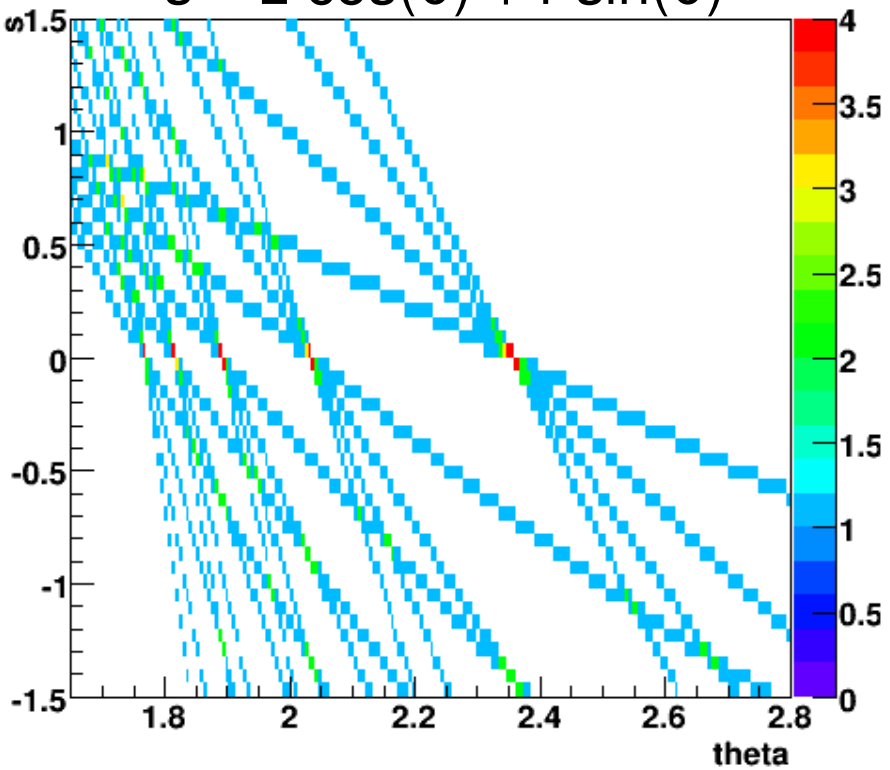
Peak Finding in (s, θ) Hough space

Method: run along θ parameter and calculate the corresponding s value

- Define peak finding strategy (easiest approach define cut off value)
- Finding all peaks is essential not to loose data
- Additional fake tracks will decrease the data reduction ratio



$s = z \cos(\theta) + r \sin(\theta)$

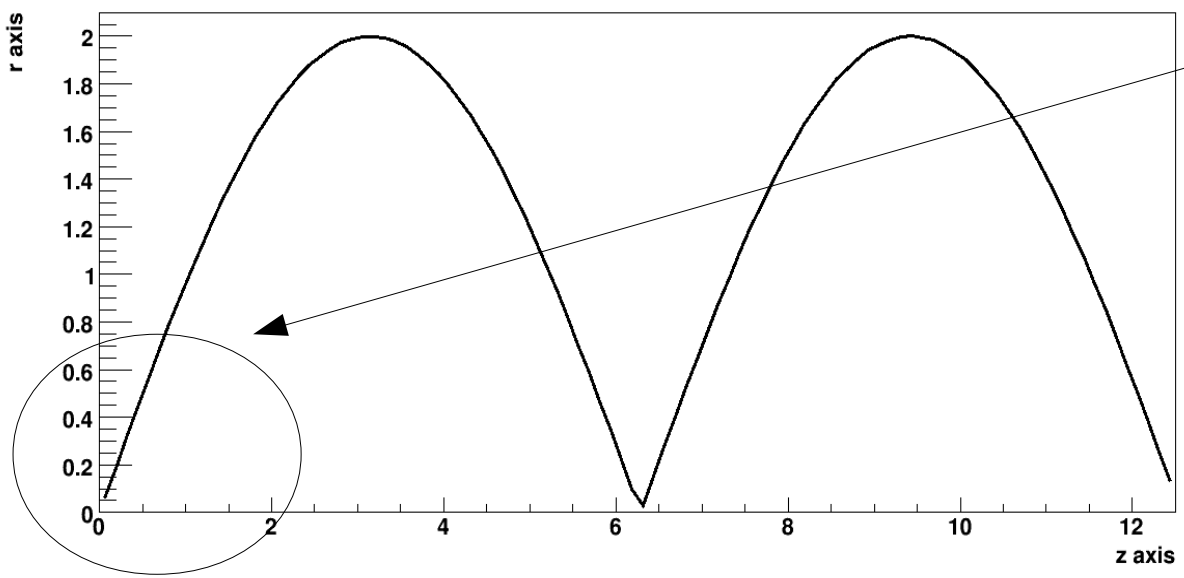


Particles in the r-z projection are not straight lines!

How does a Helix look in r-z-space?

$r = |a \sin(b z)|$: helix passes the origin

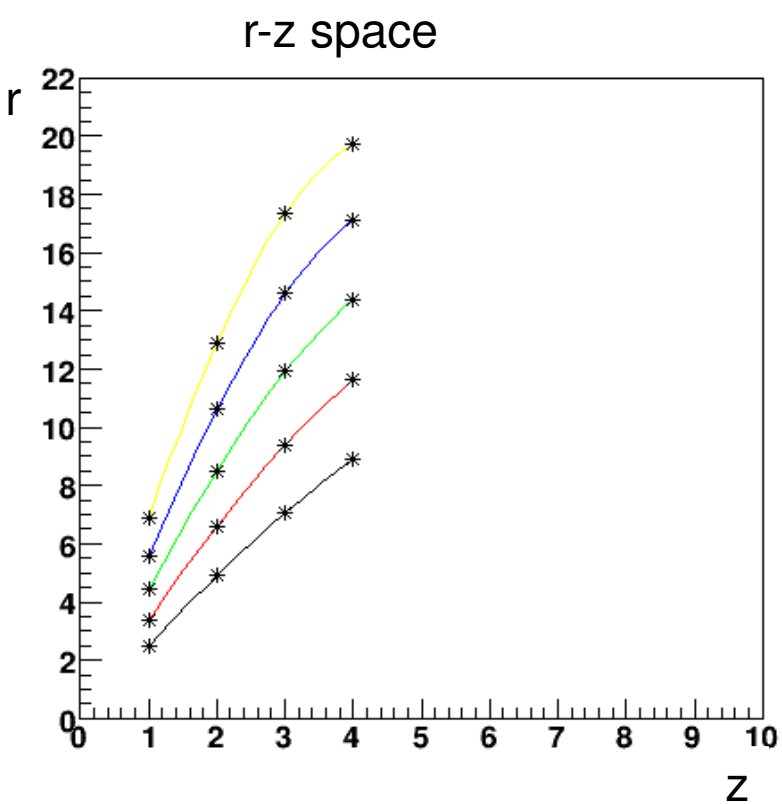
$r = |a \sin(b (z+z_0))|$: helix with offset in z

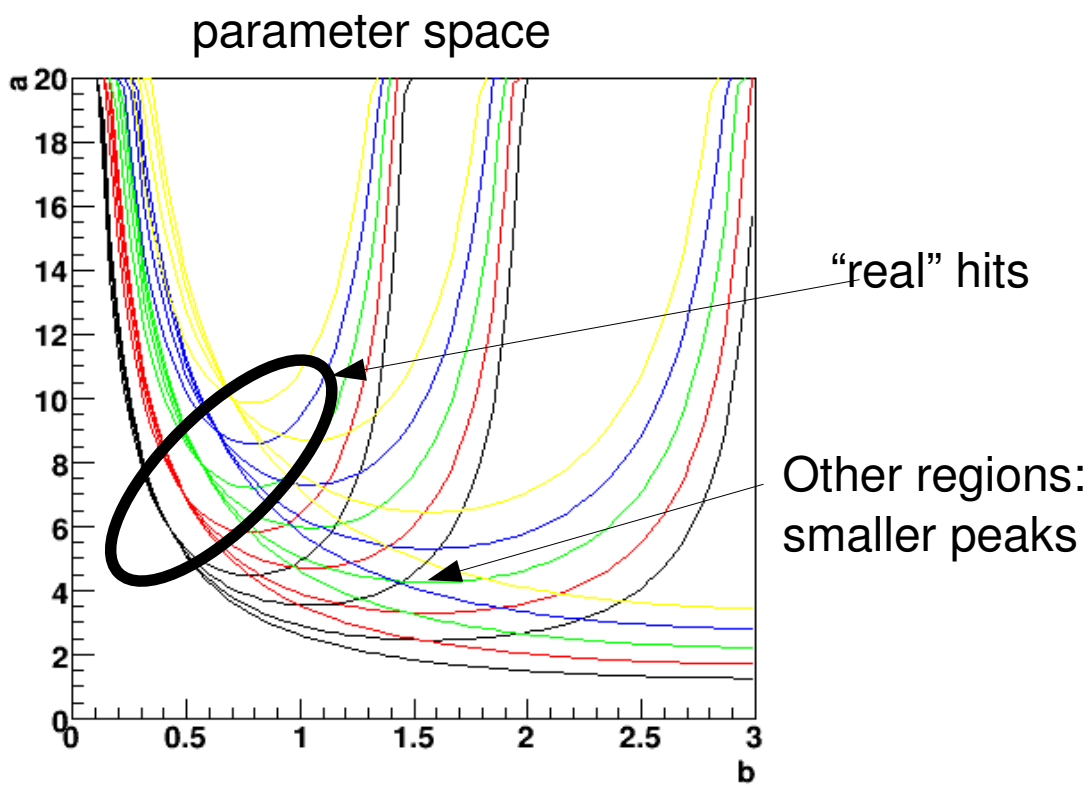


Straight line approximation
- for high momentum tracks (large a)
- for very steep tracks (small b)

Hough transform of a sine wave

Track in r-z space: r = a sin(b z) Hough transform: a = r / sin(b z)

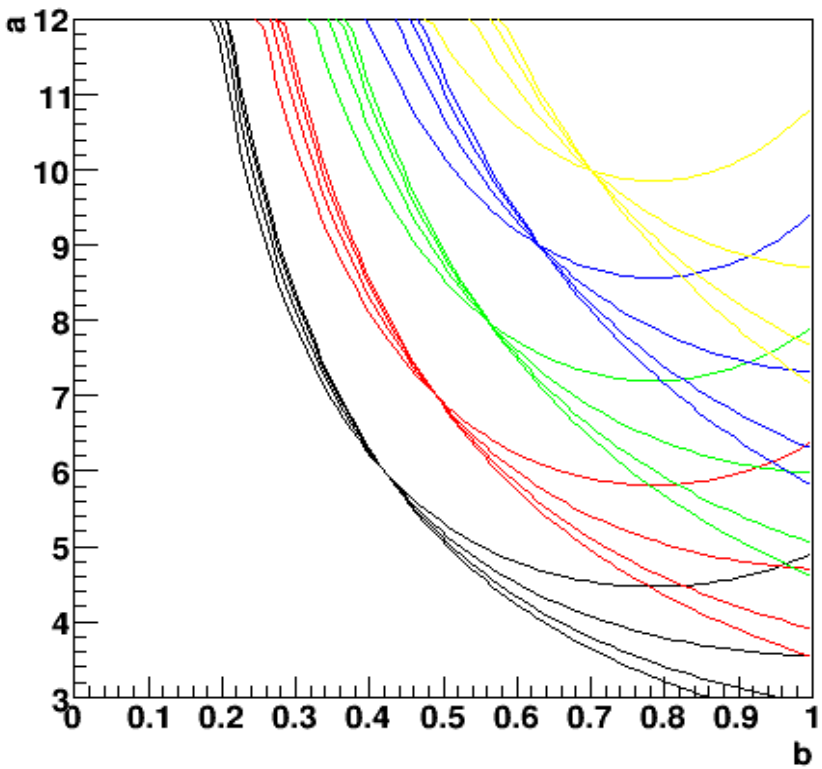




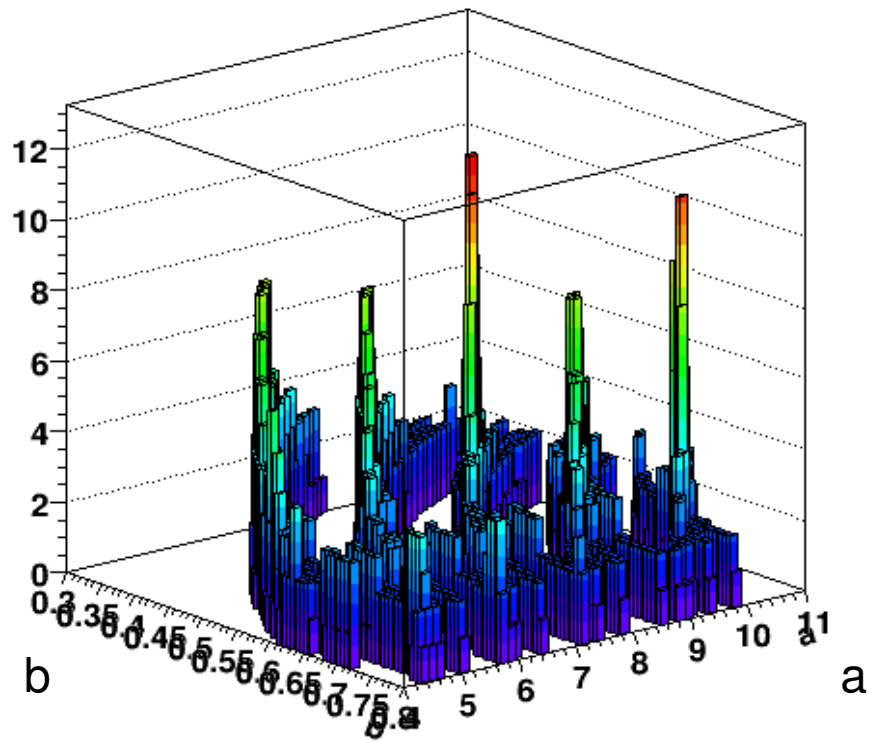
Hough transform of a sine wave - continued

$$a = r / \sin(b\, z)$$

Parameter space (Zoom in)



2D histogram of parameter space

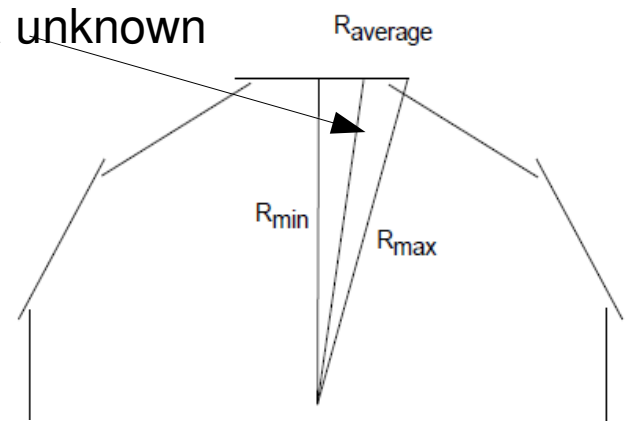


Test on real events

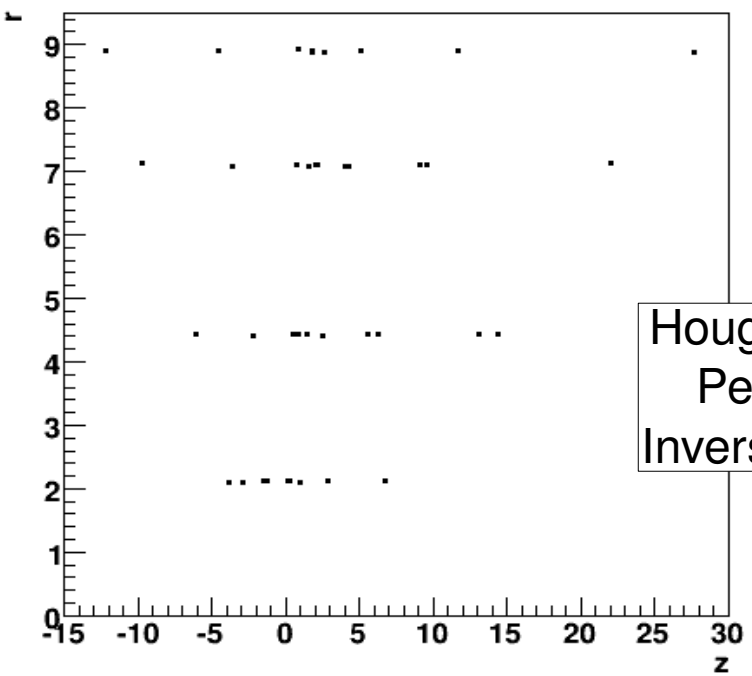
Belle Monte-Carlo D* decays

Information from SVD r-phi strips
only z-position & DSSD# of SVD hits

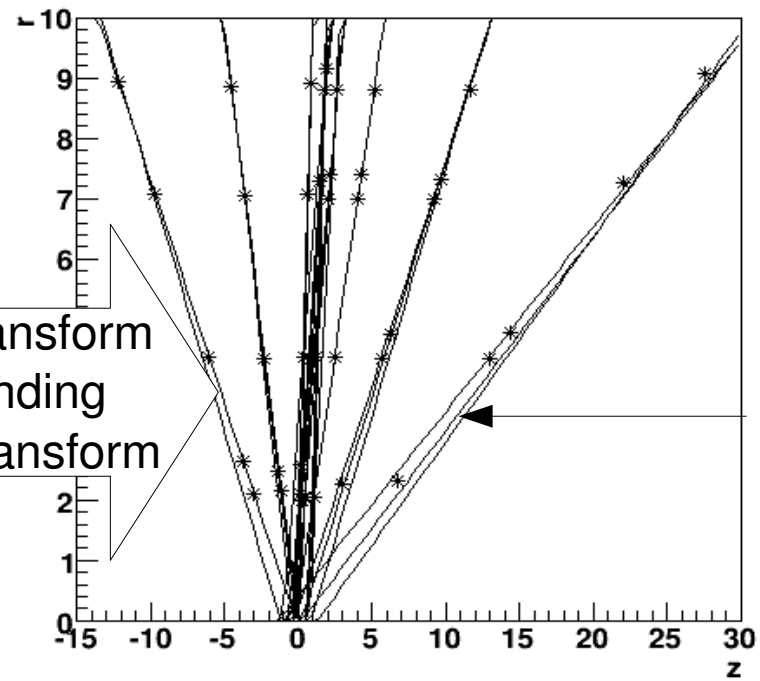
Real R unknown



All strips put to avg. radius $(R_{max}+R_{min}) / 2$



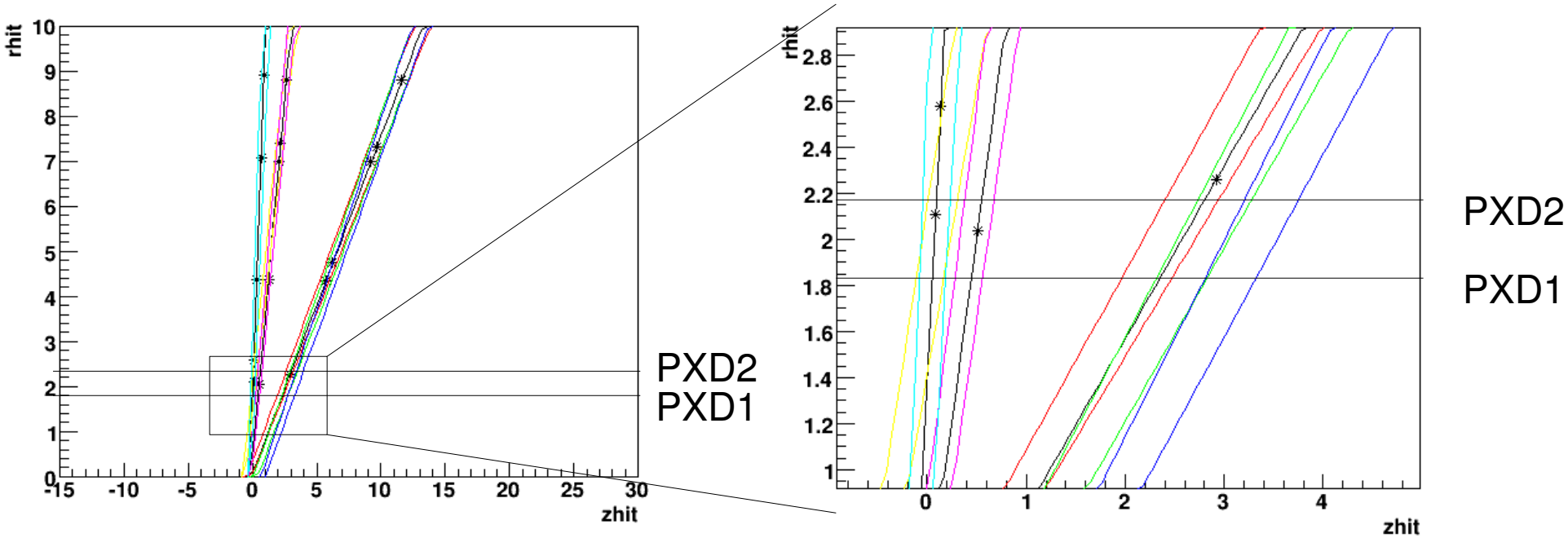
Hough transform
Peak finding
Inverse transform



Too many tracks found

Next step optimization of road width

- All tracks need to be found → study efficiency
- Width of the roads needs to be narrow enough to achieve the required data reduction (10-20)
- Width needs to be wide enough not to loose data



Thoughts about Hardware Implementation

- Work in sectors in r-phi
- Reduce number of hits and peaks
  - Minimize confusion in Hough space → efficient peak finding
- determine Shape of the sectors (minimum p_T of tracks found)
- ≥ 12 sectors (12 SVD ladders in 1st layer)
- Sectors can be computed in parallel
- Use Giessen ATCA system

Hardware ATCA crate

ATCA Advanced Telecommunications Computing Architecture

Integrated bandwidth of backplane: up to 2.1Tbit/s

fibre channel connections 1.0625 Gb/s

single ATCA crate can host up to 14 boards

Boards with FPGAs (Field Programmable Gate Array)

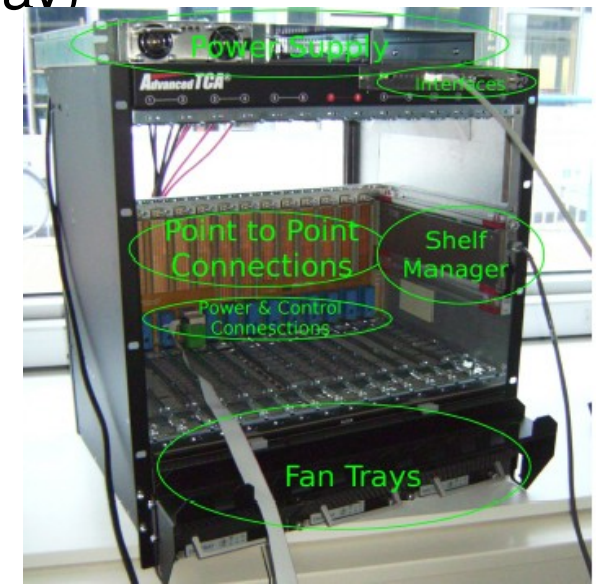
10Gbps bandwidth each channel

each FPGA is equipped with DDR2 SDRAM

Connected via Gbit Ethernet, optical links or

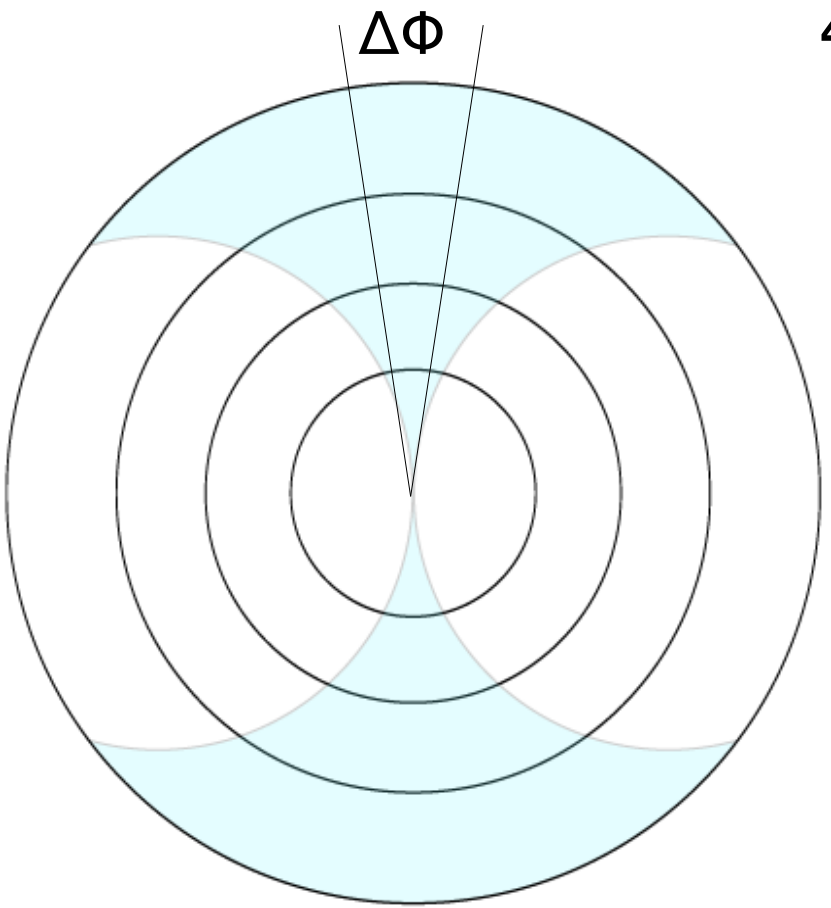
Rocket I/O

Soeren Lange's talk



Shape of a tracking sector in r-phi

Rough sketch of a sector



40-50 such sectors rotated by ΔΦ

shape corresponds to a p_T- cut

here p_T > 50 MeV

→ Hardware implementation
share SVD data in
neighboring sectors

Conclusion

- PXD data need to be reduced (10 times the size of all other data in Belle II)
- Algorithm proposed using r-phi strips of SVD (only z information)
- Initial studies with Hough transform encouraging
- Ready to start detailed MC studies
- Background studies planed
- Implementation in the FPGAs
- Hardware: using ATCA system from Giessen