Status of KUPID v2.0

2009.6.25.

Eunil Won

for Eugene Hong

(Going OSU this summer)

Korea University

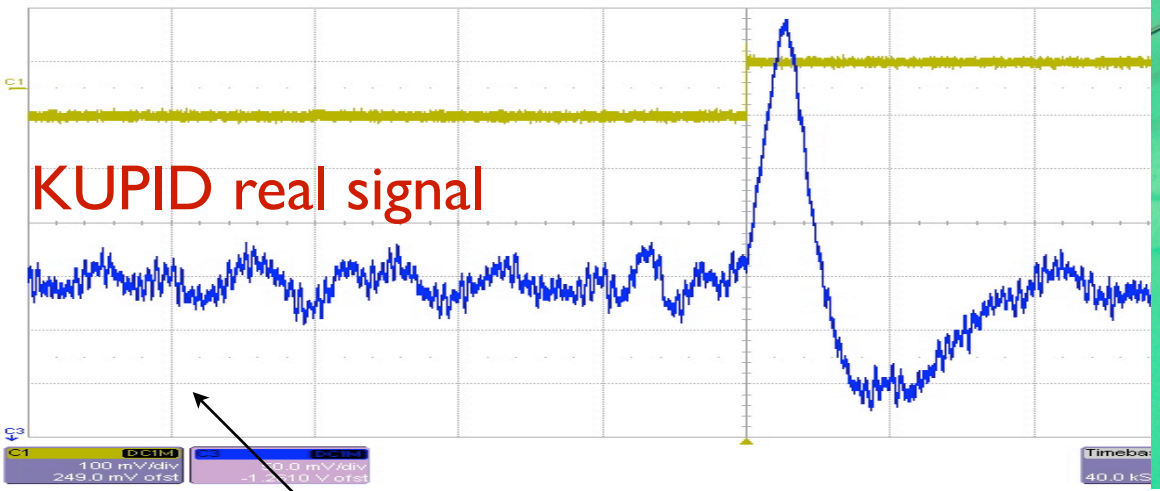
History of KUPID Development

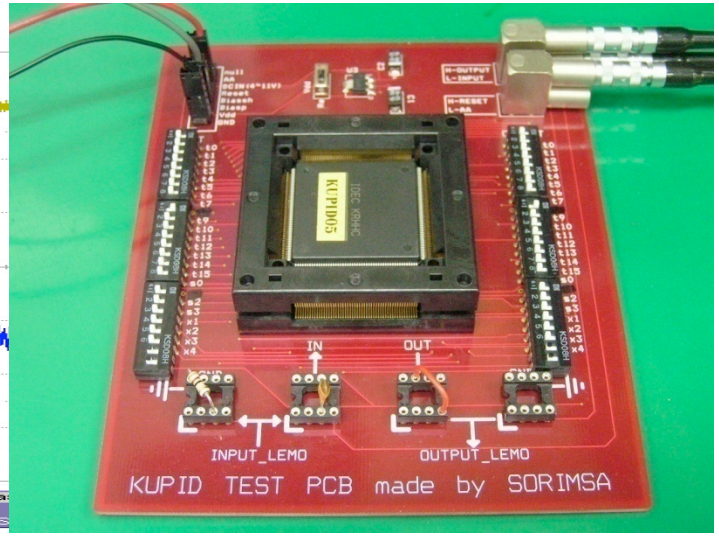
- 2006: KUPID (Korea University Preamplifier-shaper Integrated Design) ASIC fabrication thoughts - after one year successful R&D of VA-hybrid board by KU
- 2006: v1.0 submitted to Dongbu-Anam 180 nm process (a foundry in Korea)
- 2006. September: v1.0 chip received
- 2007. Jan. : we saw the first signal from KUPID v1.0

  - rather noisy, ENC~O(30,000)

  - small amplification: cannot detect one MIP from Si sensors
- 2008: v2.0 design optimized for small ENC and large gain
- 2009. May: v2.0 design submitted to IBM 130 nm process (via MOSIS) : Belle-II note 0008 is on the web

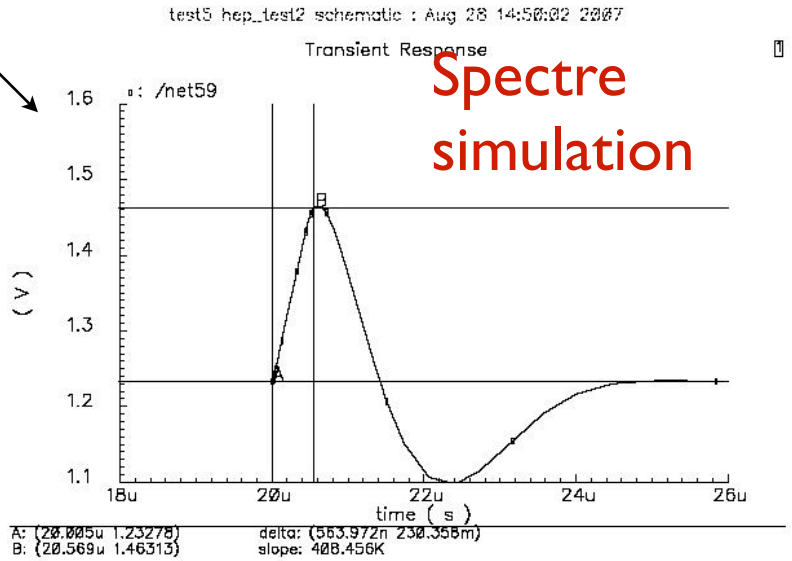
KUPID v1.0





(New PCB for better biasing)

Almost same scale

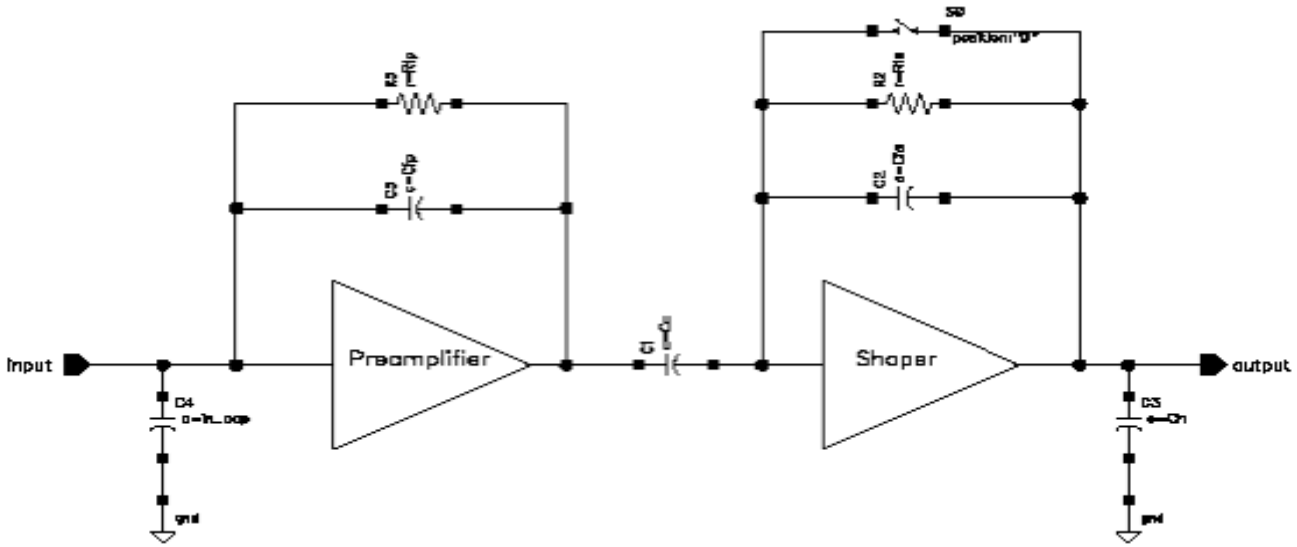


Now at least simulation "agrees" with data !

: due to

- Cable capacitance inclusion
- Availability of Spectre transient response

Basic structure: a preamplifier-shaper chain



A simplified view of (typical) preamplifier-shaper chain design.

- preamplifier: pMOS based folded-cascode structure with current sources
- shaper: typical CR-RC filtering

Note: no sample-hold, no MUX in v2.0

Noise sources from amplifiers

- Transistor 1/f noise (carrier trap in semiconductor), transistor channel noise, and Bulk-resistance noise (white thermal noise) are main sources of noise
- Noise of a charge amplification electrons is expressed in equivalent noise charge (ENC)

$$\mathrm{ENC/C_{det}} = \frac{e}{q}\left[\frac{A_1}{WL} + \frac{A_2 kT}{g_m T_p} + \frac{A_3 kT}{T_p}\right]^{\frac{1}{2}}$$

From Nygard Nucl. Instr. Meth. A 301, 506 (1991).

A_i : constants g_m : transconductance T_p : output peak time $e = 2.718$

Key point to reduce ENC : control W, L and g_m of input transistor

Noise sources from amplifiers

- In strong inversion region,

$$g_m \propto \sqrt{\frac{W}{L} I_D}$$

I_D : transistor drain current

- As a result, usually we make input transistor with small L and long W

Operating region and W/L of input transistor

- There are three operating regions for FET, weak inversion, strong inversion, and velocity saturation region.
- For each region, different optimized value for input transistor gate capacitance

From Connor Nucl. Instr. Meth. A 480, 713 (2002).

$$\frac{C_{\mathrm{det}}}{I_D} < \frac{6\mu}{v_{\mathrm{sat}}^2}$$

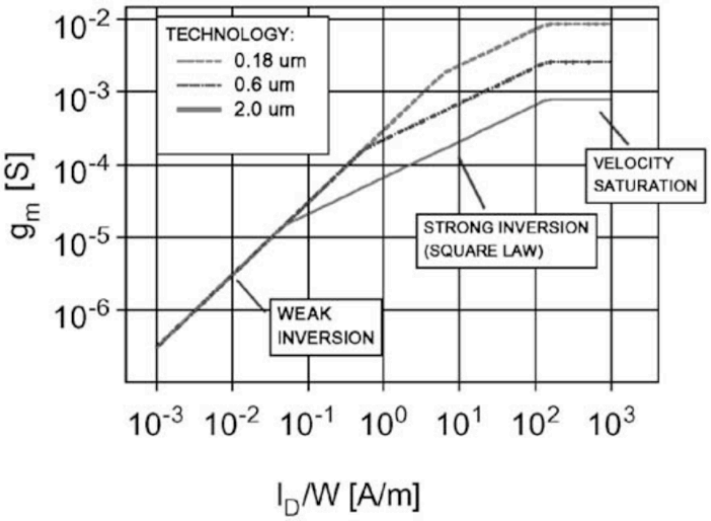
velocity saturation

$$\frac{6\mu}{v_{\mathrm{sat}}^2} < \frac{C_{\mathrm{det}}}{I_D} < \frac{3L_{\mathrm{min}}^2}{2\mu(nV_t)^2}$$

strong inversion

$$\frac{3L_{\mathrm{min}}^2}{2\mu(nV_t)^2} < \frac{C_{\mathrm{det}}}{I_D}$$

weak-strong boundary



Operating region and W/L of input transistor

- With drain current 200 μA, 20 pF detector capacitance, our system is operating in Weak-strong Inversion boundary
- In this case, optimized value for input transistor gate capacitance is

$$C_{g,opt} = \frac{L_{min}^2}{2\mu(nV_t)^2} I_D = 1.1 \text{ pF}$$

From Connor Nucl. Instr. Meth. A 480, 713 (2002).

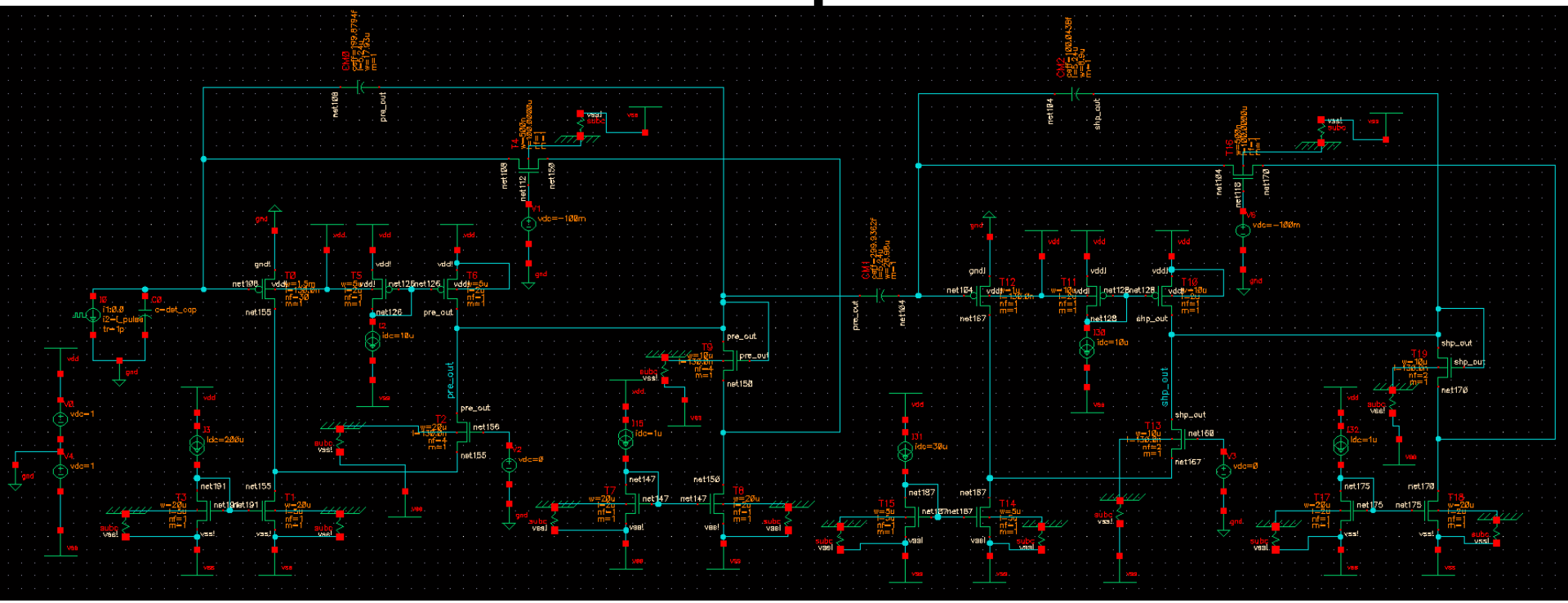
Decision of operating region and W/L of input transistor

- From simulation result, we can obtain Cgg (notation in SPICE)

$$C_{gg} = \frac{dQ_g}{dV_g}$$

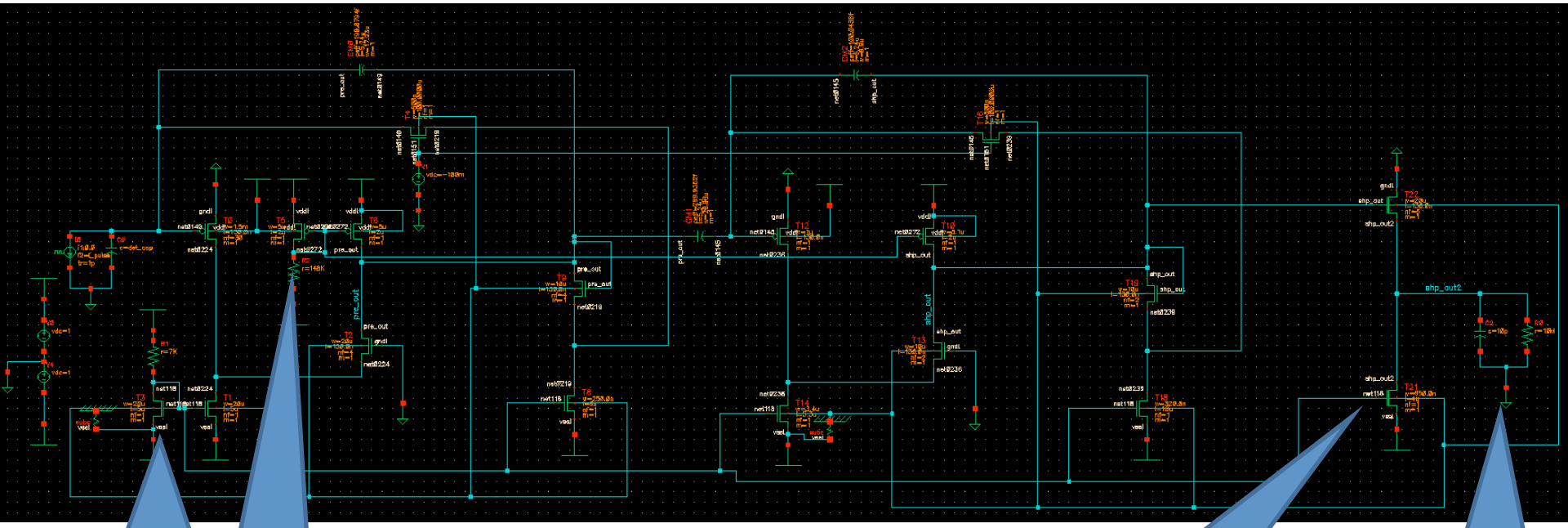
- We obtained Cgg = 1 pF with W/L = 1.5um/ 130nm
- We started schematic simulation for our preamplifier with this W/L value.

Schematic Drawing of preamp +shaper



Until now, we designed 5 different preamplifier-shaper channel.
They have different models (nfet, nfet_rf), different input transistor gate capacitance, and current source load for readout.

set4 : lowest ENC expected



Bias control combined.

Current source load.

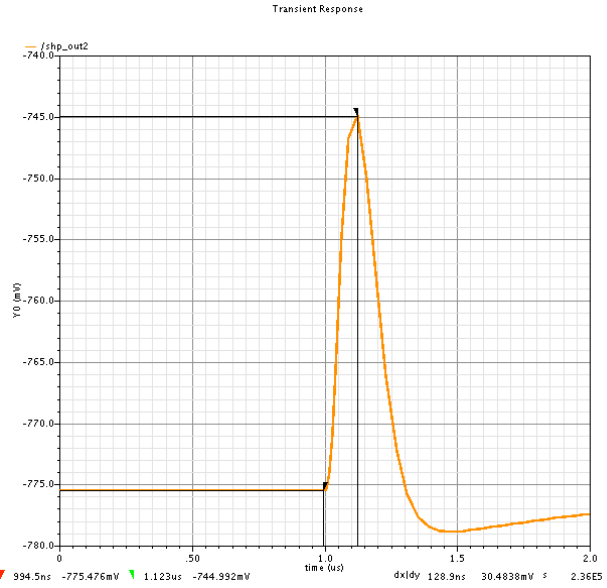
10MΩ 10pF Probe.

For lowest noise, current source FETs should be small as possible as all FETs are noise source.

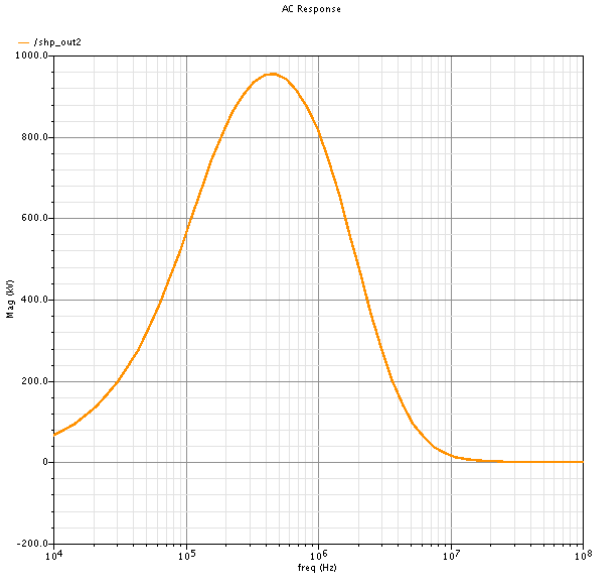
Current source load is attached to make simulation result same with real data (scope read).

Simulation result.
(set4 : lowest ENC expected)

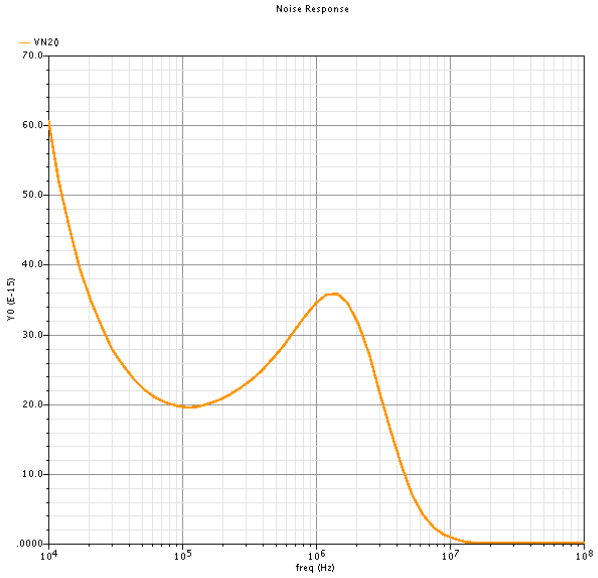
Transient



AC

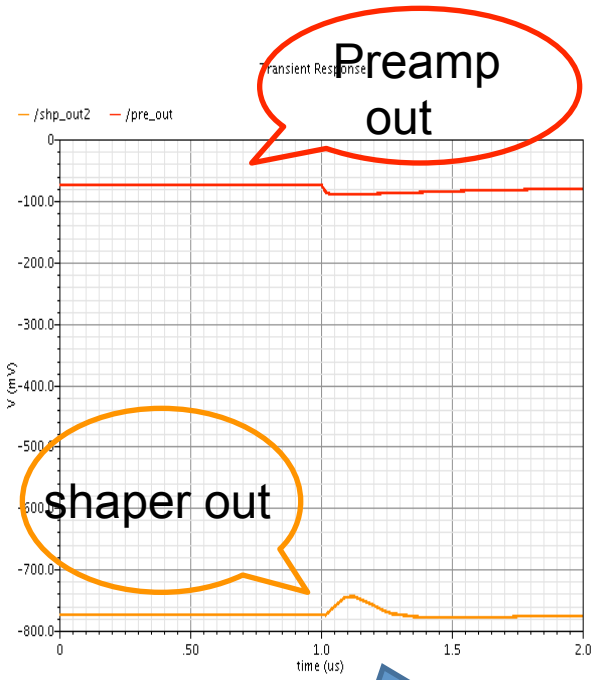


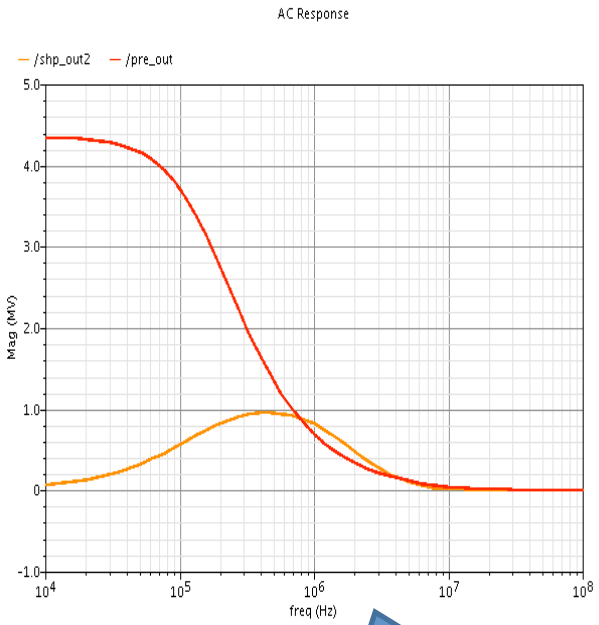
Noise

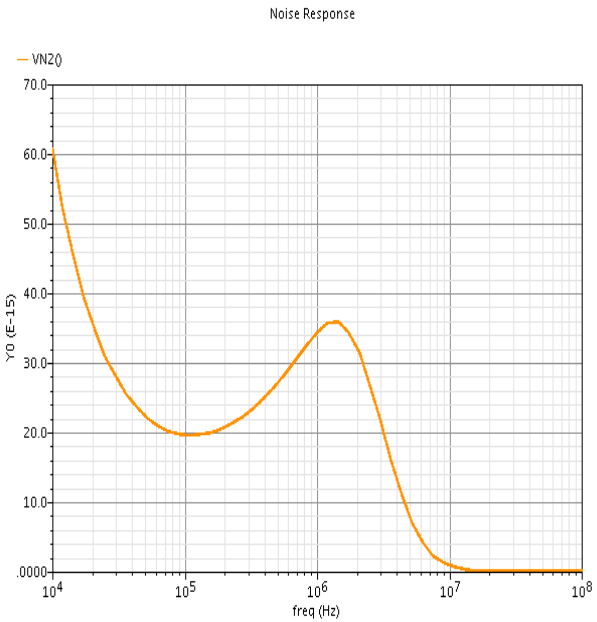


At 10 pF detector capacitance, output signal from 1 MIP (25,000 e-) is 30.4mV with 130 ns peak time.

Simulation result.
(set4 : lowest ENC expected)







Gaussian shape output.
Shaper out -> low offset
Preamp out -> high offset

Shaper AC response shows CR-RC filtering.

Simulation result. (set4 : lowest ENC expected)

Detector Cap (pF)	Vop (mV)	RMSnoise(10k,100MHz) (V)	ENC
0	44.0	0.0002437	138.4
5	36.1	0.0003017	208.9
10	30.4	0.0003681	302.7
15	25.7	0.0004249	413.4
20	21.8	0.0004714	540.6

We think we can read output signal from 1 MIP as ENC of 302 is much less than input electrons 25,000

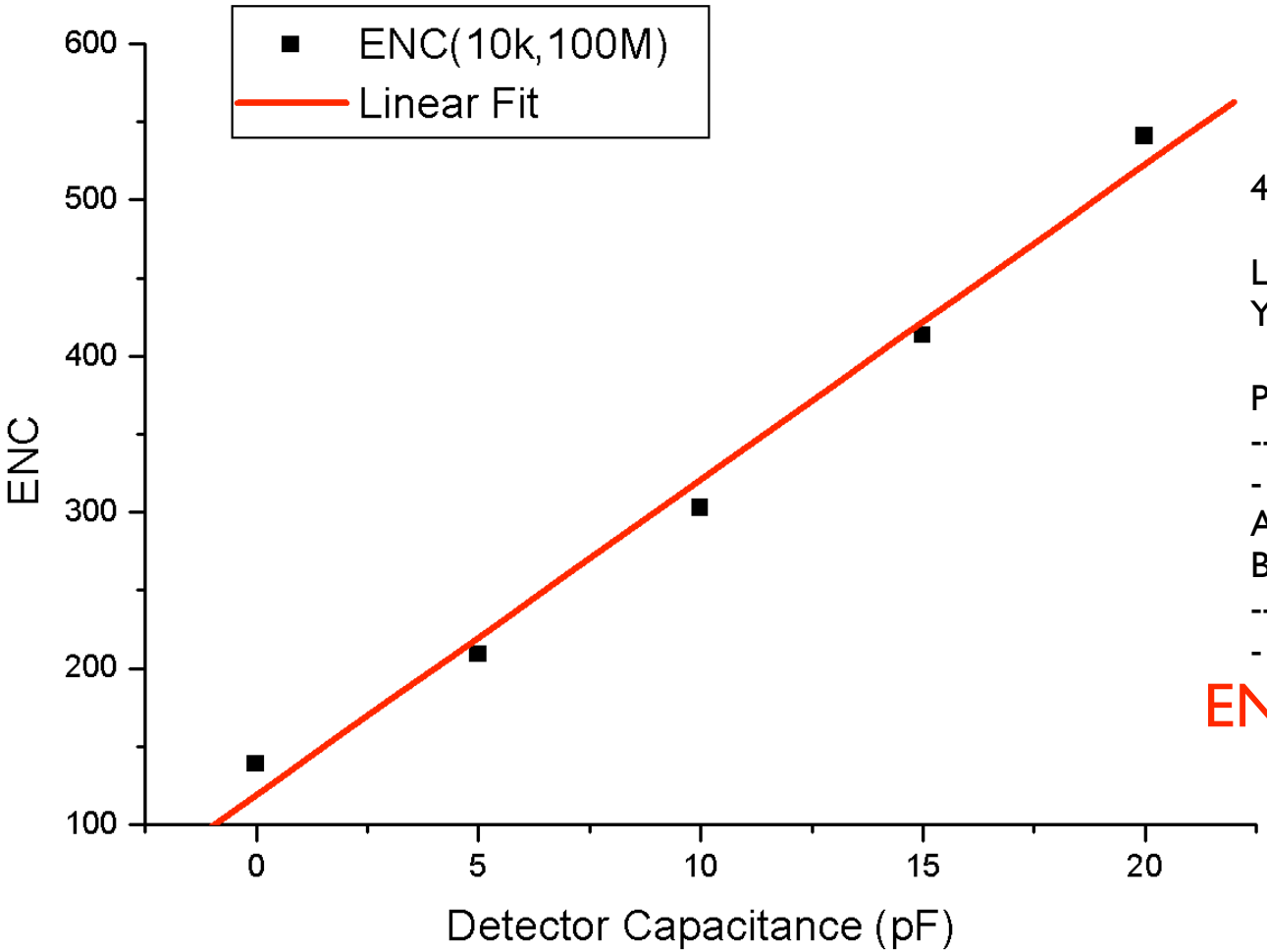
$$input\ el.\ :\ Vop\ =\ ENC\ :\ noiseRMS$$

$$ENC = \frac{25{,}000 \times noiseRMS}{Vop}$$

1 MIP = 25,000 electrons

However, real noise detection value (with chip) may be bigger than above.
There will be many parasitic noise sources such as detector leakage current, noise from power supply, etc.

Simulation result. (set4 : lowest ENC expected)



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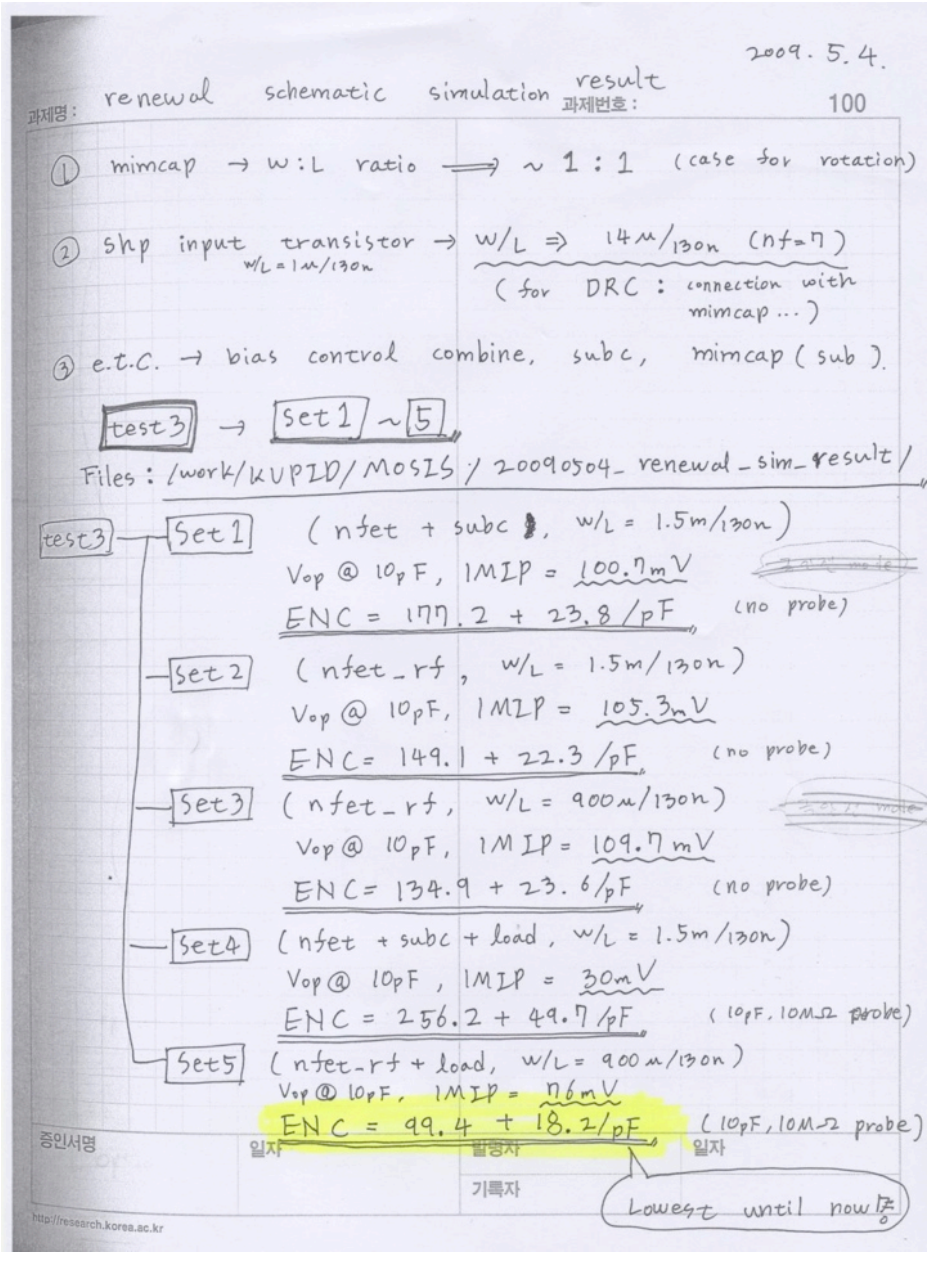
Linear Regression for Data1_B:
Y = A + B * X

Parameter	Value	Error
A	119.02	15.60679
B	20.178	1.27429

ENC = 119 + 20.2 /pF

Other designs show little more noise than this.
(ex. ENC = 225 + 26 /pF)

Further reduction of ENC noise



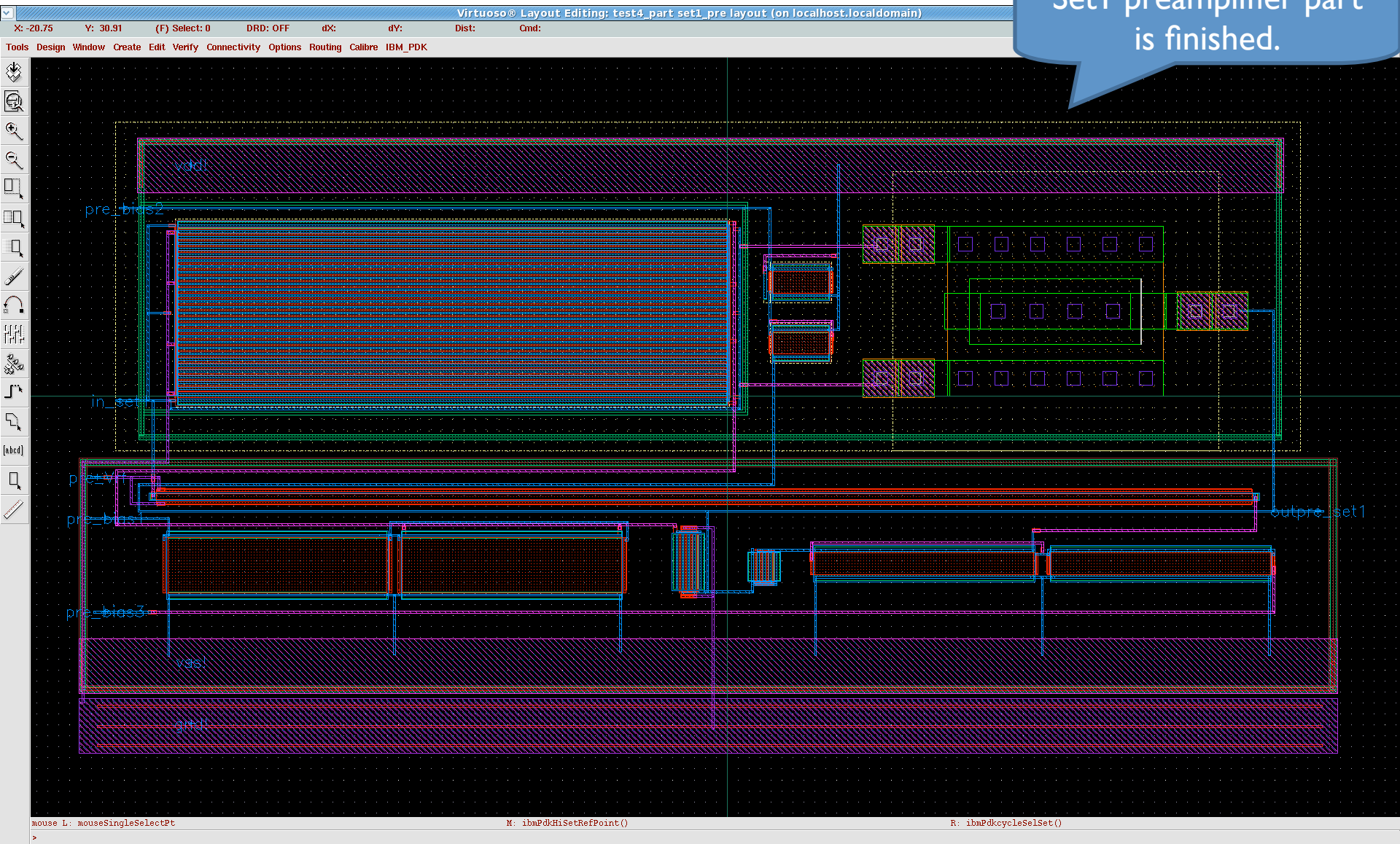
Snapshot of Eugene's logbook:
Note the date (2009. May, 4) and the submission deadline is 2009. May 11

Further optimization in the shaper side parameters - simulation shows < 100 +- 18 /pF

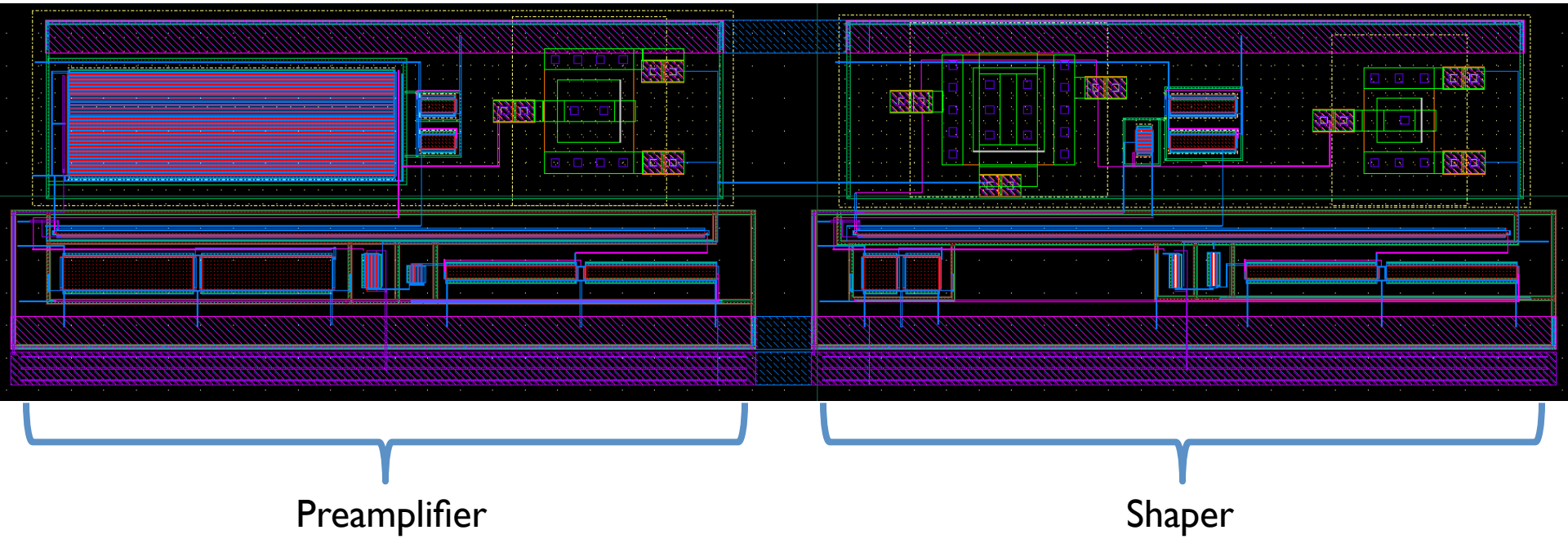
But: usually SPICE simulation underestimates real ENC : so don't get too excited yet

Layout design (preamp)

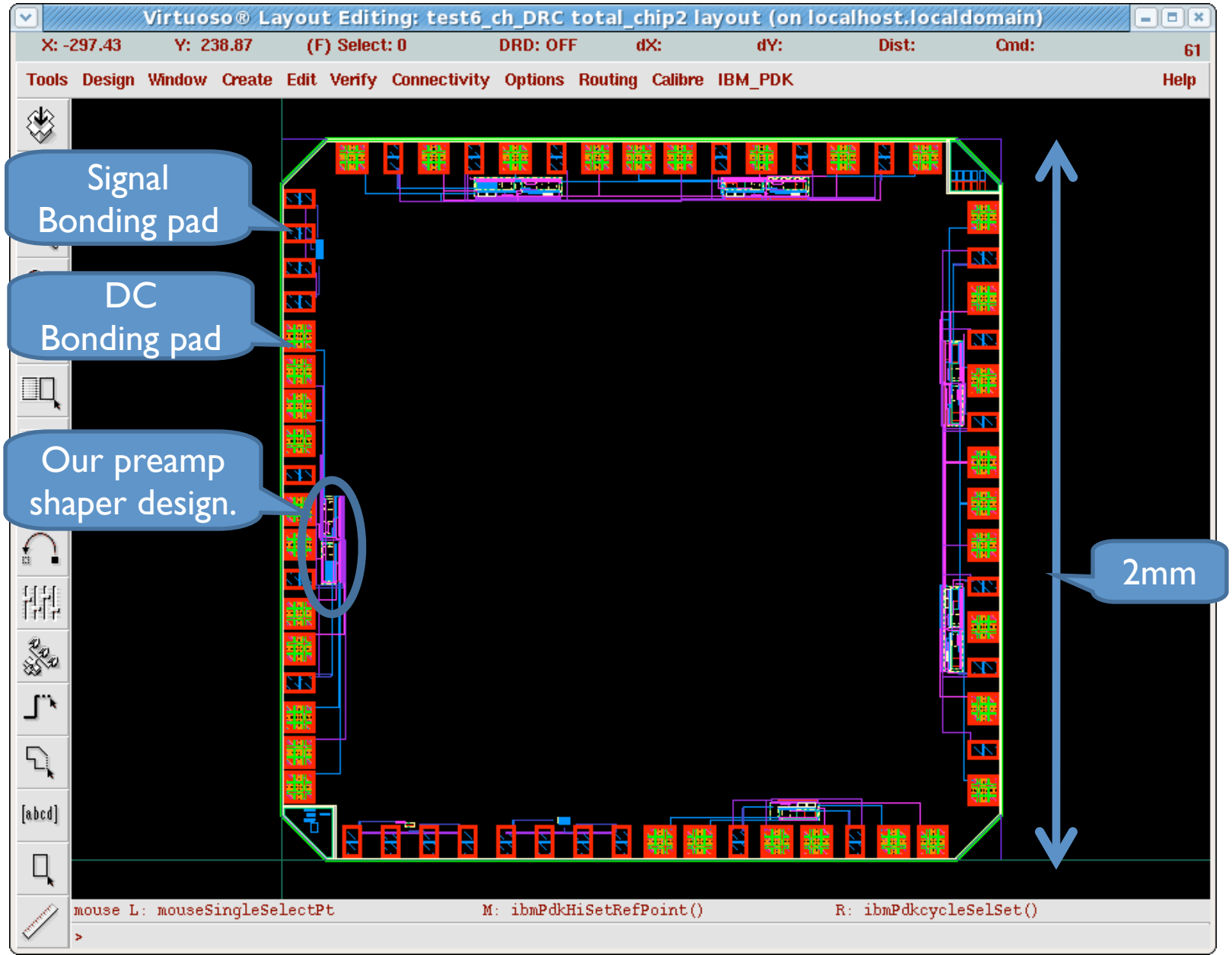
Set1 preamplifier part is finished.



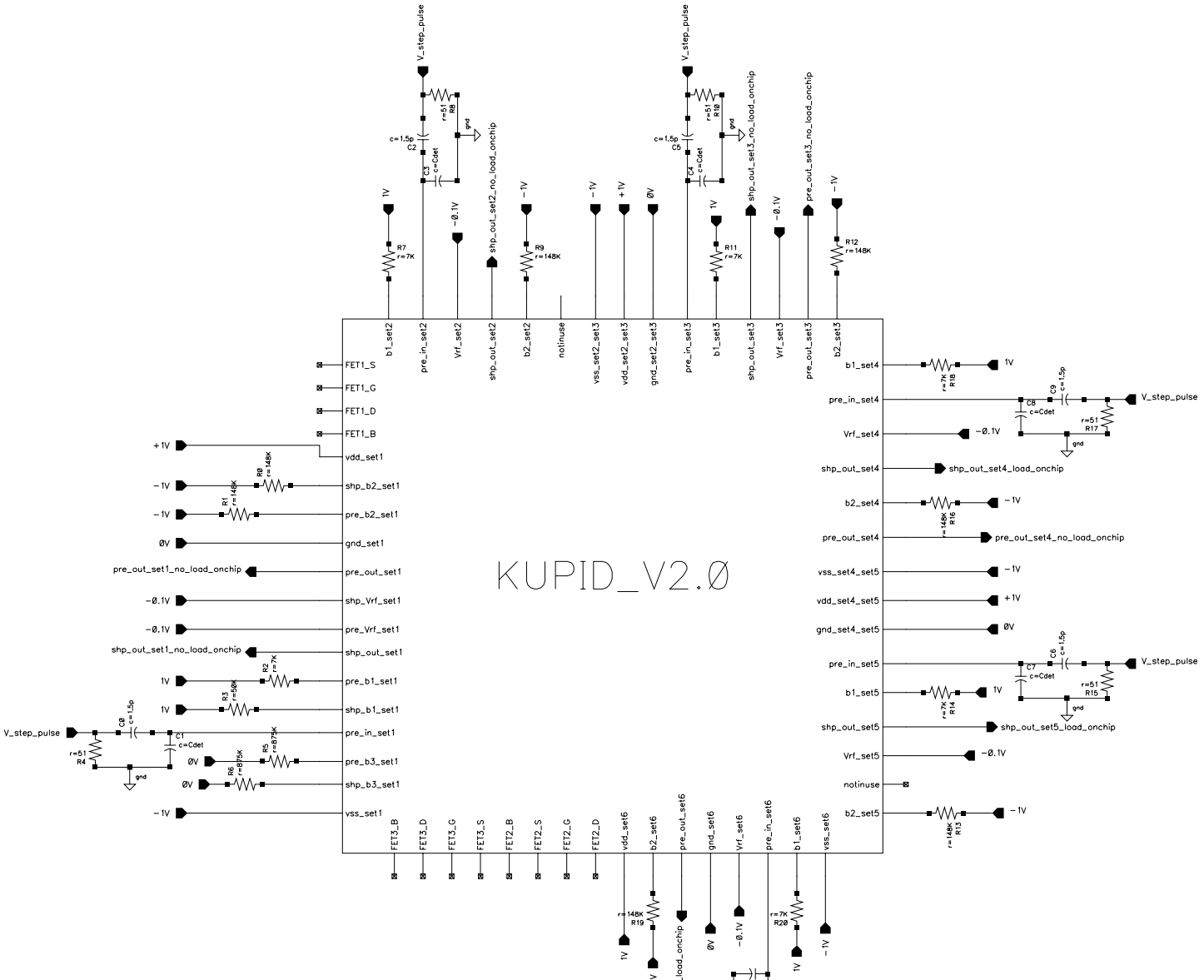
Layout design for Set1 (preamp +shaper)



Floor plan


Virtuoso® Layout Editing: test6_ch_DRC total_chip2 layout (on localhost.localdomain)
X: -297.43
Y: 238.87
(F) Select: 0
DRD: OFF
dX:
dY:
Dist:
Cmd:
61
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Calibre
IBM_PDK
Help
Signal Bonding pad
DC Bonding pad
Our preamp shaper design.
2mm
mouse L: mouseSingleSelectPt
M: ibmPdkHiSetRefPoint()
R: ibmPdkcycleSelSet()

Test board schematic started



Summary and plan

- KUPID 2.0 design submitted to IBM 130 nm process on May 11, 2009
- We expect improved ENC values, based on the SPICE simulation
- We expect to receive chip this summer: hardware test will be interesting
- We plan to include sample/hold, MUX at the next stage