Report on PXD Session

H.-G. Moser
Max-Planck-Institut fuer Physik

2nd open meeting
July 4, 2008

"2nd Open meeting for the proto-collaboration Joint IR/PXD/SVD session "

Friday 04 July 2008
from **08:30** to **12:30**
at 3 go-kan Seminar Hall

Friday 04 July 2008

Friday 04 July 2008

top

08:30->*12:30* **Joint IR/PXD/SVD session** (Location: 3 go-kan Seminar Hall)

08:30	Self introductions (10')	Everyone, 30 seconds
08:40	IR (Interaction region), detector-machine interface, beam pipe (20') (Slides)	M. Iwasaki
09:00	Short introduction to Super Belle Geant4 and optimization of the vertex system (25') (Slides)	T. Hara
09:25	Overview on pixel layer requirements (20') (Slides)	G. Varner
09:45	Pixel simulations, backgrounds (15')	A. Frey
10:00	Overview of pixel detector based on DEPFET and common issues: expected performance, backgrounds (20')	L. Andricek
10:20	Coffee break	
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11:55	Other DSSD R&Ds (05')	T. Tsuboyama
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12:10	General discussions & contingency (20')	

Overview on pixel layer requirements (G. Varner, Hawaii)

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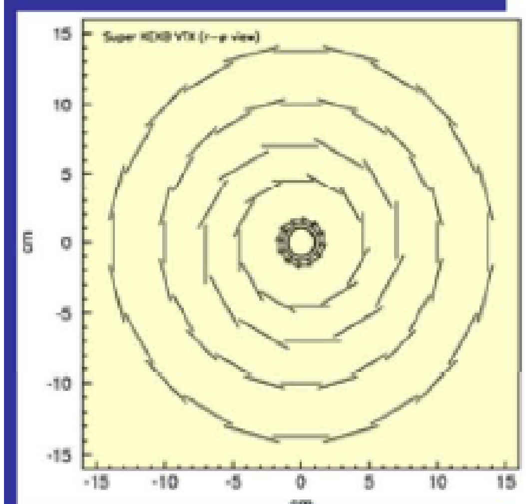
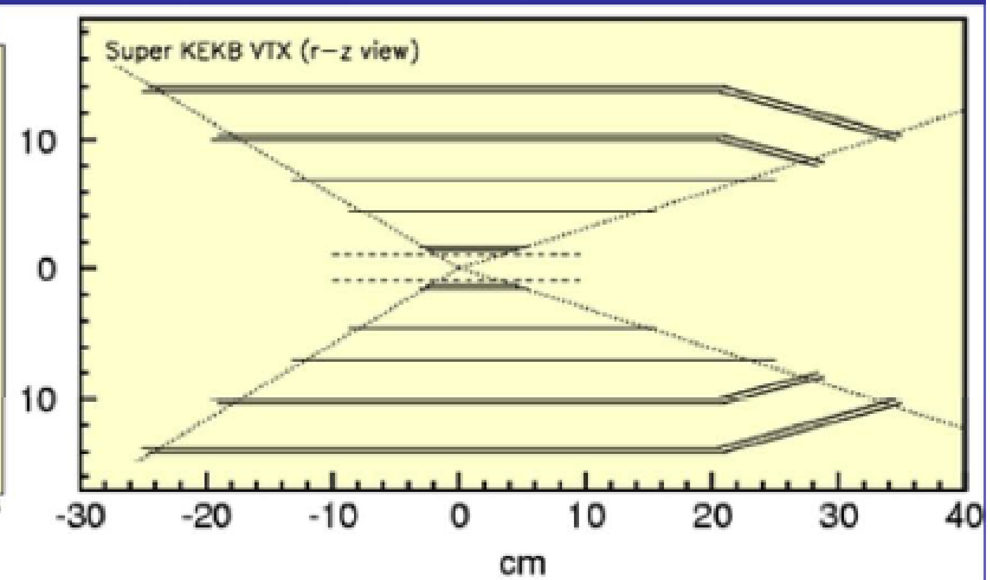
Overview on pixel layer requirements (G. Varner, Hawaii)

Sensor configuration

- Belle acceptance: 17<θ<150°
- Outer radius: 150 mm (CDC)
- Inner radius: 13 mm (Beam pipe)
  - For better vertex resolution.
- 5 layers
- Total sensitive area ~1 m^2

- Inclined sensors in Layer 4 and 5
  - Reduce readout channels
  - Reduce material budget
  - Reduce the ladder lengths (Without slant sensors, length ~75 cm)
- Option in the Layer 1 sensor
  - DSSD (*striplet*) option → Super-layer
  - Pixel option





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Overview on pixel layer requirements (G. Varner, Hawaii)

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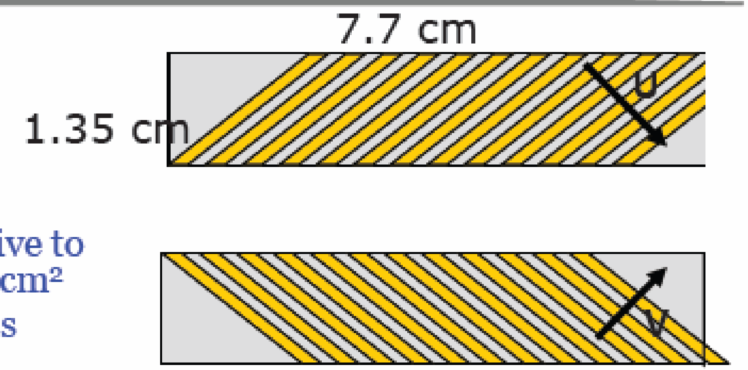
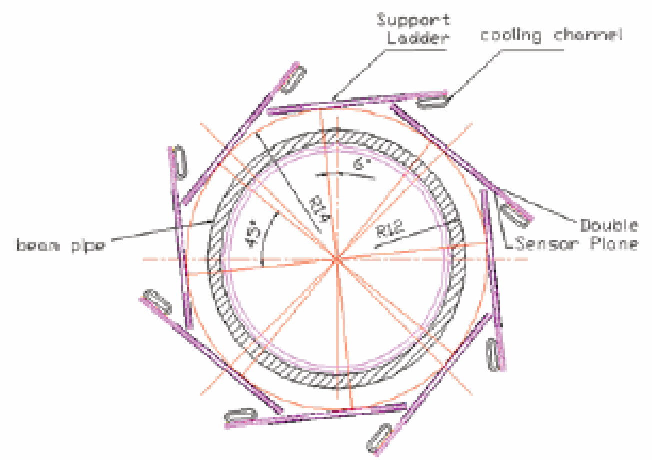
Inner Layers – a common theme

- Depends critically on background level
  - Striplet solution
    - Basically already available technology but more sensitive to background. OK for 1MHz/cm²
    - Factor few over “long” strips
  - Monolithic Pixel Solution
    - R&D is still ongoing but gives a large safety margin in terms of performance and occupancy
    - Cooling and mechanical issues need to be addressed
    - Active R&D program in place





What R&D still needed?

Overview on pixel layer requirements (G. Varner, Hawaii)

Pixel Occupancy Scaling

- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as “current”
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm^2
    - Reduction factor ~8400
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal loss:
    - 0.8μs SVD vs. 10μs PXD (could be improved)
    - Increase factor ~ 12.5
  - Grand total:
    - 10% * 20 * 8400^{-1} * 12.5
    - Can expect ~ 0.3% occupancy (no ghosting)

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Overview on pixel layer requirements (G. Varner, Hawaii)

Critical Technology R&D Issues

1. Readout Speed
2. Radiation Hardness
3. Thin Detector
4. Full-sized detector (mech/power)

Technology Options

1. DEPFET
2. SOI
3. CMOS MAPS
4. 3D (for future)

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Overview on pixel layer requirements (G. Varner, Hawaii)

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Pixel Upgrade Summary

- Specifications:
  - Are somewhat soft (TRACKERR easy, real G4 sims?)
  - Clear mandates
    - Handle higher particle fluences
    - Maintain or improve resolution (less material, smaller Rad)
  - Not needed (?) initially, but better to integrate vertexing
- A number of important issues:
  - Signal-Noise Ratio of thin devices
  - Infrastructure support
  - In the long term
    - **DAQ**: Support during years of operation
    - **Data rate**: avoid dominating the event size

Pixel Simulations (A. Frey, Munich)

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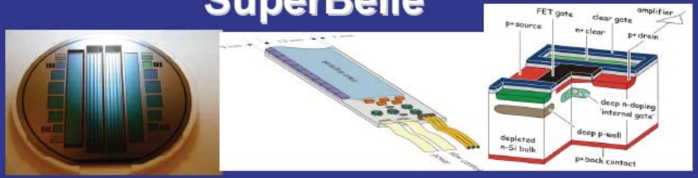
Pixel Simulations (A. Frey, Munich)

Proposal:
Consider Mokka framework (Geant4) for general superBelle MC

Simulation Studies of a (DEPFET) Vertex Detector for SuperBelle

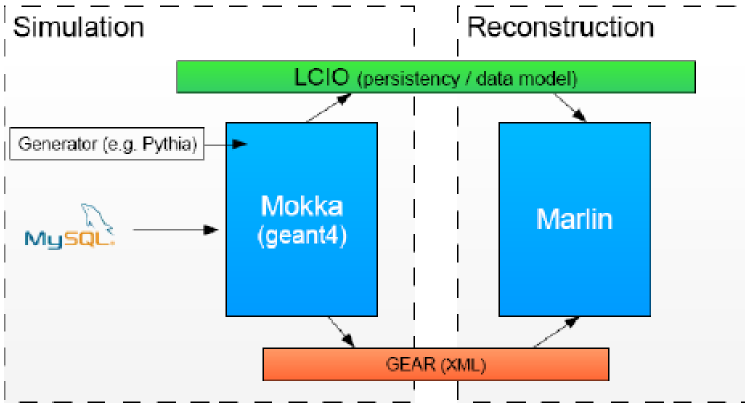


Contents:
- Software framework
- Simulation of the sensor response
- Validation of the simulation with data from beam tests
- Evaluation of the physics performance assuming SBelle geometry

Ariane Frey, Max-Planck-Institut für Physik München

ILC Software Framework

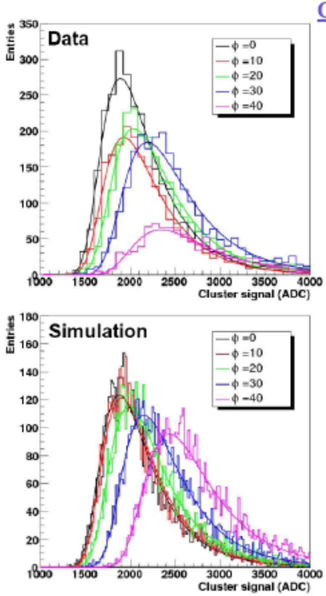
Based on LDC software:

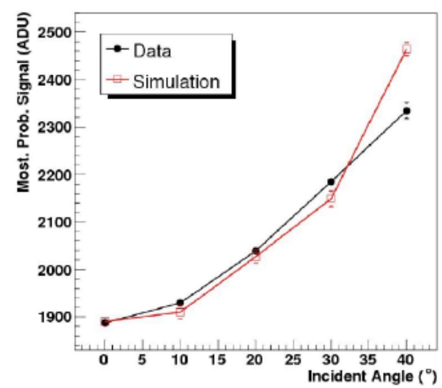


Mokka is geant4 based framework for full detector simulation
LCIO is a persistency framework that defines a common data model
Marlin is modular C++ application framework based on LCIO
GEAR: one source of geometry. Mokka creates geometry xml files u

Validation with Test Beam Data

Cluster Signal





Good agreement of test beam data and simulation

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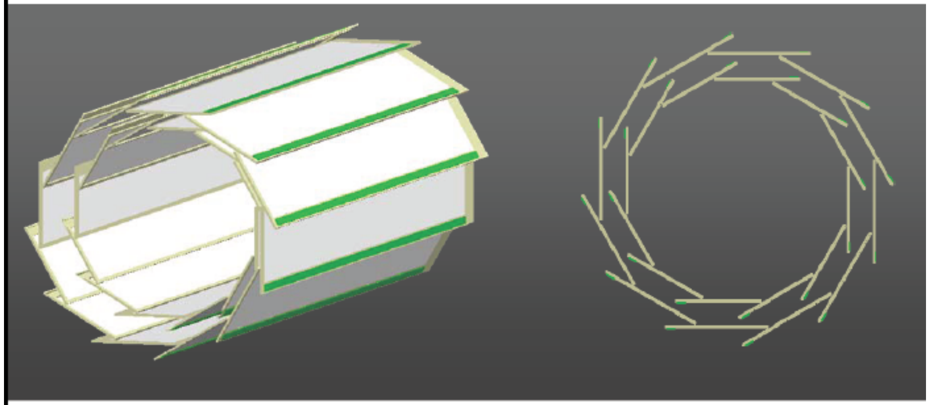
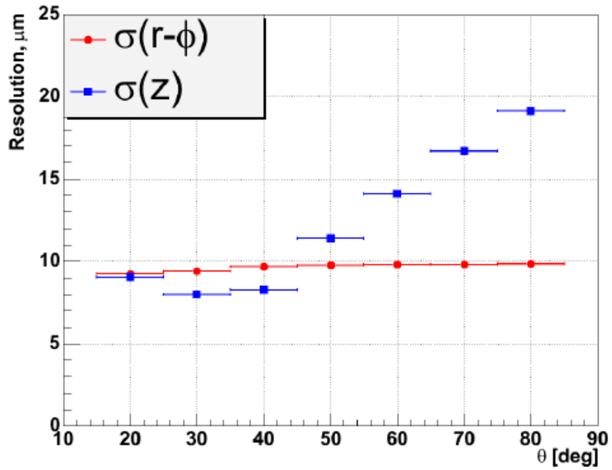
Pixel Simulations (A. Frey, Munich)

Initial Study of SBelle LoI Layout with DEPFETs

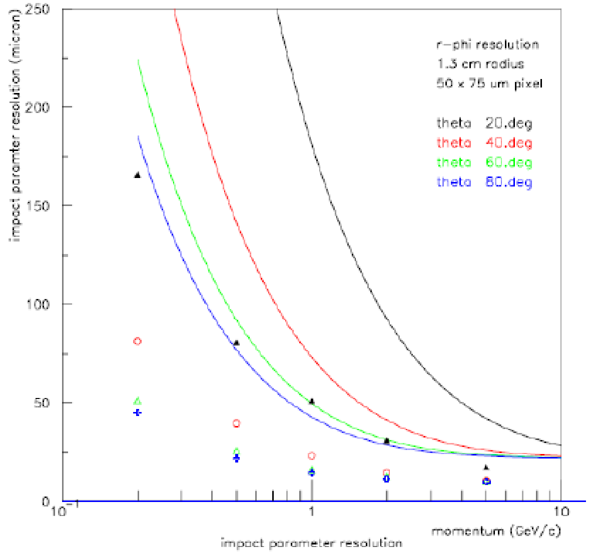


done by **Alexei Raspereza**

Single muon tracks with 5 GeV/c



Performance: Impact parameter resolution



Solid lines: Belles SVD2, symbols: DEPFET sBelle

- We used the ILC software framework for SuperBelle Vertex Detector performance studies
- ILC software can be easily adopted to other detector geometries
- Digitization, Tracking and Pattern recognition in VXD detector developed at MPI
- Software has been validated by test beam data
- Optimization studies on-going.
- We need background samples to estimate occupancy, fake track rates
- Outer layers simulated as pixels, need to implement realistic strip detector design.

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Super KEKB Quest for BSM

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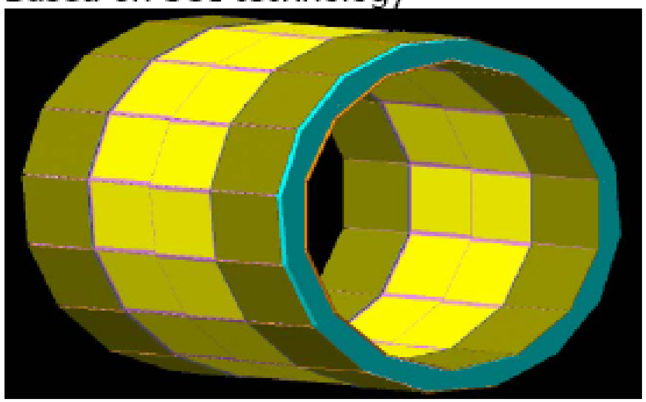
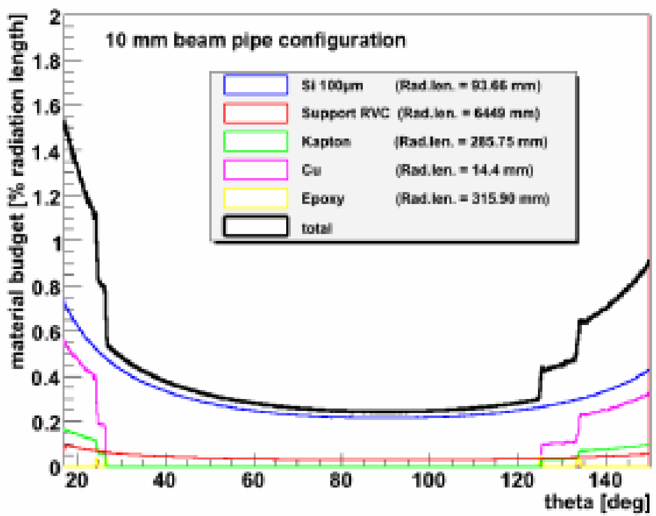
Pixel Simulations (A. Frey, Munich)

Simulation work at U Hawaii

H. Hoedelmoser et al.

Based on SOI technology





Stand-alone Geant4 Simulation of a Pixel Detector for the SuperKEKB Vertex Detector

H. Hoedlmoser, G. Varner, M. Rosen

University of Hawaii at Manoa

SuperBelle Note sBN/0006

June 20, 2008

Abstract

This note is the documentation of a stand-alone Geant4 simulation of a double layer of pixel detectors for the vertex detector of SuperKEKB. The model for the pixel detector was based on a binary SOI pixel detector, which is one of the candidate technologies for the pixel detector of an upgraded vertex detector. The model includes the pixel dies with sensitive and insensitive volumes, a support structure and cabling, all in two different configurations corresponding to two different beam-pipe radii. In the first part of the document all the relevant parts of the simulation from material and geometry definitions to digitization and event clustering are described. In the final part of the note results from the simulation are given, including material budget, cluster size distributions, layer efficiencies and intrinsic resolution.

Studies of 15mm and 10 mm beam pipe radius configuration

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Super KEKB
Quest for BSM

DEPFET Technology (A. Andricek, Munich)

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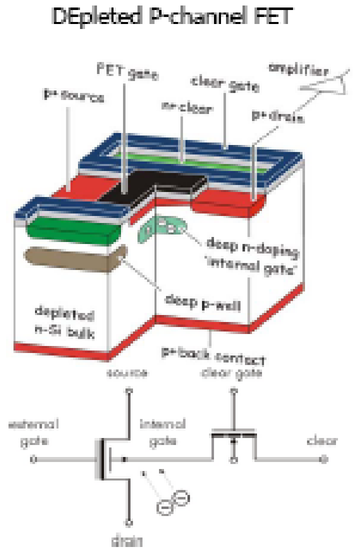
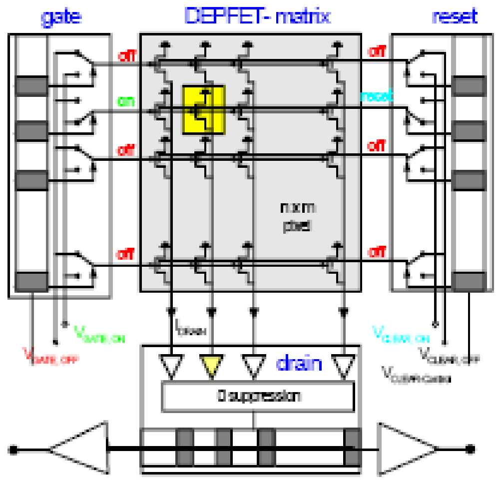
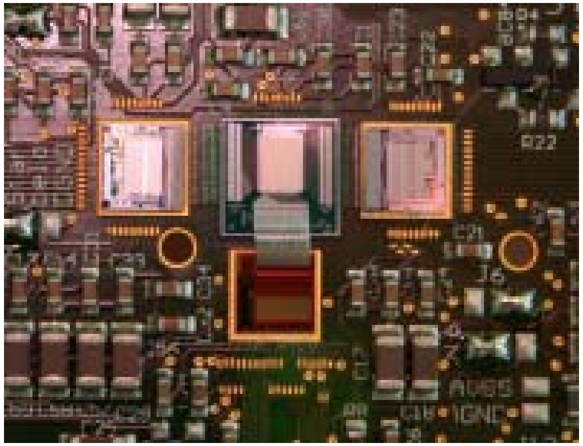
DEPFET Technology
(A. Andricek, Munich)







- fully depleted sensitive volume, charge collection by drift
- internal amplification → q-I conversion: 0.5 nA/e, scales with gate length and bias current
- Charge collection in "off" state, read out on demand

DEPFETs for the ILC VXD

- ✓ Prototype System with DEPFETs (450μm), CURO and Switcher
- ✓ test beams @ CERN:
  - ✓ S/N≈110 @ 450 μm
  - ✓ sample-clear-sample 320 ns
  - ✓ s.p. res. with 24 μm pixels: 1.3 μm @ 450 μm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 μm ... ~100 μm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2

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DEPFET Technology (A. Andricek, Munich)

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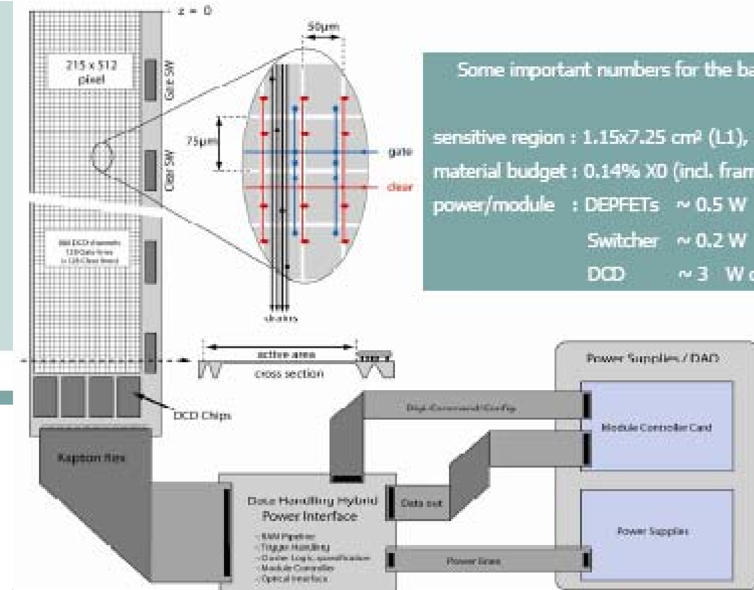
In this talk:

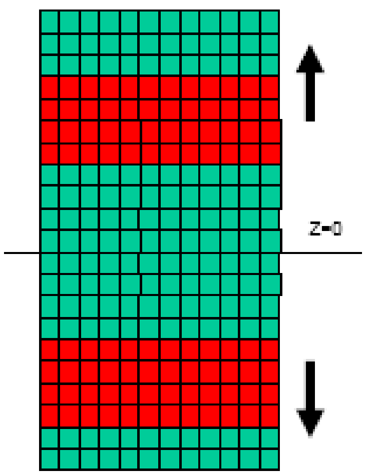
- Towards SuperBelle...
- New irradiation of DEPFETs to higher TIDs
- Update on thinning/ladder R&D



Some important numbers for the baseline layout:

sensitive region : 1.15x7.25 cm² (L1), 1.15x9.26 cm² (L2)
material budget : 0.14% X0 (incl. frame, chips, bumps)
power/module : DEPFETs ~ 0.5 W
Switcher ~ 0.2 W
DCD ~ 3 W on each ladder end

-: For pixels of >50 µm there is enough space to add more readout lines per row:
-: Parallelization adds more r/o channels but increases frame rate by the same factor
-: ILC: two-fold → SuperKEKB: four-fold readout



option (r-phi x z)	25 x 25 mm² (2fold)	50 x 75 mm² (2fold)	50 x 75 mm² (4fold)
Frame time	57 µs	19 µs	9.5 µs
occupancy	1.4% (?)	2.8%	1.4%
Data rate moule end	6 Gb/s	2 Gb/s	1 Gb/s

Assuming 0.4 hits/mm²/s background and 12.5 MHz row rate

Data rate per end, 10kHz Trigger rate, 0-suppression,~ 4 pixels/hit, 32 bits per pixel including address

Disadvantage: ~1% inefficienciency

DEPFET Technology (A. Andricek, Munich)

ASICs: DCD and Switcher are deep submicron technologies → rad. hard beyond 10Mrad (with the appropriate design)

DEPFETs: Not that easy ... ☹ ...

noise performance seems to be okay up to 8 Mrad

threshold shift could be compensated by re-adjustment of the Switcher voltages

ΔV_t variation at higher TID (reason for this under investigation) and hence

ΔI_D at a given V_{Gate} has to be compensated by the DCD → slightly higher noise of the f/e

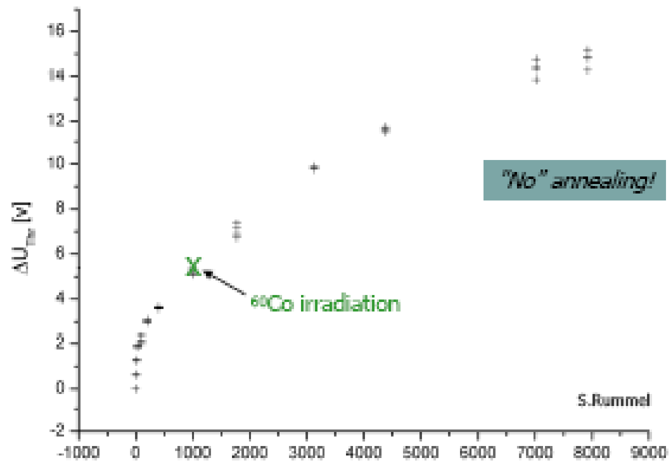
technological counter measures: thinner gate oxide reduces $|\Delta Vt|$

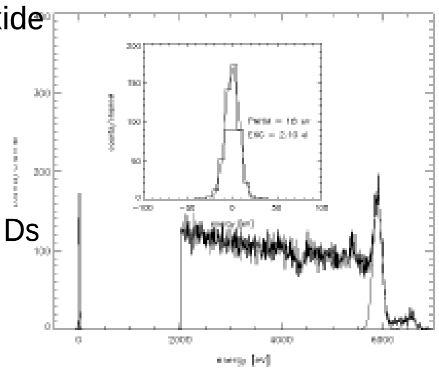
further optimization of the gate dielectrics

In conclusion: The DEPFET gets worse at high TIDs (8Mrad).

Probably ok for several years of running

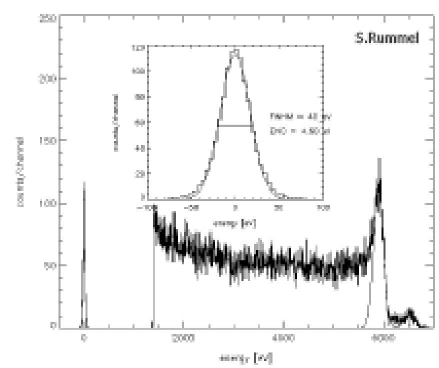
-: PXD5, Wafer 90, 8x12 mini-matrix, 24x24 μm²
-: irradiation with 10keV X-ray photons in Karlsruhe, ~150krad/h
-: entire matrix biased in "off" during irradiation, periodically cleared
-: four pixels selected to measure basic characteristics throughout irradiation





non-irradiated
V_{thresh}=-0.2V
time cont. shaping τ=10 μs

Noise ENC=2.1 e⁻ (rms) at T>23 degC



7.9 Mrad, 10keV X-rays
V_{thresh}=-13.0V,
time cont. shaping τ=10 μs

Noise ENC=4.6 e⁻ (rms) at T>23 degC

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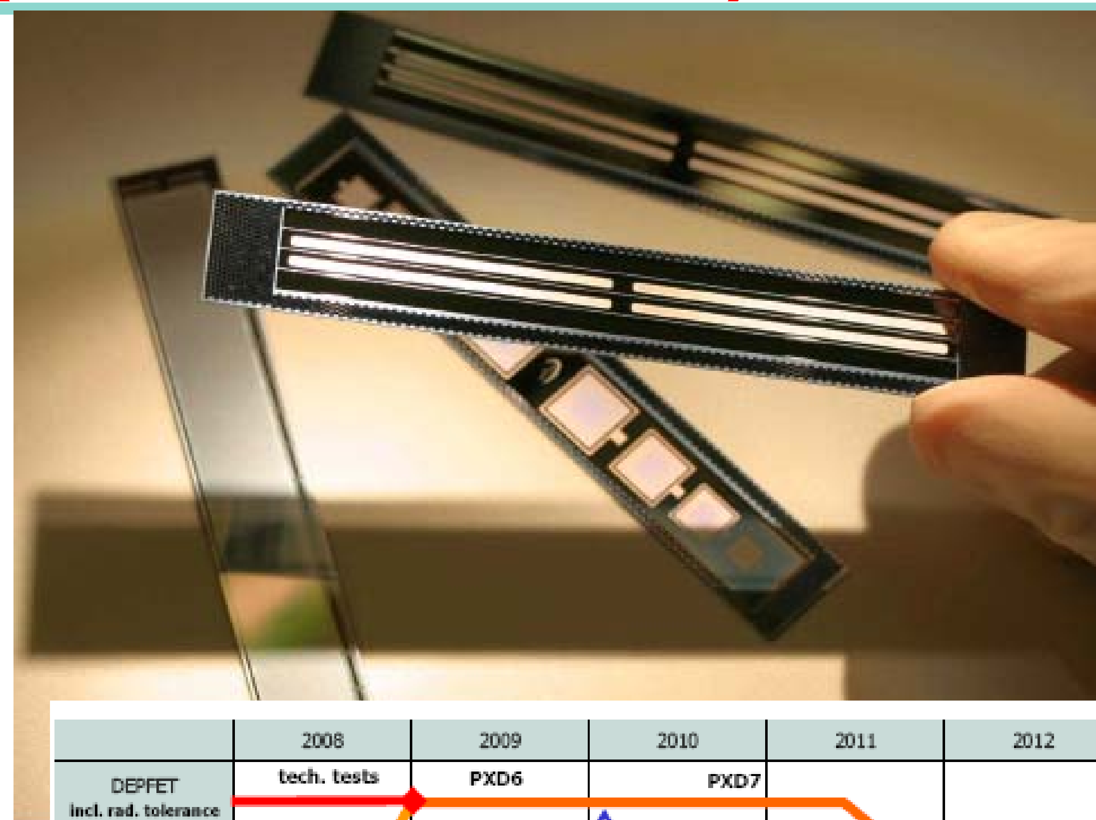
DEPFET Technology (A. Andricek, Munich)

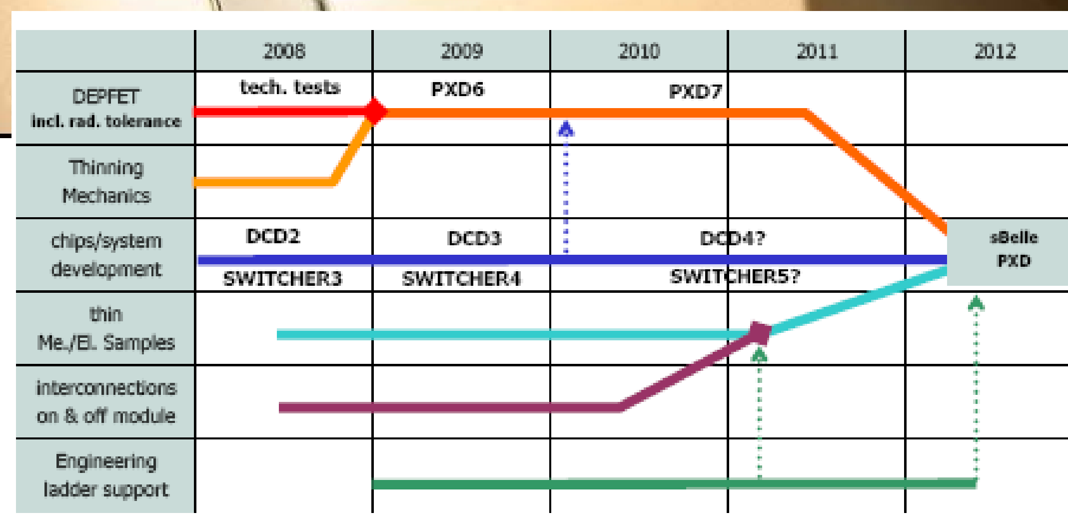
Thinning technology established
50 µm + frame
All silicon
~0.14% X_0 (average)

Collaboration forming

First superBelle prototypes 2010 (PXD5)

Schedule to build complete detector till 2013





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SOI Technology
(T. Tsuboyama, KEK)

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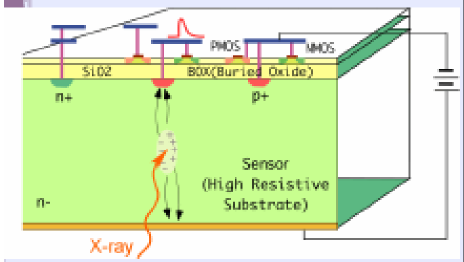
SOI Technology
(T. Tsuboyama, KEK)

SOI pixel sensor

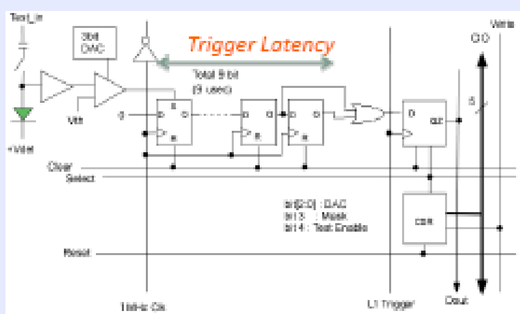
- The charge induced by radiation in the silicon wafer is processed by CMOS circuit above the buried oxide (BOX).

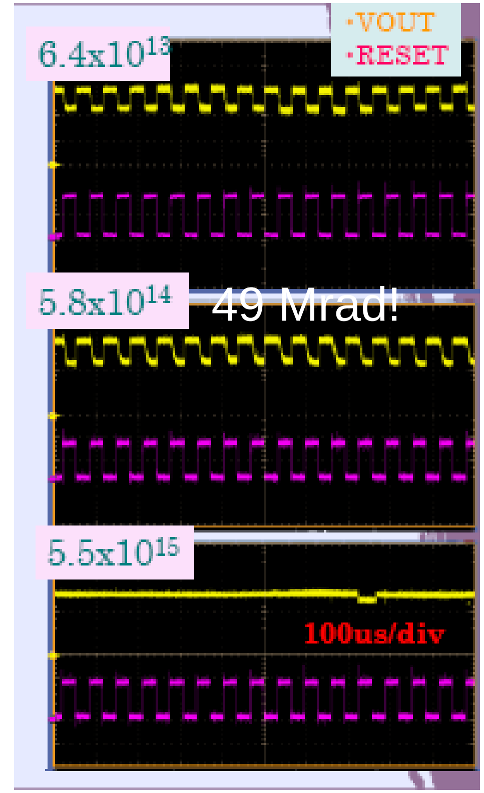


Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz, 700 Ω-cm (n-type), 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).

Belle PIXEL prototype

- A prototype pixel sensor for the Belle SVD upgrade was submitted in Dec 2007.
  - Continuous sampling + comparator + digital pipeline.
  - Implemented in 60x60 μm² cell.
  - More room to shrink the pixel size.





Typical problem: Back gate effect
Chip submitted, still waiting

Similar project by Hawaii (same submission)

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fuer Physik

CMOS Technology (G. Varner, Hawaii)

"2nd Open meeting for the proto-collaboration Joint IR/PXD/SVD session "

Friday 04 July 2008
from 08:30 to 12:30
at 3 go-kan Seminar Hall

Friday 04 July 2008 |

Friday 04 July 2008

top

08:30->*12:30* **Joint IR/PXD/SVD session** (Location: 3 go-kan Seminar Hall)

08:30	Self introductions (10')	Everyone, 30 seconds
08:40	IR (Interaction region), detector-machine interface, beam pipe (20') (Slides)	M. Iwasaki
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09:25	Overview on pixel layer requirements (20') (Slides)	G. Varner
09:45	Pixel simulations, backgrounds (15')	A. Frey
10:00	Overview of pixel detector based on DEPFET and common issues: expected performance, backgrounds (20')	L. Andricek
10:20	Coffee break	
10:30	SOI (10')	T. Tsuboyama
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12:00	Schedule and Milestones (10')	T. Tsuboyama for Z. Natkaniec
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$\Delta p \cdot \Delta q \geq \frac{1}{2}\hbar$

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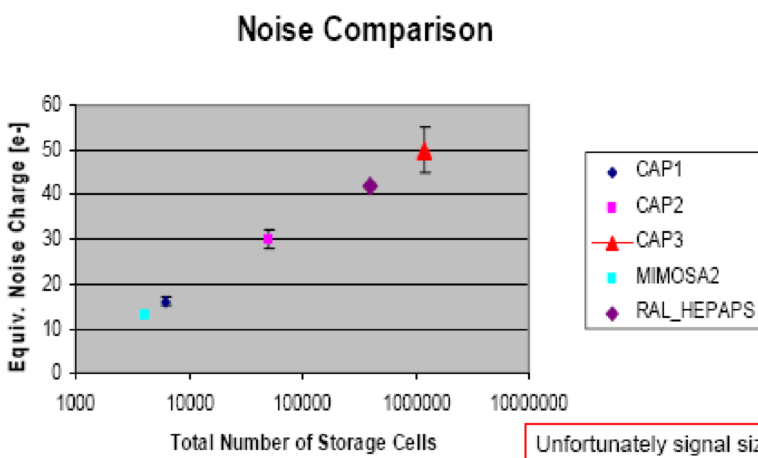
Critical R&D Scorecard

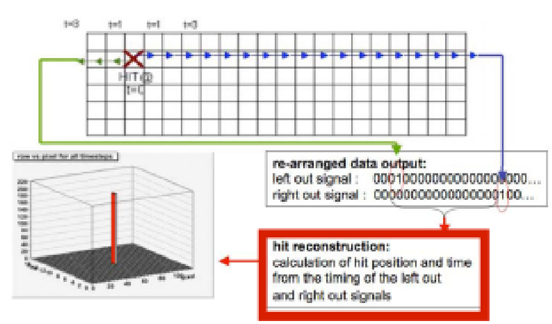
1. Readout Speed — 100kHz frame rate, 10kHz L2 accept
   - CAP3 too slow, SNR concerns
2. Radiation Hardness — >= 20MRad
   - Leakage current OK (CAP2) for short integration time
3. Thin Detector — <= 50μm, layer
   - 50μm LBL test bench, thinning at APTEK (same SNR)
4. Full-sized detector — Span acceptance (reticle limit)
   - CAP3 large acceptance biasing/uniformity



Unfortunately signal size Fixed and small

hit reconstruction for a binary detector with time encoding

you are familiar with this:



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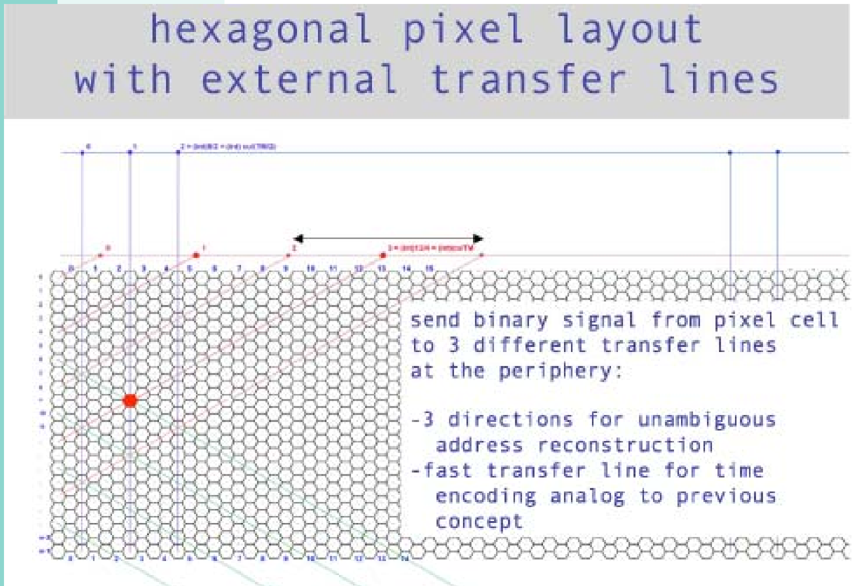

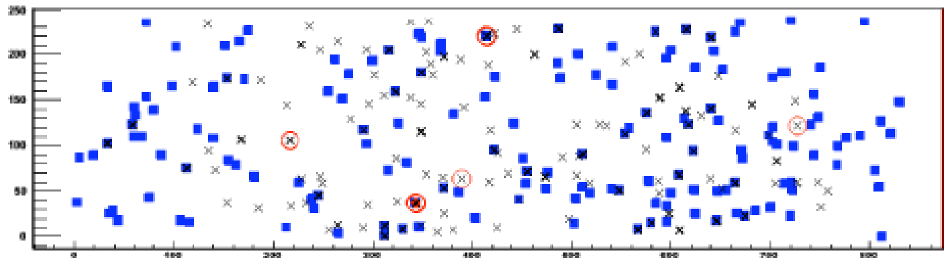

■ background
● seeded hit
x all reconsructed hits in time window
○ reconstructed @ t_{trig}

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- Need to demonstrate binary can work
  - SNR is still an issue
  - SOI variant probably more realistic
    - Next OKI submission
    - TSMC 0.35um opto submission end of July
  - Issues of cross-talk, threshold dispersion
- Binary has possible benefit
  - Reduced data size
  - Intrinsic Resolution degradation not critical
  - Original benefit of commercial CMOS MAPS

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Data Rate & DAQ
(C. Lacasta, Valencia)

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Super KEKB Quest for BSM

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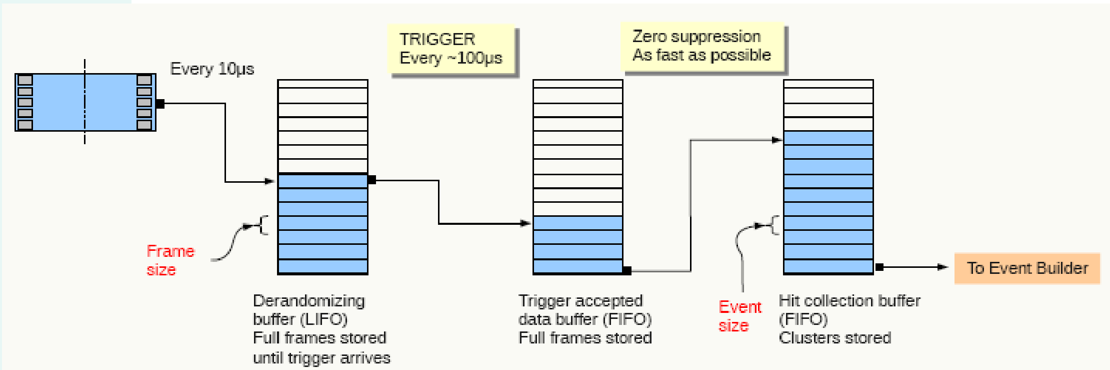

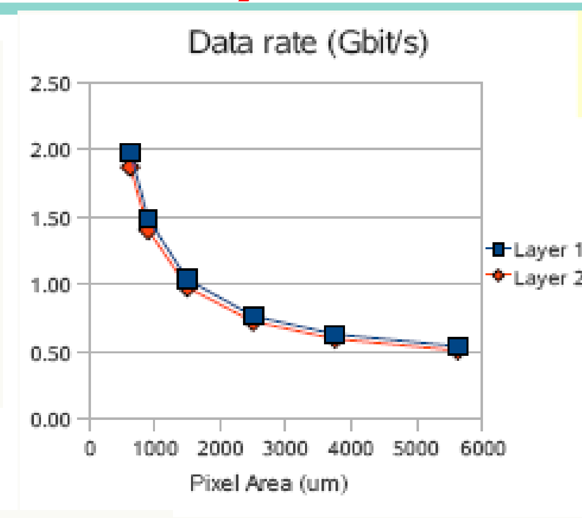

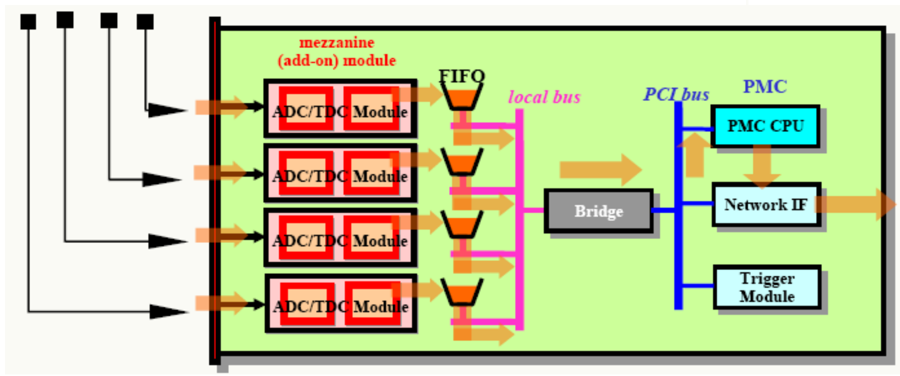

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- ✔ Each input has, in the best case, ~
- ✔ Local bus 4x more
- ✔ PCI bus can handle at most 133 M
- ✔ A serious bottleneck...

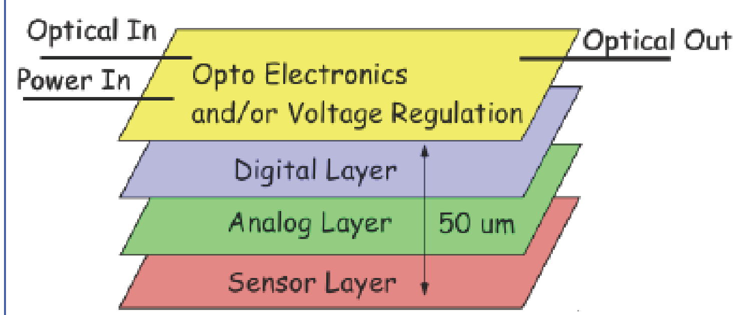
Possible remedies: Further data reduction on Finesse boards
- ➔ Smart coding of address information in the cluster
- ➔ Level II trigger rejection
  - We need access to that information
- ➔ ROI (Regions of interest)
  - Needs higher level information
- ➔ Smart algorithms to reject background based on
  - Pulse height
  - Cluster size
  - ...

New Technologies: 3D

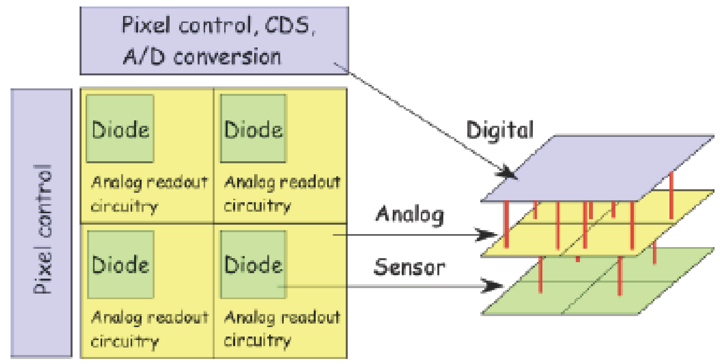
Ron Lipton (Plenary)

3D Electronics

- 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a “monolithic” circuit.
  - Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- Utilizes technology developed for Silicon-on-Insulator devices
- This is a major direction for the semiconductor industry.



Physicist's Dream



Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

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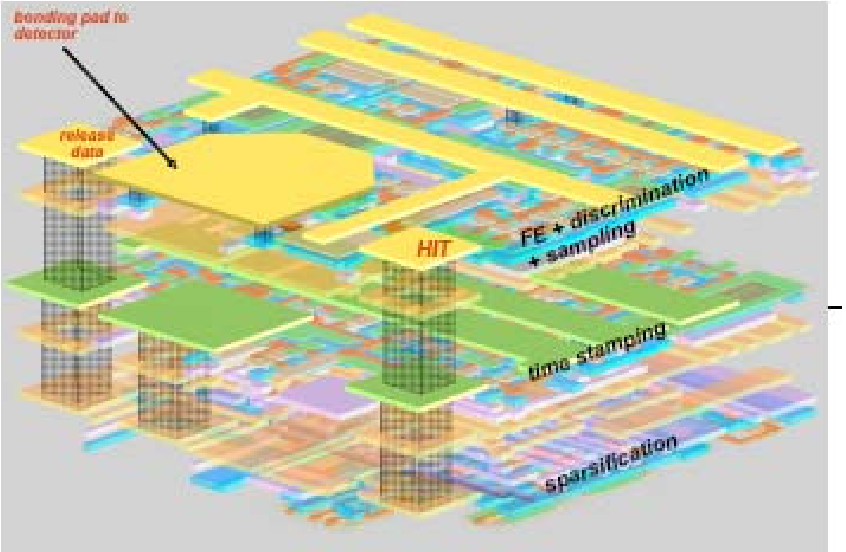
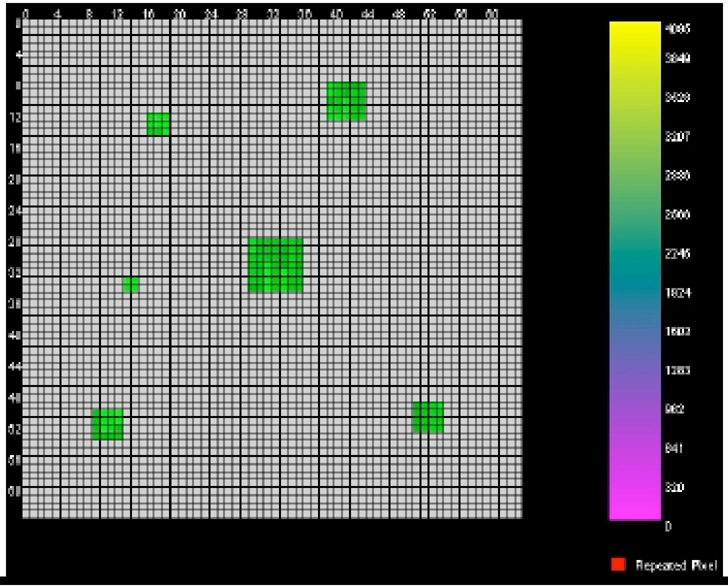
New Technologies: 3D

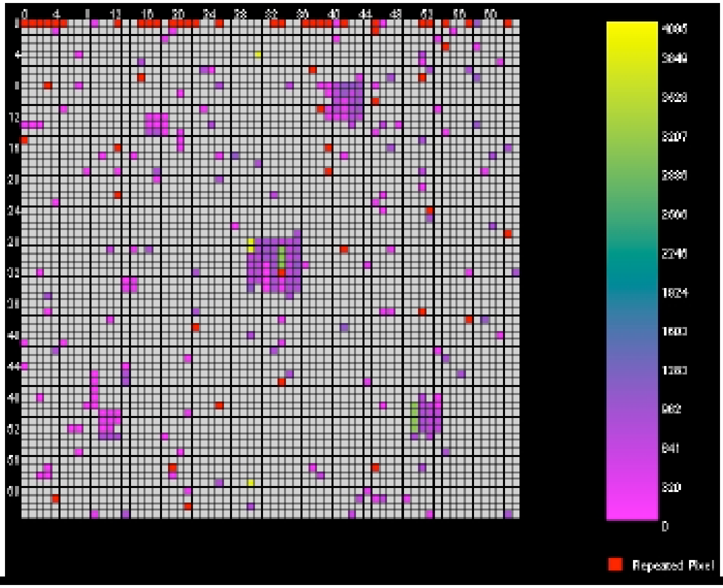
Ron Lipton (Plenary)

Test run with MIT:
VIP chip: 3 layer, no sensor
Low yield, many problems
⇒Proof of principle!
Continue with Tezzaron/Ziptonix

⇒Powerful technology
Time stamp
ΔT = 300 ns: 1/33 reduction of Occupancy!







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Conclusions

Pixel Detector for SuperBelle should:

allow robust vertexing at high background
improve performance with respect to SVD2

=> fast readout (or time stamp), thin

Technologies:

DEPFET
SOI
CMOS-MAPS
3D-technologie

Aiming for installation in 2013 the DEPFET option seems to be the most realisitc (ok for running ~years at initial luminosity)
=> Tight schedule: start now!

For final luminosity: consider ALL options

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