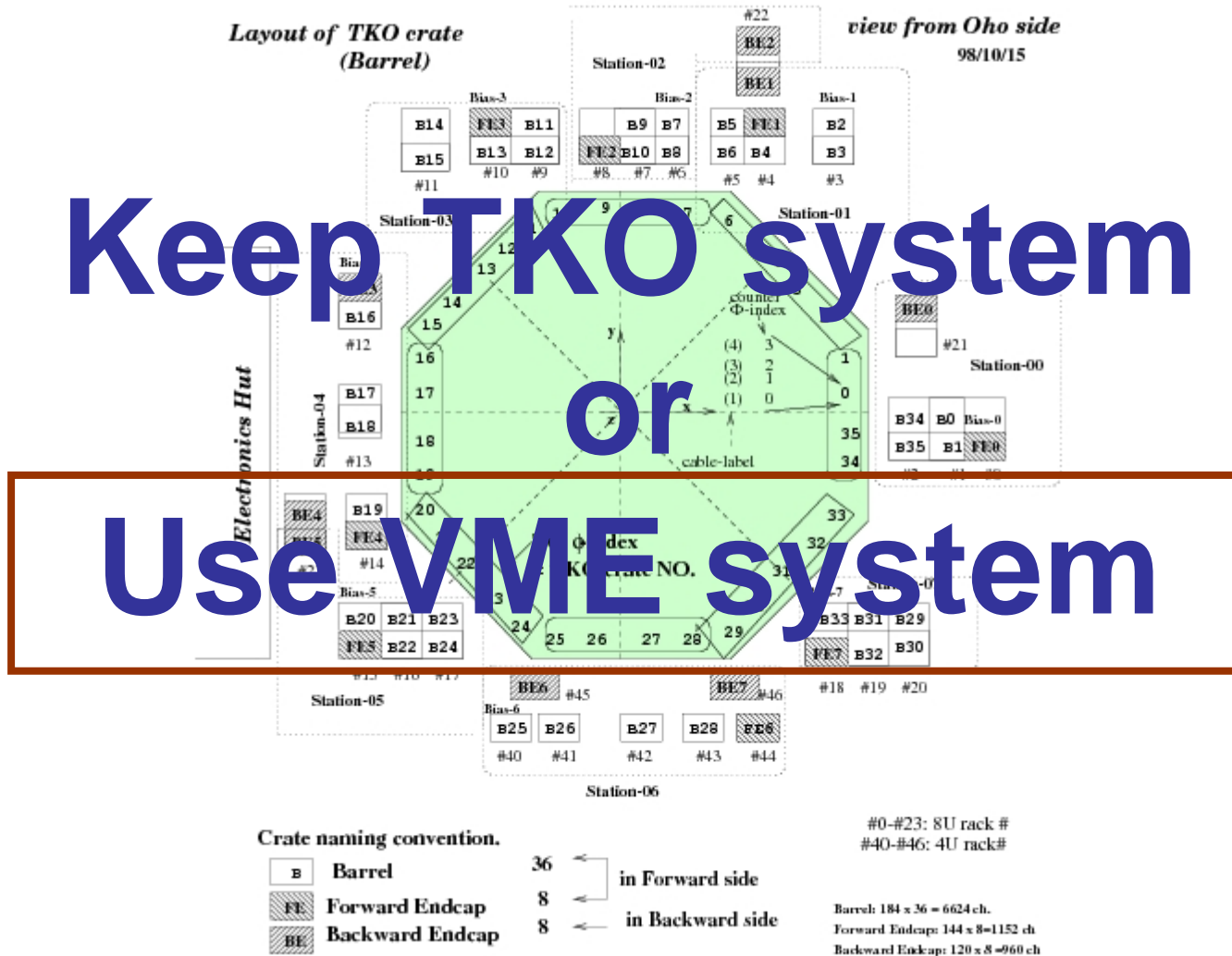


Calorimeter Trigger for sBelle

ByungGu Cheon
(Hanyang Univ)

Super Belle Meeting, July 3-4, KEK

52 TKO crates



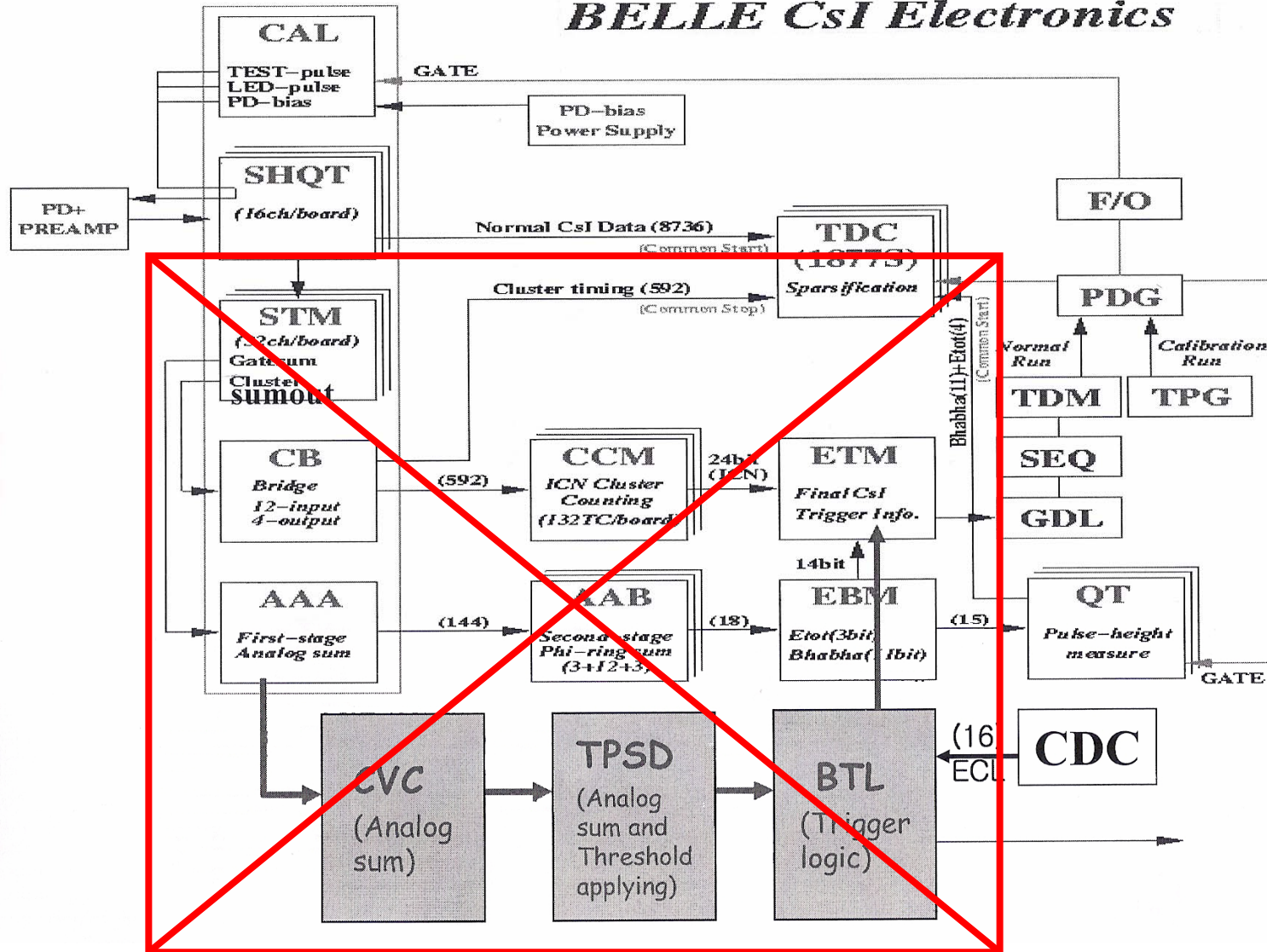
Option Conservative → Official scheme

I. Nakamura

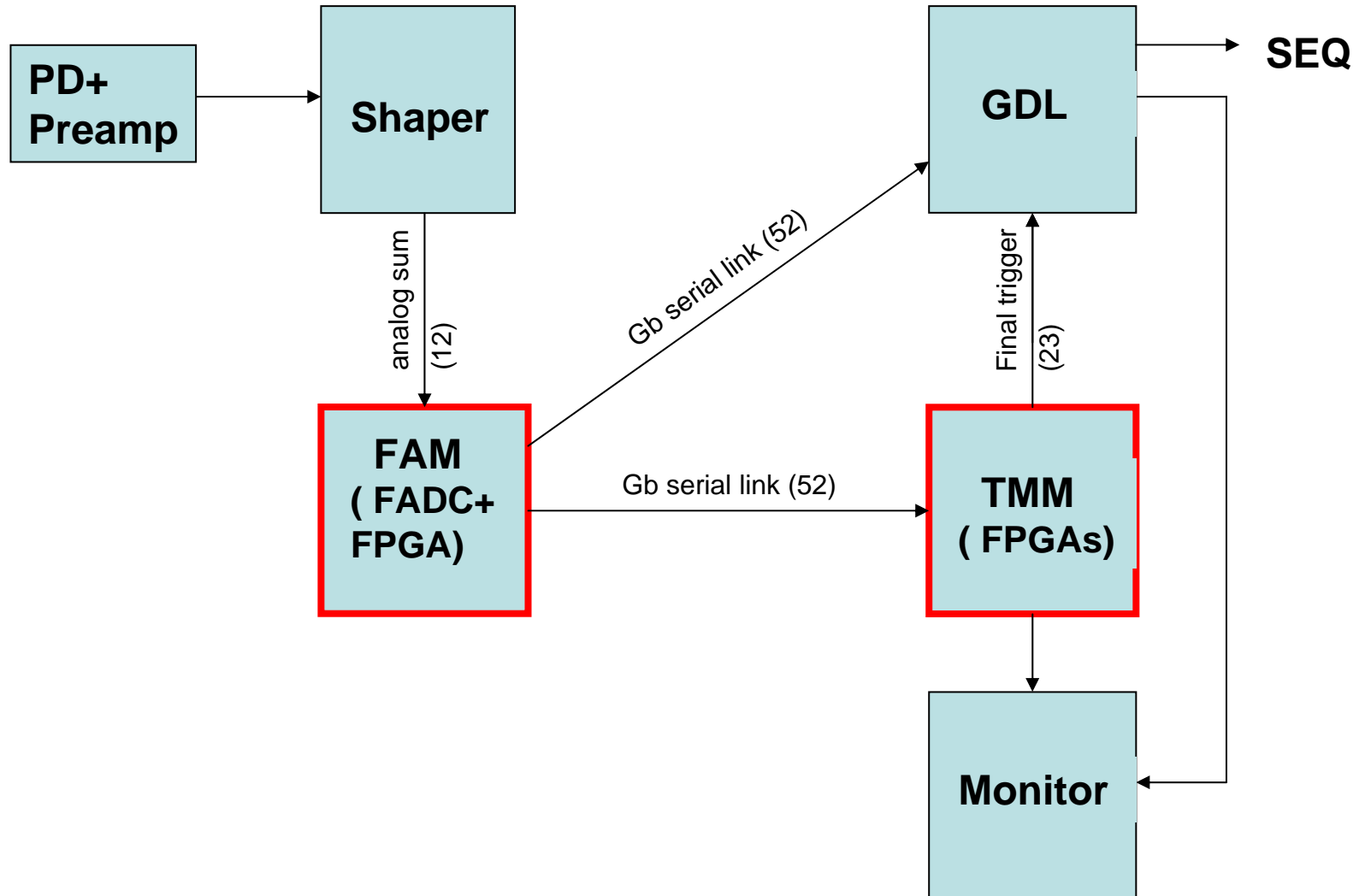
- ❑ One VME crate
- ❑ Shaper Digitizer Board (8–12 boards/crate)
 - 16 channel input
 - One additional input for test pulse
 - One digital output with current cable
 - One trigger sum output to FAM
- ❑ Flash ADC Trigger Module
 - upto 12 input from digitizer board
- ❑ Calibration Module
- ❑ Controller (CPU) board

Belle ECL Electronics

BELLE CsI Electronics



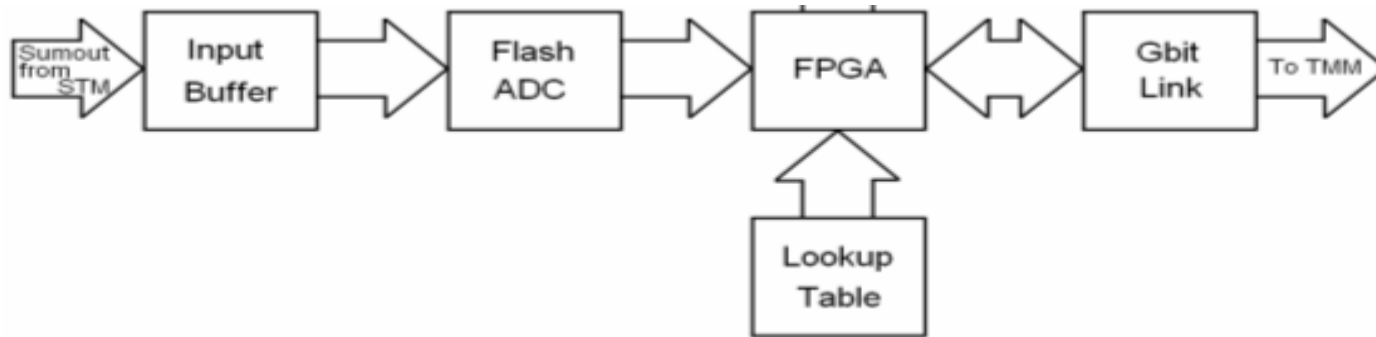
sBelle ECL trigger electronics



Advantage of FAM + TMM scheme

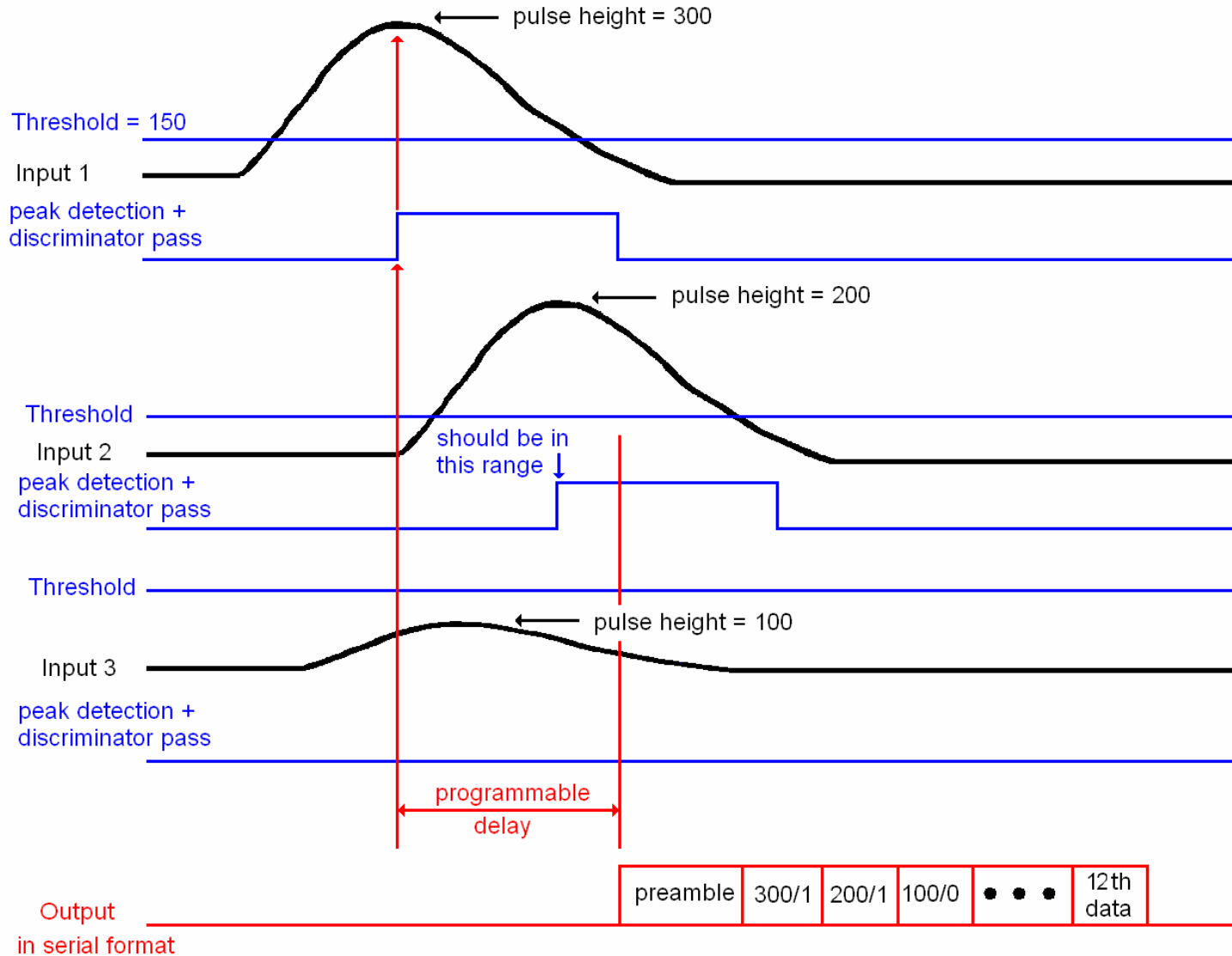
- Electronics chain will be very simple.
- More flexible trigger design (because we have waveform information).
- Reduction of cable; lots of bulky copper cables → 52 optical fibers
- Simple monitoring scheme (extra QT & TDCs are not necessary)
- Easy handling of CsI(Tl) and pure-CsI together

Flash ADC Module (FAM)



- Input : 12 TC(4x4Xtlas) analog sum signals from Shapers
- Continuous Input signal digitization @ 100MS/s 10~12bit
- Find a pulse peak value or a partial sum of rising signal region
- Digital discrimination of pulse height (programmable)
- Output : 12 TC pulse height (or partial sum) + discriminator bit via Gbit link (with 10ns timing resolution)
- TC output gain variation adjustment using look-up-table
- One board(12 TC channels) / VME crate
- Xtal gain adjustment should(may?) be done at Shaper.

How FAM works



Trigger & Monitoring Module (TMM)

- Input : 52 x 12 TC signals from FAM modules
 - 7 FPGAs + VME interface
 - If all parts are not fitted into one board, partitioning & cascading design will be taken into account.
 - Output : 23 ECL final trigger signals
 - 4 ECL trigger timings (Final, Fwd, Barrel, Bwd)
 - 3 Total Energy (>0.5, 1.0, 3.0 GeV)
 - 4 Isolated Cluster Number (3 bits + 1 carry-bit)
 - 11 types of Bhabha triggers
 - 1 Cosmic Veto
- ** Any more useful trigger algorithm will be studied.

Timing Latency

- Peaking time=**700ns** @ peak position of analog sum signal
- ADC pipeline latency @ FAM = **~100ns**
- Peak finding process @FAM = **100 ~ 200ns**
- Programmable delay @ FAM = **~300ns**
- Gbit transfer(~200bit) = **~200ns**
- Optical cable length(40~60m) = **200 ~ 300ns**
- 52 Trigger input alignment @ TMM = **~100ns**
- Trigger decision @ TMM = **100 ~ 200ns**

Total latency = **1800 ~ 2100ns**

FAM key algorithm test

New EBM

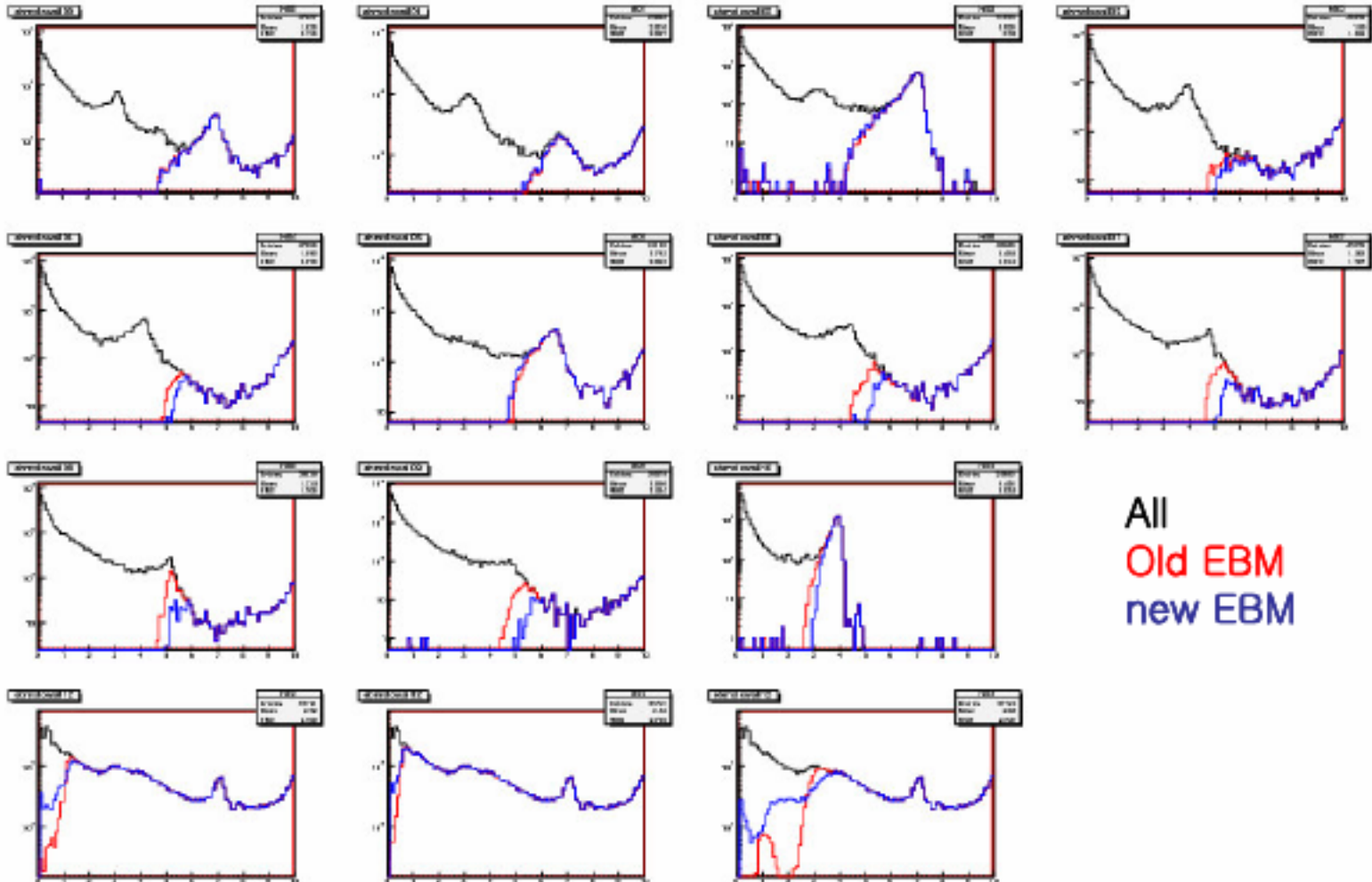
M.J.Lee

- New EBM is not just a replacement of old EBM
 - It uses digitization of incoming signal and FPGA processing for discrimination & peak searching
- We installed new EBM test bench
 - This test bench is also aiming possible test for sBelle



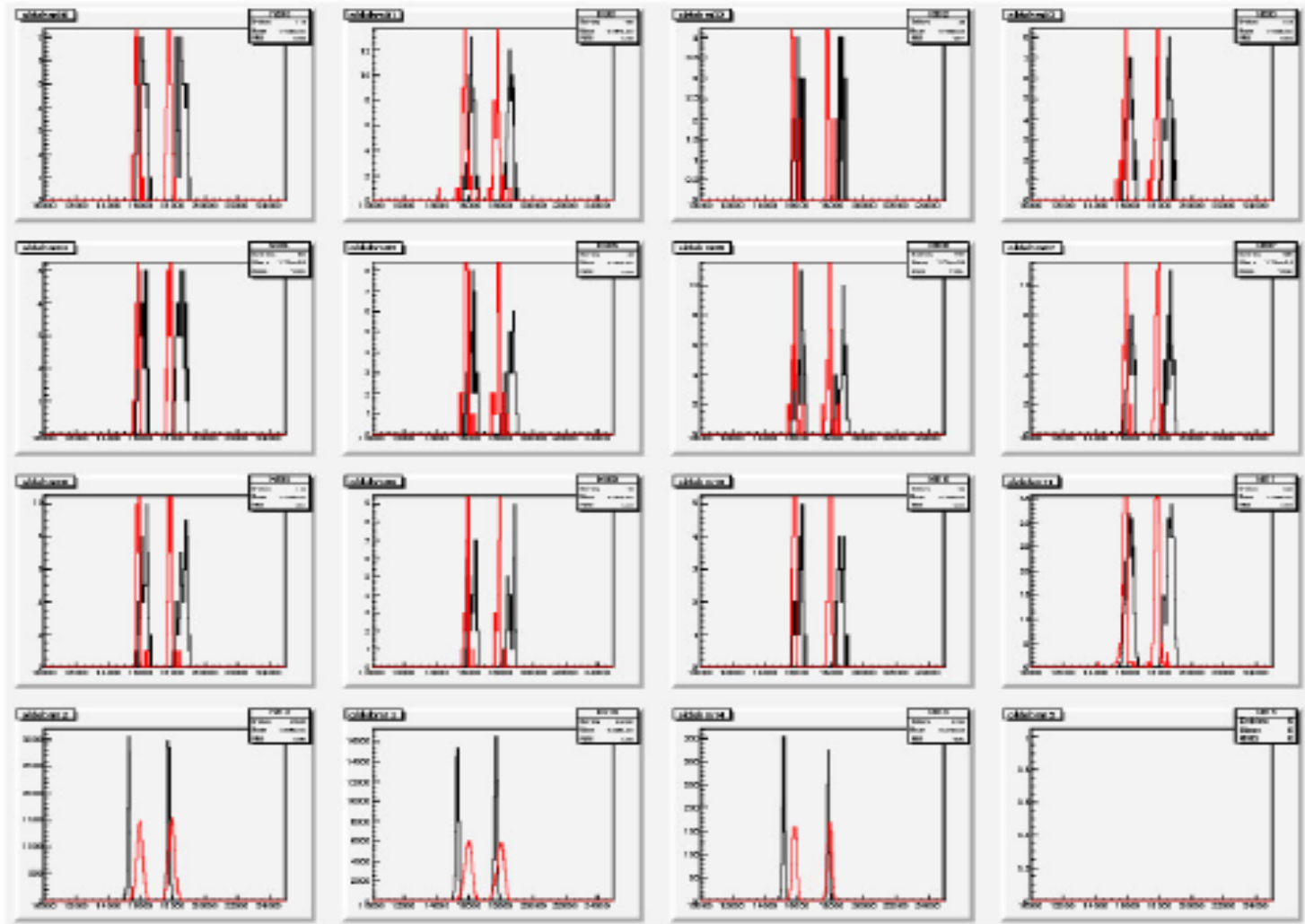
Bhabha, Etot Calibration

M.J.Lee



Bhabha, Etot Timing

M.J.Lee



How can we handle pure Csl signals together with Csl(TI) if we replace endcap Xtals ?

- Peaking time and pulse height difference btw Csl(TI) and pure Csl
- All the triggers will be problematic without any correction.
- Timing and pulse height correction of pure Csl can be done @ TMM.
- New FAM+TMM chain will generate all the trigger signals we provide now.

Manpower

- Hanyang Univ. : Y. Unno, S.H.Kim, I.S, Lee, B.G. Cheon (4)
- Seoul N. Univ. : M.J. Lee, S. Ryu, S.K. Kim (3)
- BINP : Y. Usov (1)
- Notice co. : S.Y. Kim (1)

Summary

- FAM core firmware algorithm will be studied using new EBM.
- We will start designing FAM if VME type Shaper design is ready.
- Trigger algorithm will be studied with sBelle trigger simulator.
- We have investigated the possibility of producing Shaper in Korea.

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