Shaper-digitizer design.
July 04, 2008
Yu.Usov

Outline:

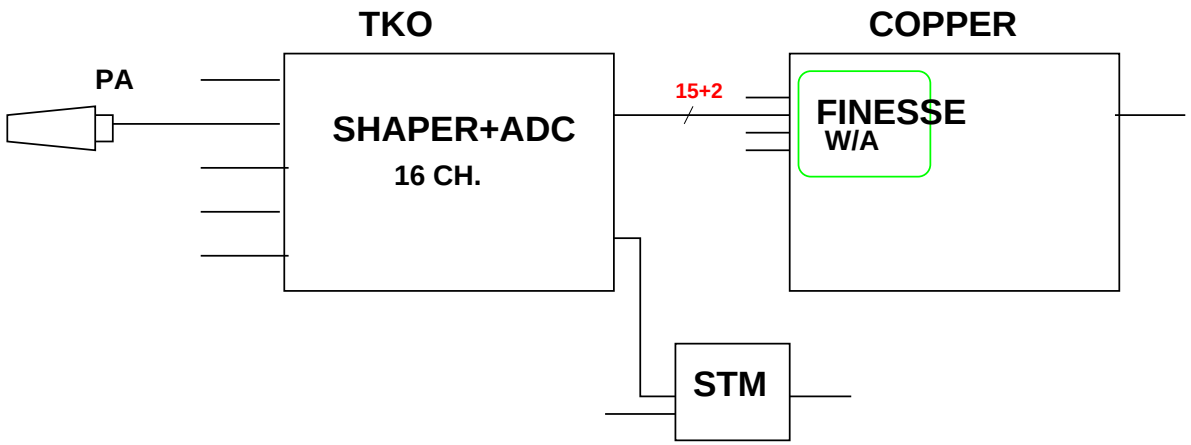
- Change of the DAQ aproach
- Change of the Shaper-digitizer design
- Current status

Change of the DAQ aproach

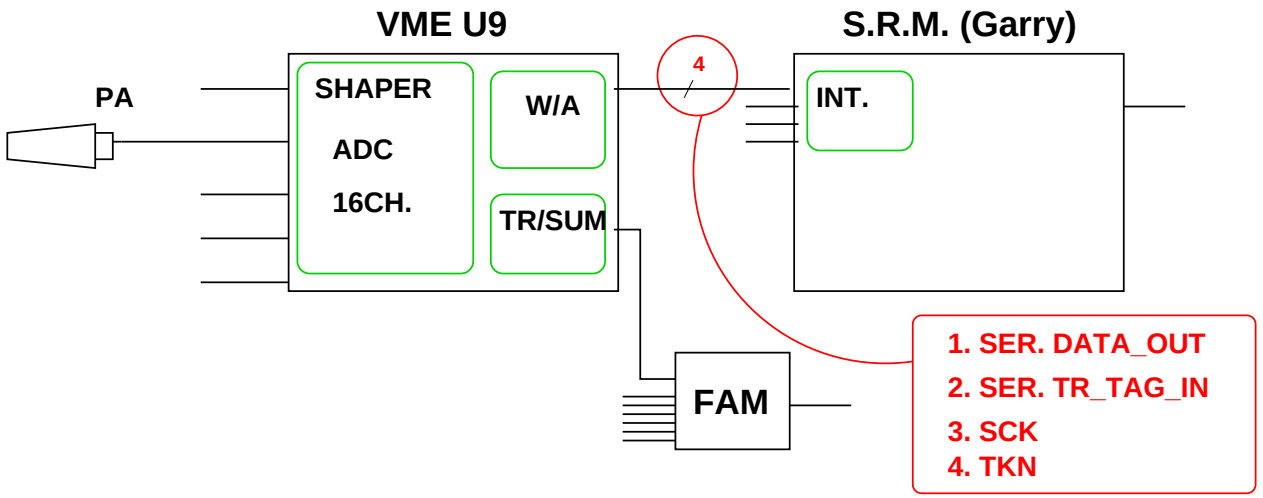
- **Taking into account the necessity of the long time of the further work of the shaper digitizer modules, it was decided to refuse from the TKOand pass to the VME format.**
- **The sizes of the module are equal to: 430x318 and 367x400 for TKO and VME correspondently and as a result, the area of the printed-circuit-board increases for about 10%.**
- **DAQ suggested to change the electronics to the unified electronics basing on the Gary SRM.**
- **We decided to implement the functions of STM trigger module into shaper digitizer module.**
- **Put the WFA FPGA logic into the same module**

Change of the DAQ aproach

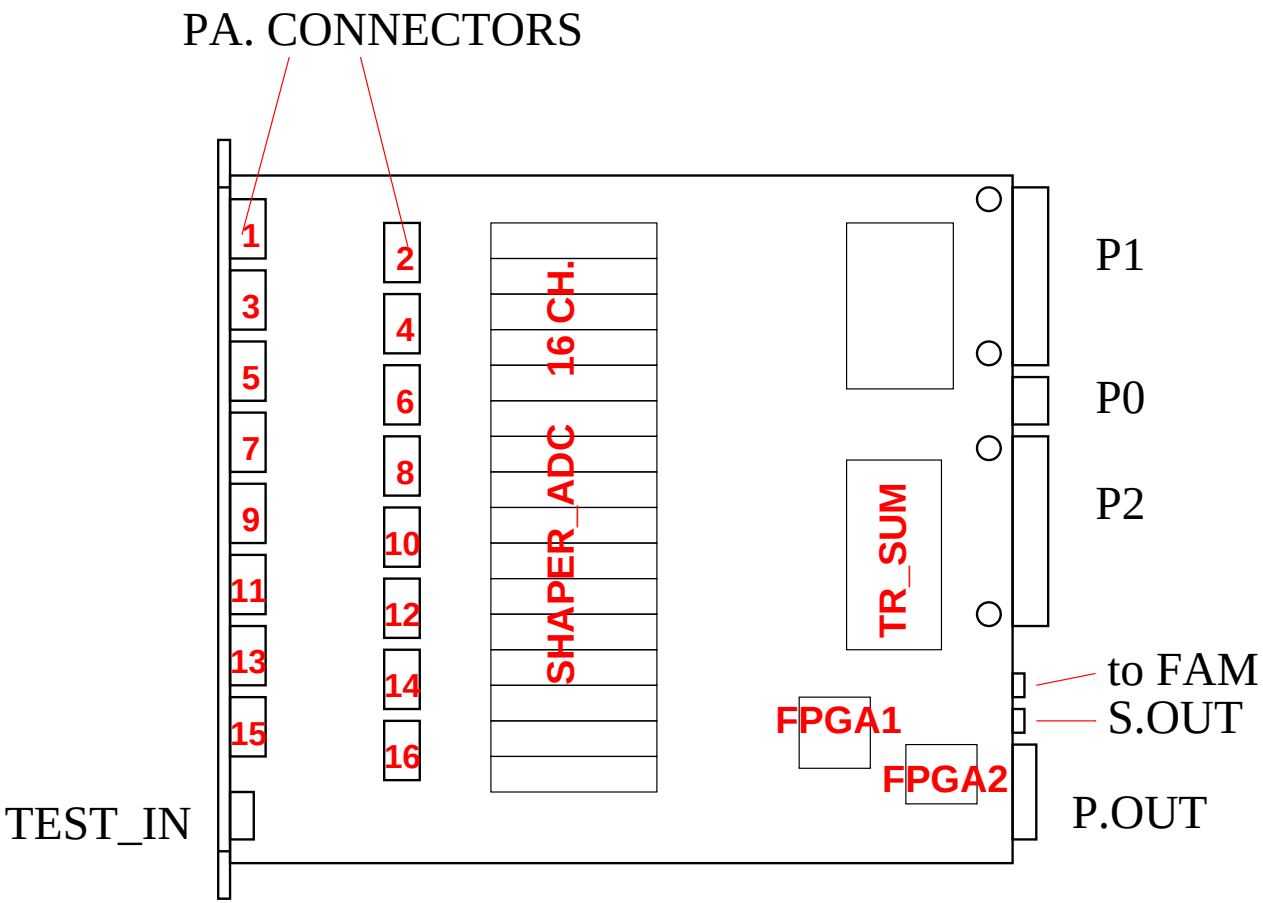
CARRENT VERSION



NEXT VERSION



New shaper digitizer module



VME U9 MODULE

New shaper digitizer module

- **The layout of the analog shaper digitizer part for each channel should be shrinked for about 10%.**
- **Add fast trigger sum module.**
- **Implement uploud function via data line.**
- **Implement the Wafe Form Analysis FPGA part into the module. (The part which was located on FINESSE)**
- **The data transfer from the shaper digitizer to unified collector module is performed via 4 pair CAT5 cable with 500 MHZ**
- **Special output of the analog trigger signal for FAM module is located on the back side.**
- **For voltage supply we'll probably need to use special voltages ($\pm 7.5 \sim 9$ V.**

New shaper digitizer module oder

- **To make the electronics production cheaper we plan produce it in Korea(about 1.5 times cheaper).**
- **The schematic diagram is almost ready.**
- **Within one week we plan to communicate with the production company (with help B.G.Cheon)**
- **We'll need at least one more iteration to have the final version.**
- **For test (without Garry module will not have been ready) the parallel output for ECL FINNESSE is implemented.**