ECL FINESSE status

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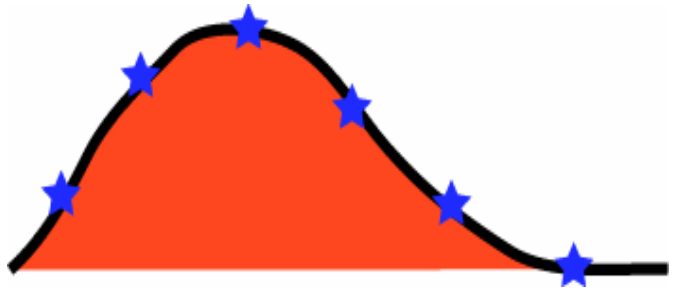
Algorithm details

$$\chi^2(A, p, t_0) = \sum_{i,j} (y_i - Af(t_i - t_0) - p) S_{ij}^{-1} (y_j - Af(t_j - t_0) - p) \to \min$$

$$S_{ij} = \overline{(y_i - \bar{y})(y_j - \bar{y})}$$

$f(t)$ – counter response



$$Af(t_i - t_1 - \Delta t) = Af(t_i - t_1) - A\Delta t f'(t_i - t_1) = Af(t_i - t_1) + Bf'(t_i - t_1)$$

where t_1 – initial time (trigger time)

$$\sum_{i,j} f_i S_{ij}^{-1} (y_j - Af_j - Bf'_j - p) = 0$$

$$\sum_{i,j} f'_i S_{ij}^{-1} (y_j - Af_j - Bf'_j - p) = 0$$

$$\sum_{i,j} S_{ij}^{-1} (y_j - Af_j - Bf'_j - p) = 0$$

$$\Rightarrow$$

$$A = \sum_i \alpha_i y_i$$

$$B = \sum_i \beta_i y_i \Rightarrow \Delta t = -B / A$$

$$p = \sum_i \gamma_i y_i$$

Reconstruction options

ADC data ➔ amplitude reconstruction is needed somewhere

1. In FINESSE
2. In COPPER
3. In event builder

Hardware data processing

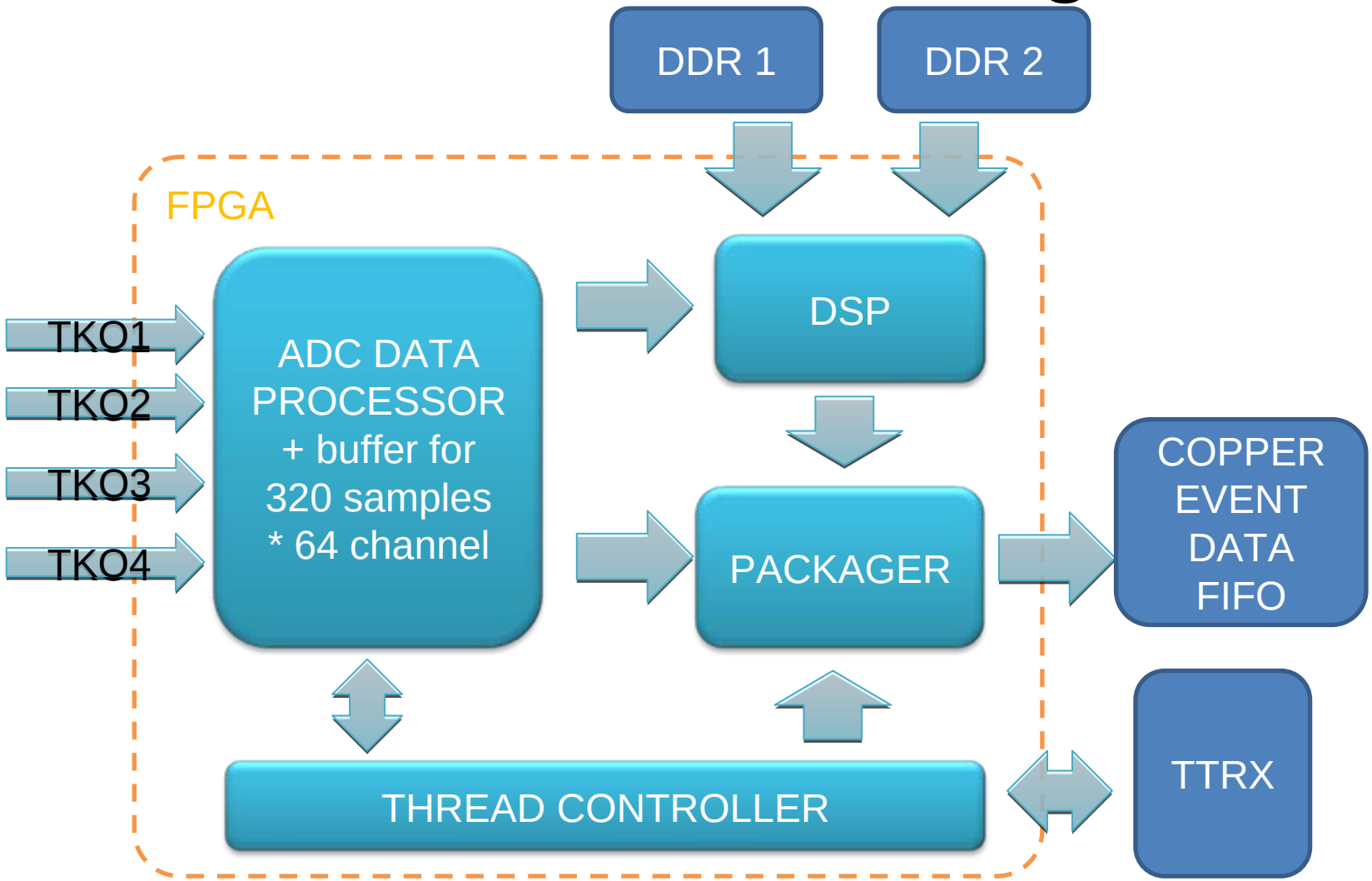
Advantages:

- Low data amount transferred from FINESSE to COPPER
- Low processing load of the COPPER CPU

Disadvantages:

- Inflexible realization – the algorithm must be strictly defined and intensively tested

FPGA overall design



Output data format

Contents	Comments
HEADER	Event info + info on following data included
DSP data	A, T, quality flag for hit channels. May be skipped
ADC	Up to 64 samples per any channel. May be skipped. A decimation is possible.
FOOTER	

Offset	Contents	Comments
0	FFAA0000	Header
1	b[7..0] – TTRX TAG b[31..24] – Event number	
2	b[4..0] – trigger time (0-23) b[7..6] – trigger source b[15..8] – dsp_num b[23..16] – raw_len b[31..24] – raw_num	0 <= trigger time <= 23 Trigger source: 0 – TTRX, 1 – TKO, 2 – LB dsp_num – number of hit channels raw_len – samples number per channel in raw ADC data raw_num – number of channels in raw ADC data
3	b[15..0] - dsp_mask for TKO1 b[31..16] – dsp_mask for TKO2	0x80000003 means channels 1 and 2 of the TKO1 and channel 16 of the
4	b[15..0] - dsp_mask for TKO3 b[31..16] – dsp_mask for TKO4	The number units in dsp_masks are equal to dsp_num

Output data format (cont.)

Offset	Contents	Comments
5	b[15..0] - raw_mask for TKO1 b[31..16] – raw_mask for TKO2	
6	b[15..0] - raw_mask for TKO3 b[31..16] – raw_mask for TKO4	The number units in raw_masks are equal to raw_num
7 … 6+dsp_num	DSP results b[17..0] – amplitude b[29..18] – time b[31..30] – flags	
7+dsp_num.. 6+dsp_num+raw_len	raw_len RAW ADC samples for the first marked channel in raw_mask	
7+dsp_num+raw_len.. 6+dsp_num+2*raw_len	raw_len RAW ADC samples for the second marked channel in	
…		
7+dsp_num+ raw_num*raw_len	FF550000	FOOTER

ECL FINESSE initialization

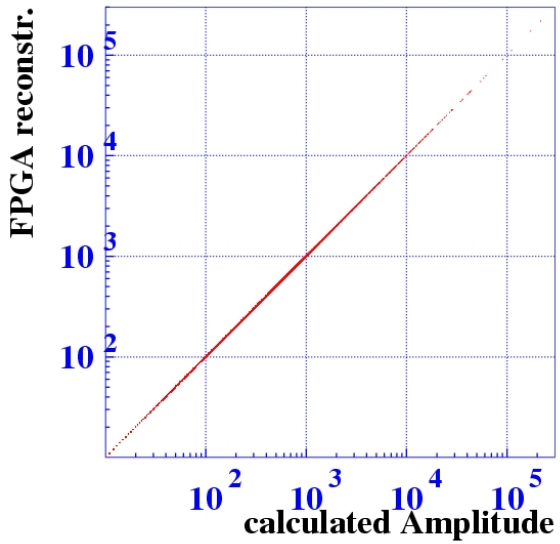
1. Load driver (once after COPPER boot up):
   `insmod cprfin_ecl.o`
2. Load firmware (once after COPPER boot up):
   `cp he2932.bin /dev/copper/ecl_conf:[ab|cd]`
3. Load DSP coefficients and supplement settings:
   `cp dspfile.ecldsp /dev/copper/ecl_dsp:[ab|cd]`
4. Setup other parameters:
   `user_soft/ecl_setup [ab|cd]`
   or using library `cprfin_ecl_lib.` The initialization is made via ioctl() calls

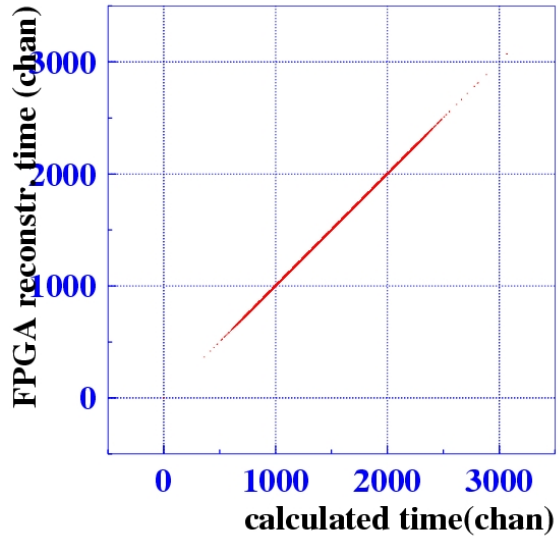
ECL FPGA settings

There are several kinds of FPGA parameters:

1. parameters and coefficients concerning DSP – special file
2. parameters of the synchronization with TKO modules and ADC work.
3. Masks for DSP and RAW ADC DATA – they must be changed for local run and luminosity run
4. Decimation factor Fd– how often FPGA stores raw ADC data. Can be set from 1/1 to $1/10^7$

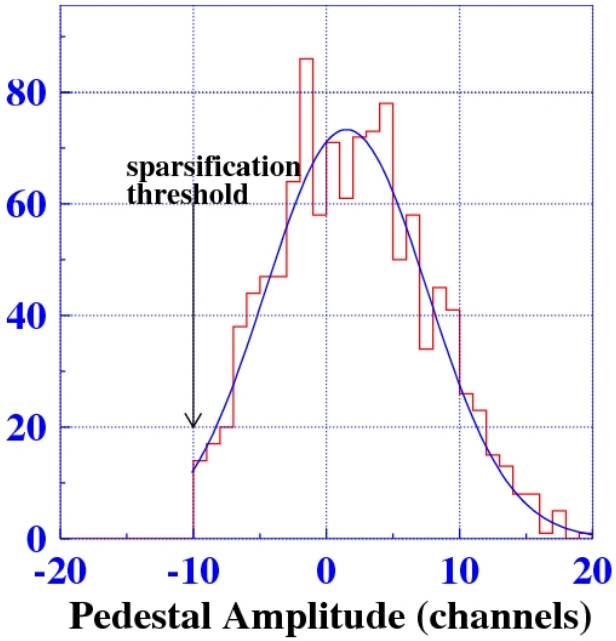
Cosmics reconstruction

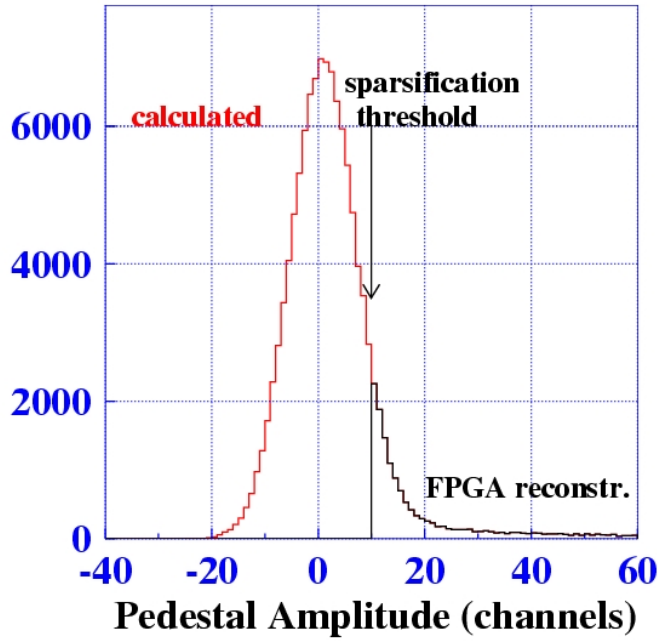




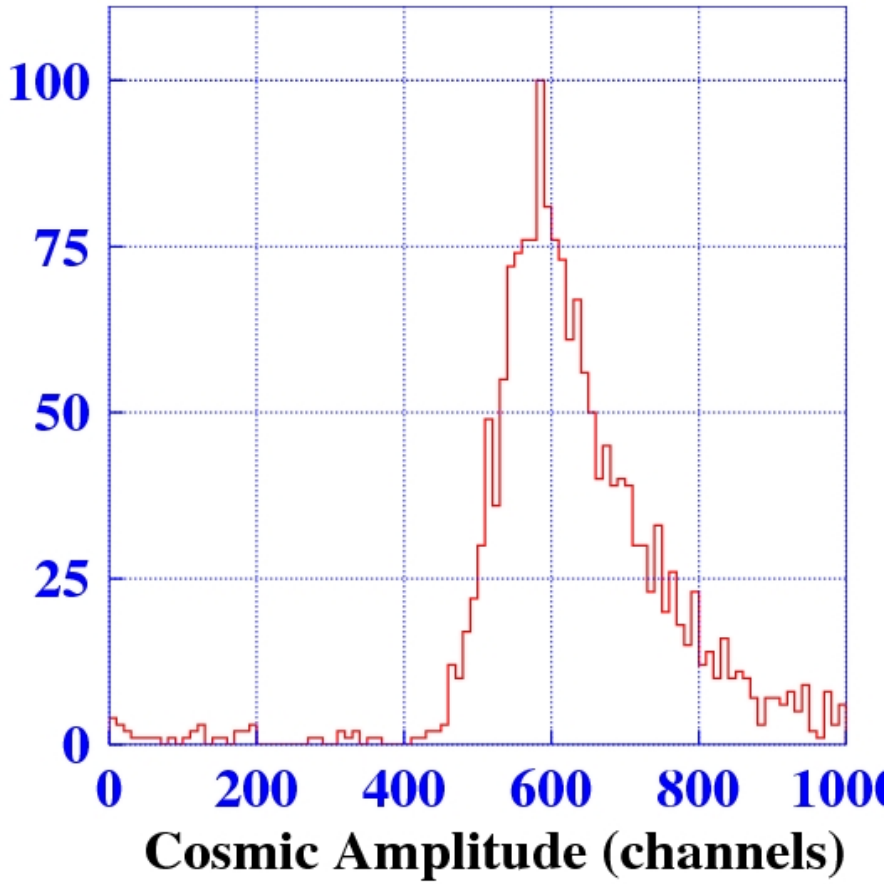
Reconstruction in FPGA is equal software reconstruction

Reconstructed pedestal

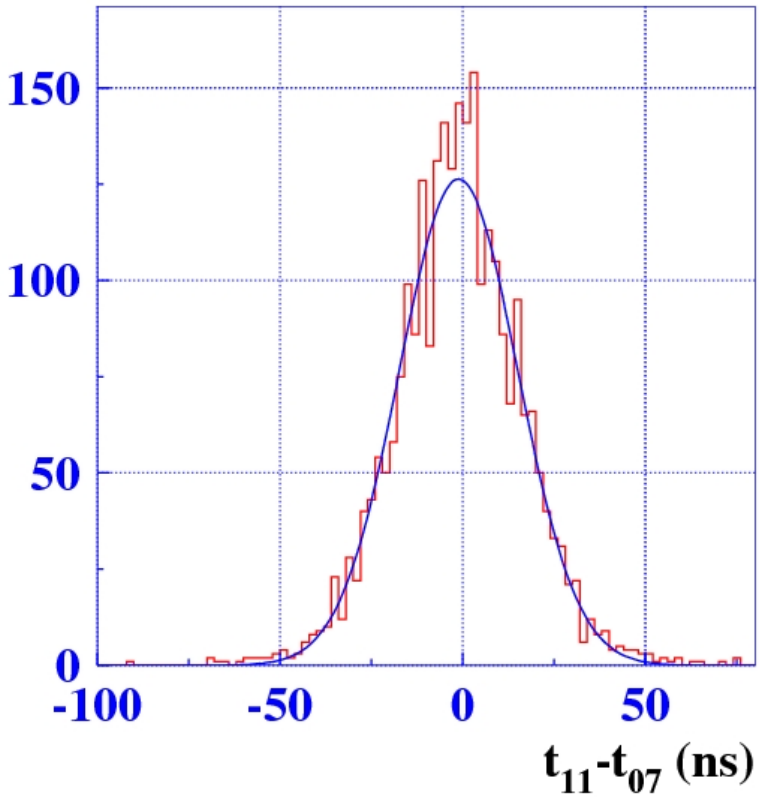


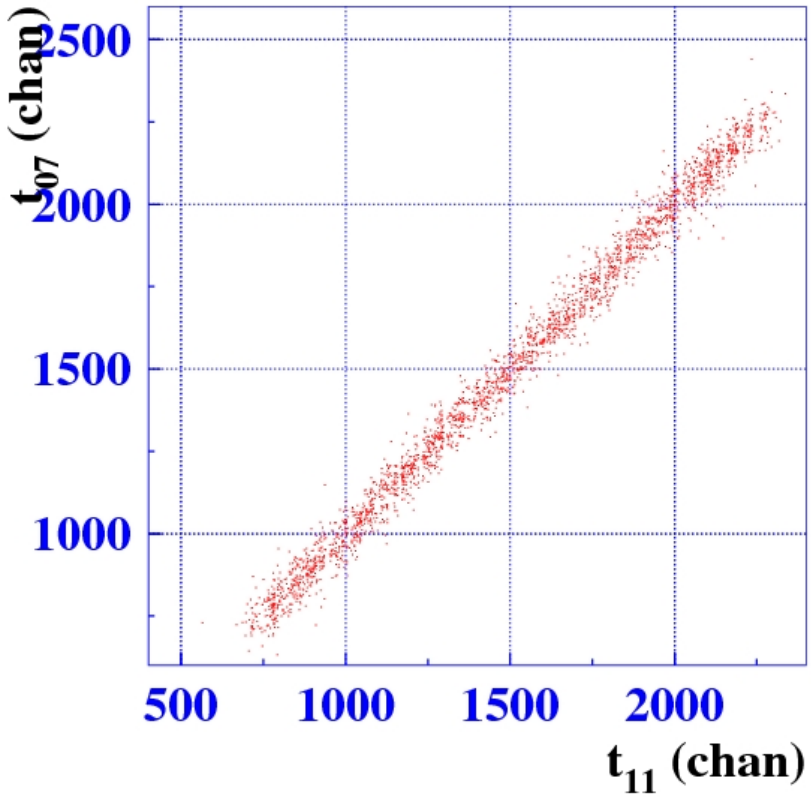


Reconstructed amplitude



Comparition of reconstructed time for 2 channels

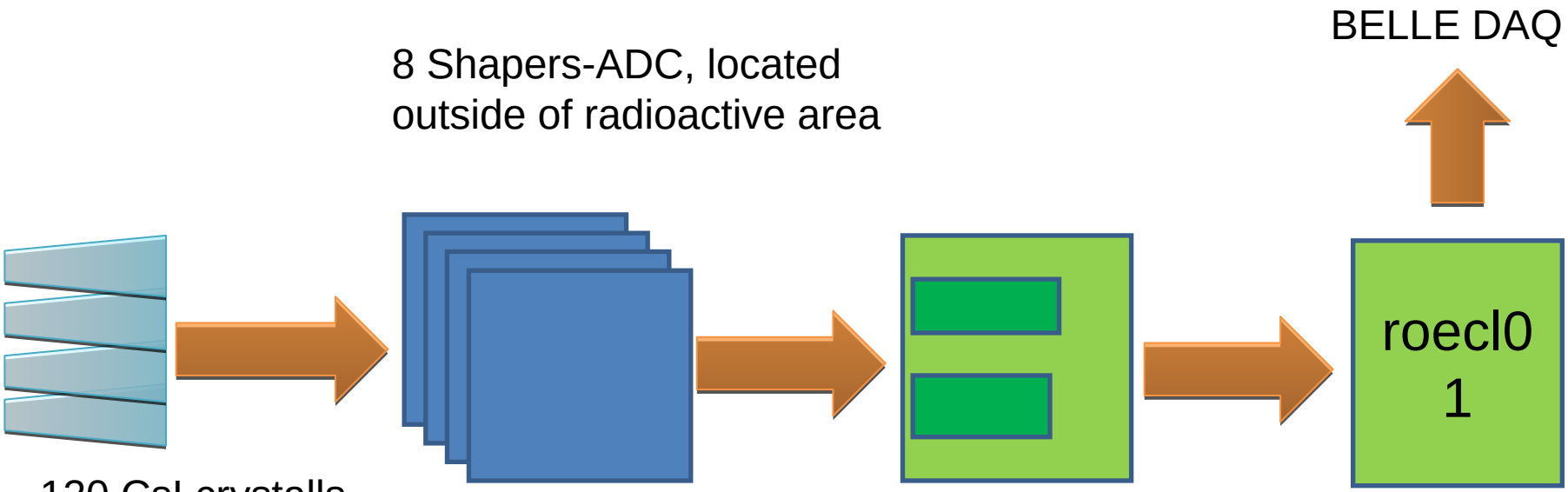




Status

- The hardware implementation of DSP algorithm is fully debugged (no evidence against that). The hardware result of over then 80000 cosmics events matched sofware version of DSP restoration algorithm.
- There are 5 FINESSEs and 8 Shapers ready – That’s enough to serve 1/8 of backward endcap

Installation of new electronics



We are going to replace part of current electronics

Current activity

- Debugging the ECL DAQ software left by Kiyama.

To do

- Install the new new electronics for 1/8 of backward endcap (120 crystalls)
- Test data pass to BELLE DAQ
- Check hardware DSP implementation and consistency of read out data on cosmics
- Measure real noise and coherent noise
- Test of DAQ reliability (with and without parallel readout from FASTBUS part of ECL) – tune related software
- Measure maximum capable trigger rate
- We hope the new electronics and new DAQ will be tested with beam data at October!!!

Thank you
for your attention