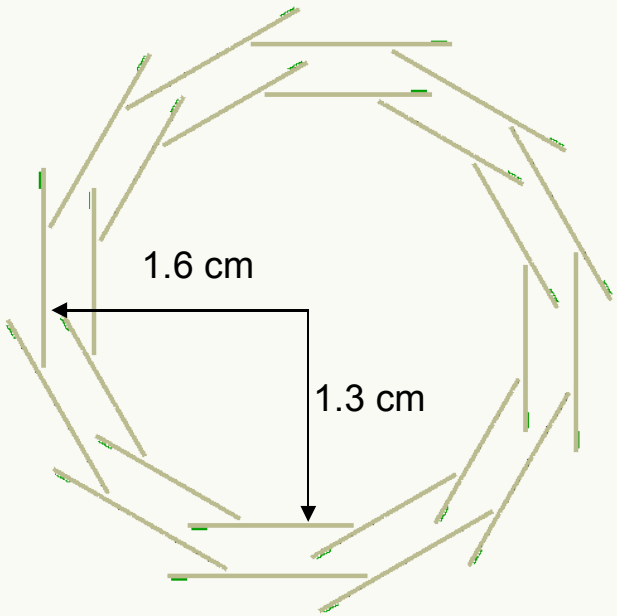
Pixel data size, rate and acquisition

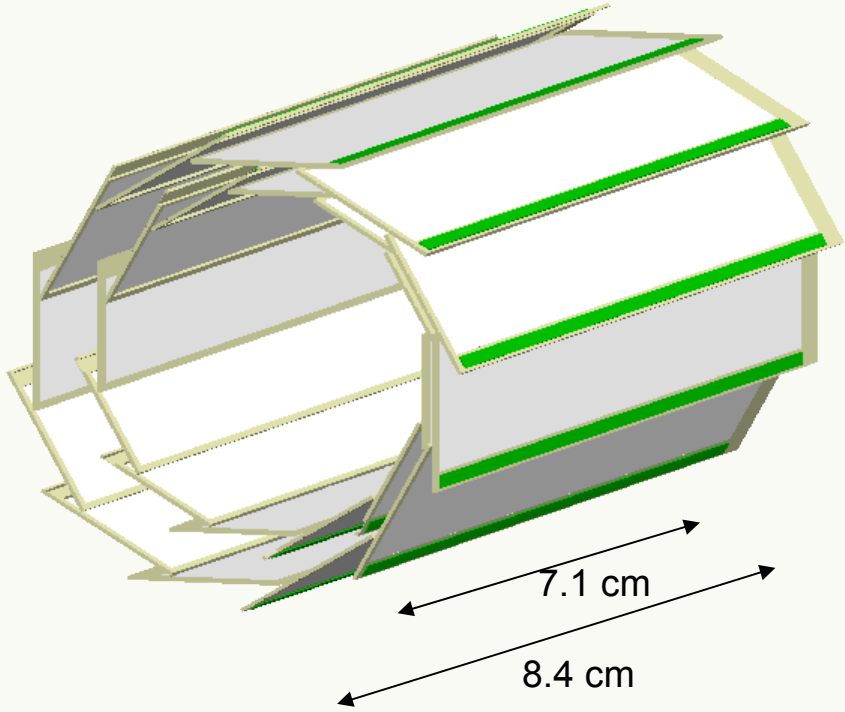
Introduction

- A “generic” approach...
  - Try to decouple from any available technology... just “pixels”
- Factors that determine the data size,
  - Background ↔ Occupancy
  - Pixel size
  - Trigger rate
  - Acquisition
  - ....
- SuperBelle DAQ

Pixel layout

- ✔ Two layers of pixels:
  - ➔ 12 modules each



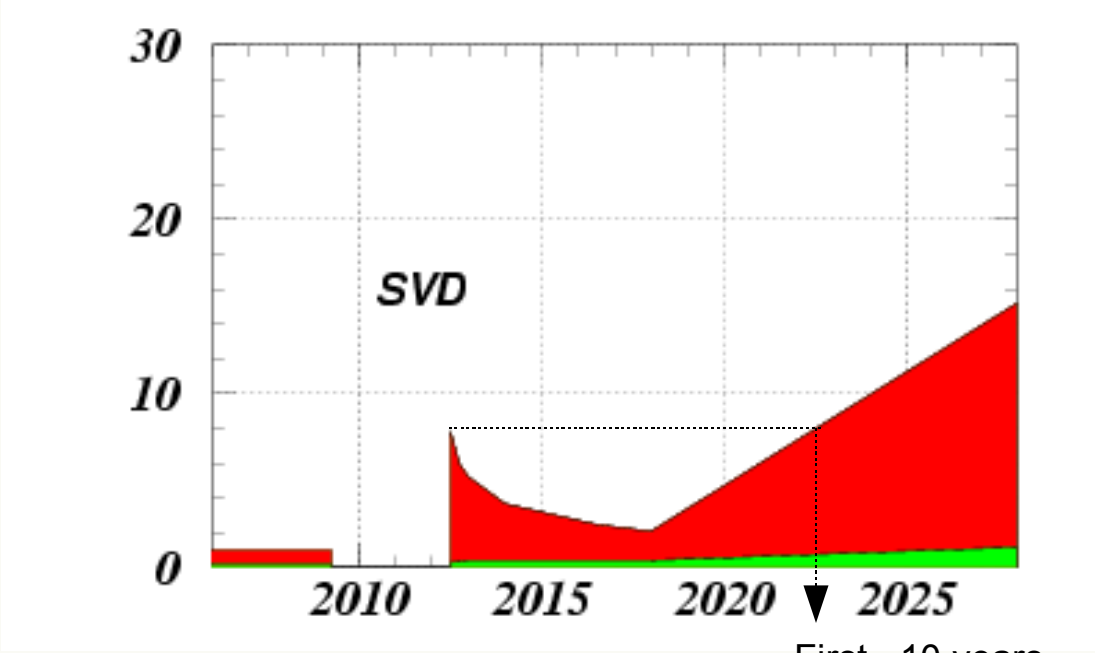


LOI layout:

L1 R=1.3 cm 0.8 x 7.1 cm^2
L2 R=1.6 cm 1.0 x 8.4 cm^2

Background

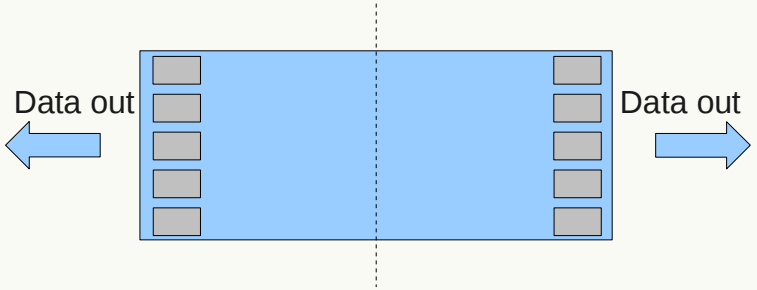
- The expected occupancy at the initial conditions:
  - Consider only the “initial” conditions, which already cover first ~10 years
  - Estimated from from the SVD2 8% occup.
    - $1/R^2$ dependency: from 2cm to 1.3 and 1.6 cm
    - Higher background: 8x larger (initial conditions)
  - Hit density is:
    - Layer 1: 0.4 hit/s/μm^2
    - Layer 2: 0.265 hits/s/μm^2
    - Not clear if the “occupancy” quoted in different sources refers to “strips” or “hits”



Pixel size

- We are dominated by low momentum tracks (<1GeV/c)
  - Low material
  - MS error (beampipe & 0.14%X0 Si ~ 9 μm at 1 GeV)
  - Modest intrinsic resolution of σ ~ 10 μm sufficient:
    - pixels can be large
- Upper limit set by required intrinsic resolution:
  - What are the expected values for Rϕ and Z ?

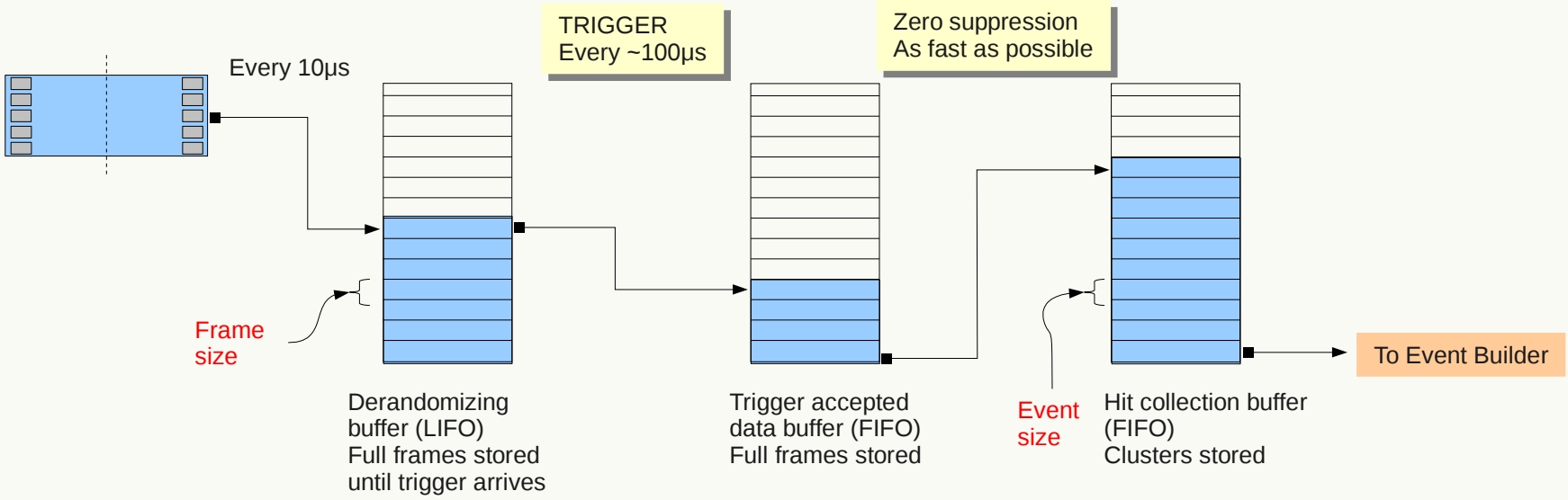
The data size



- ✔ Read modules at both ends
- ✔ We are able to read a complete frame (or side) in 10 µs
- ✔ The trigger rate is 10kHz
- ✔ We can do zero suppression
  - ➔ We assume 32 bits/pixel
    - ↘ ~8 bits for the ADC value
    - ↘ ~24 bits for address info
- ✔ Number of pixels/cluster: $1 + \frac{1}{2} (S_{cluster}/S_{pixel})$
  - ➔ Cluster size: from preliminary simulations, the cluster is:
    - ↘ Normal incidence: ~6000 μm^2
    - ↘ 10^0 polar angle: ~22000 μm^2
  - ➔ Used the normal incidence for this exercise...

Data path

- Assume we have a DAQ like in the picture below:
  - Continuous frame readout
  - 2 buffers for full frames
    - 1st is a LIFO that stores the frames until the data arrives
    - 2nd is a FIFO which stores the accepted events
    - We need to know the frame size to optimize the buffer sizes, in particular the second
  - We have a “processor” that makes zero suppression
    - Clusters found are stored in the 3rd buffer, which is a FIFO
    - We need an estimate of the event size to optimize the buffer capacity
  - Data from 3rd buffer is sent to the Event Builder.



Data rates

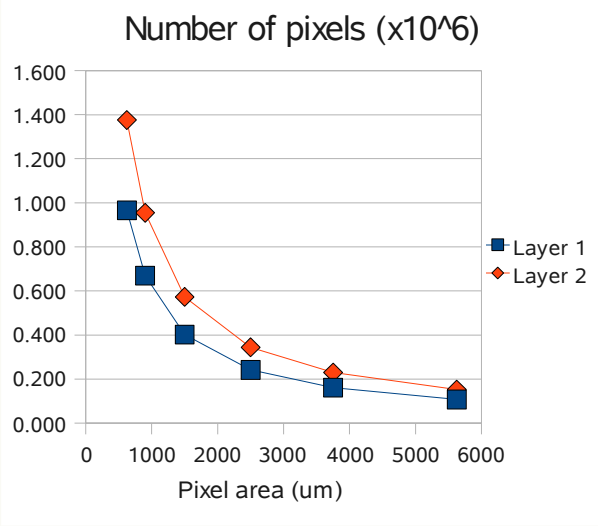
- ✔ Try with different pixel sizes.
- ✔ The numbers here correspond to one module side

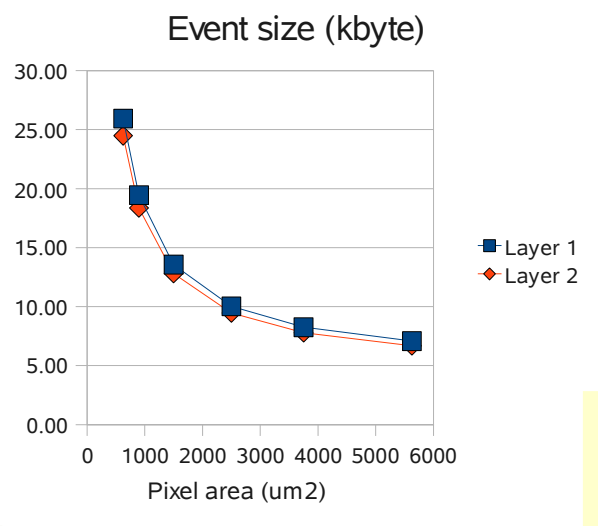
Layer dimensions and hit density

	Width (μm)	length (μm)	Area (μm^2)	Hit density (hit/s/μm^2)	hit rate (hit/μs)
Layer 1	8.50E+03	7.10E+04	6.04E+08	0.400	2.41E+02
Layer 2	1.00E+04	8.60E+04	8.60E+08	0.265	2.28E+02

				Layer 1						
R-phi	*Z*	*Pixel area*	*Npix/Cluster*	*Ncol*	*Nrows*	*Npixel*	*Frame size (Mbit)*	*Nhits/frame*	*Event size (kb)*	*Data rate (Gbit/s)*
25	25	625	5.50	340	2840	0.966	3.683	2414	25.93	1.98
30	30	900	4.13	283	2366	0.670	2.554	2414	19.45	1.48
30	50	1500	2.88	283	1420	0.402	1.533	2414	13.56	1.03
50	50	2500	2.13	170	1420	0.241	0.921	2414	10.02	0.76
50	75	3750	1.75	170	946	0.161	0.613	2414	8.25	0.63
75	75	5625	1.50	113	946	0.107	0.408	2414	7.07	0.54
				Layer 2						
				Ncol	*Nrows*	*Npixel*	*Frame size (Mbit)*	*Nhits/frame*	*Event size (kb)*	*Data rate (Gbit/s)*
				400	3440	1.376	5.249	2279	24.48	1.87
				333	2866	0.954	3.641	2279	18.36	1.40
				333	1720	0.573	2.185	2279	12.80	0.98
				200	1720	0.344	1.312	2279	9.46	0.72
				200	1146	0.229	0.874	2279	7.79	0.59
				133	1146	0.152	0.581	2279	6.68	0.51

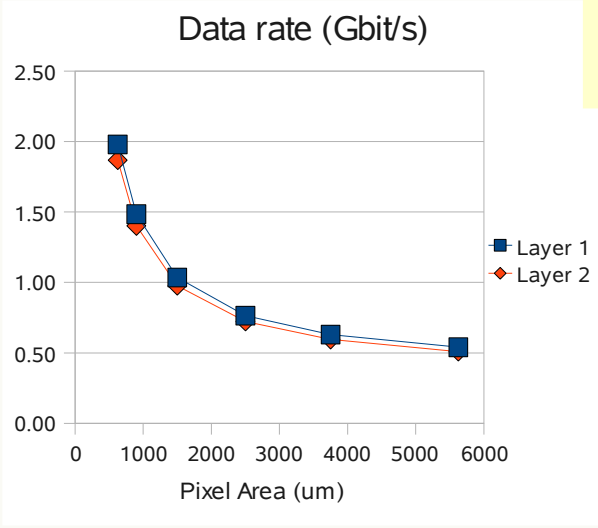
Data size and rate



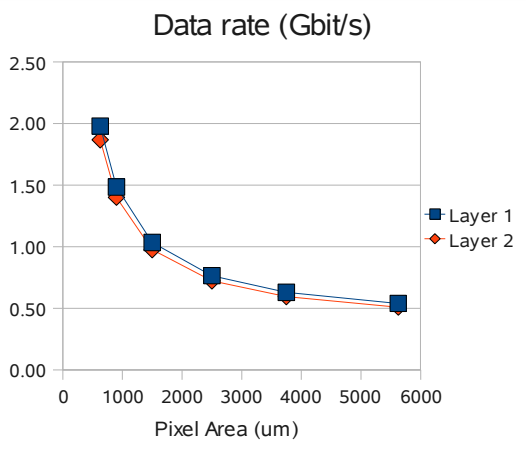


- ✔ Pixel size has a huge influence on the data size
  - ➔ Has to be optimized with simulation studies..

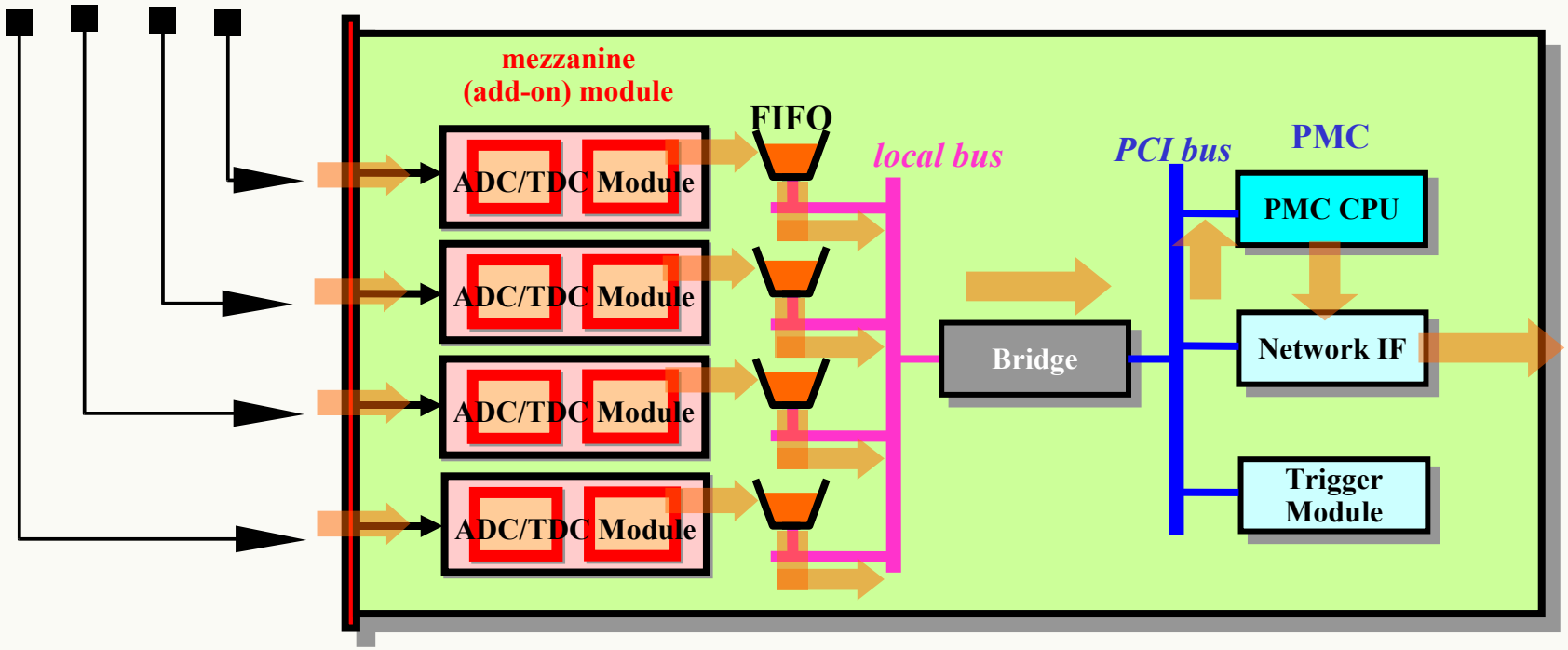
R-phi	*Z*	*Pixel area*
25	25	625
30	30	900
30	50	1500
50	50	2500
50	75	3750
75	75	5625



SuperBelle DAQ



- ✔ Each input has, in the best case, ~0.5 Mbit/s
- ✔ Local bus 4x more
- ✔ PCI bus can handle at most 133 Mbit/s
- ✔ A serious bottleneck...



SuperBelle DAQ (II)

- ✔ Possible remedies: Further data reduction on Finesse boards
  - ➔ Smart coding of address information in the cluster
  - ➔ Level II trigger rejection
    - ➘ We need access to that information
  - ➔ ROI (Regions of interest)
    - ➘ Needs higher level information
  - ➔ Smart algorithms to reject background based on
    - ➘ Pulse height
    - ➘ Cluster size
    - ➘ ...

Conclusions

- ✔ Nothing comes for free...
  - ➔ Granularity and resolution have a price
- ✔ Pixel data stream is too big for the current DAQ even in the most optimistic case
- ✔ Adding “intelligence” to the FINESSE cards may help but probably will not solve the problem
- ✔ We need to understand the background:
  - ➔ Have real estimates of the occupancies
  - ➔ Discriminate background from real data