CMOS MAPS Silicon Pixel VTX for SuperB

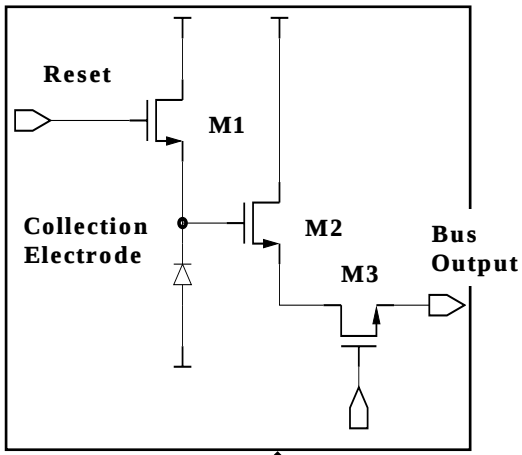
Gary S. Varner

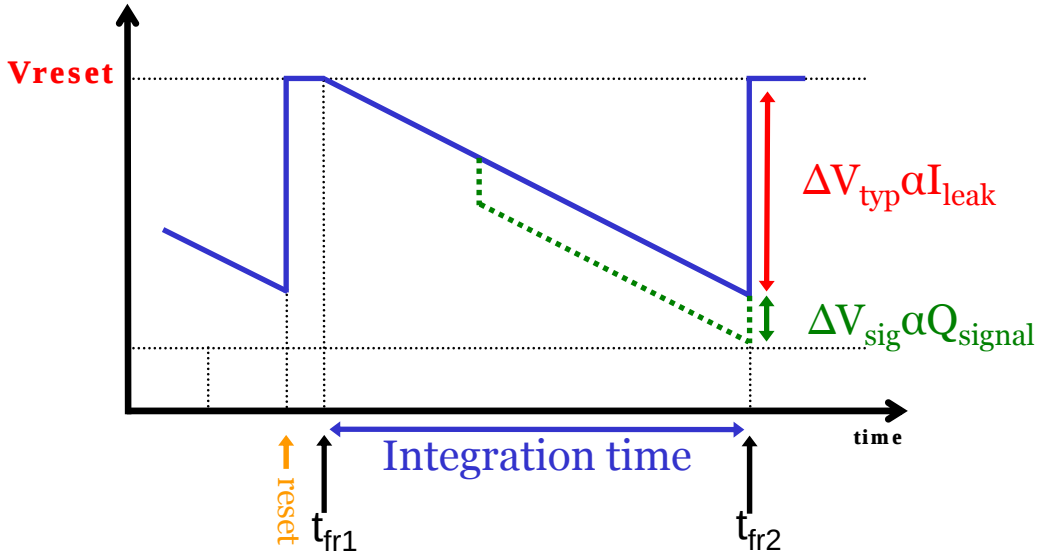
Open Collaboration Meeting #2

July 4th, 2008

- Issues
- CAP series
  - Evolution of strategy
  - Desire for improvement
  - Hexagonal Pixel (hixel) [CAP7]
- Next generation

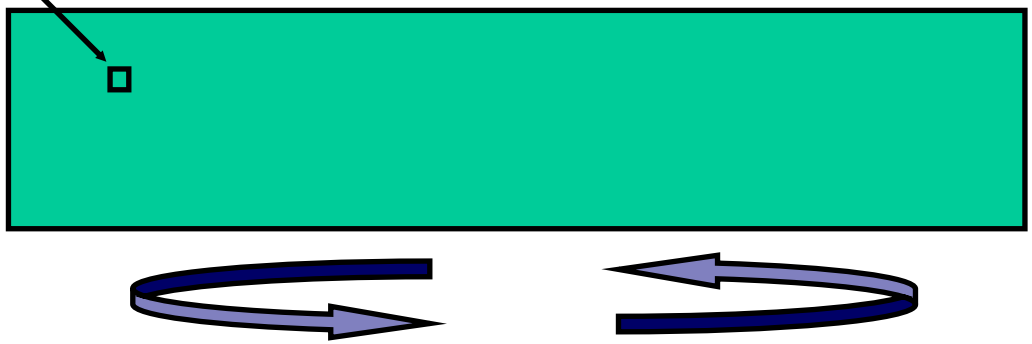
Continuous Acquisition Pixel (CAP)





Pixel

Array of 132x48 pixels



High-speed

analog

ADC

& storage

Pixel Array: Column select – ganged row read

Low power – only significant draw at readout edge

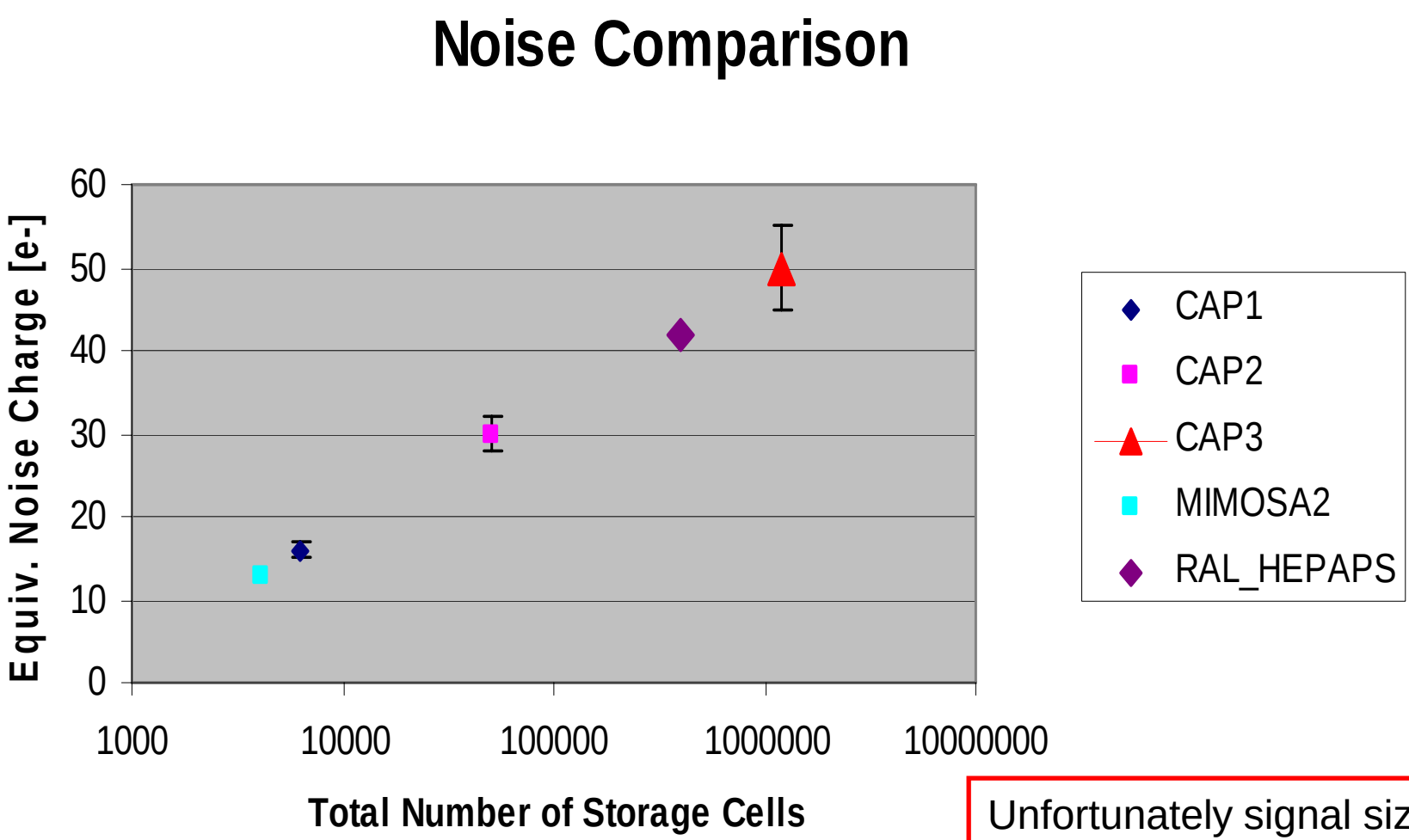
sBelle CMOS Pixel Study Activities

- CAP1/2 [MAPS technology] Studies
  - Characterization of CAP1 in test beam [NIM **A541** (2005) 166]
  - Study of radiation hardness/storage [IEEE Trans.Nucl.Sci.**52** (2005) 1187]
  - Storage density/max. pipeline depth studies
- CAP3 "full size" Detector [NIM **A565** (2006) 126]
  - Development of laser scan system for systematic studies
  - Systematic scan and study of transfer rate and signal uniformity
  - Non-uniformity and transfer limitations observed
- CAP4 AMS 0.35um Opto [NIM **A568** (2006) 181]
  - Study of new analog storage/readout – evaluation started
- CAP5, 7 SOI prototypes – studies continue
  - Study of 0.15um OKI process [SLAC-PUB-12079]
  - Fully depleted, time-space correlation storage study

Critical R&D Scorecard

1. Readout Speed — 100kHz frame rate, 10kHz L2 accept
   - CAP3 too slow, SNR concerns
2. Radiation Hardness — >= 20MRad
   - Leakage current OK (CAP2) for short integration time
3. Thin Detector — <= 50μm, layer
   - 50μm LBL test bench, thinning at APTEK (same SNR)
4. Full-sized detector — Span acceptance (reticle limit)
   - CAP3 large acceptance biasing/uniformity

Noise (ENC): Summary of MAPS

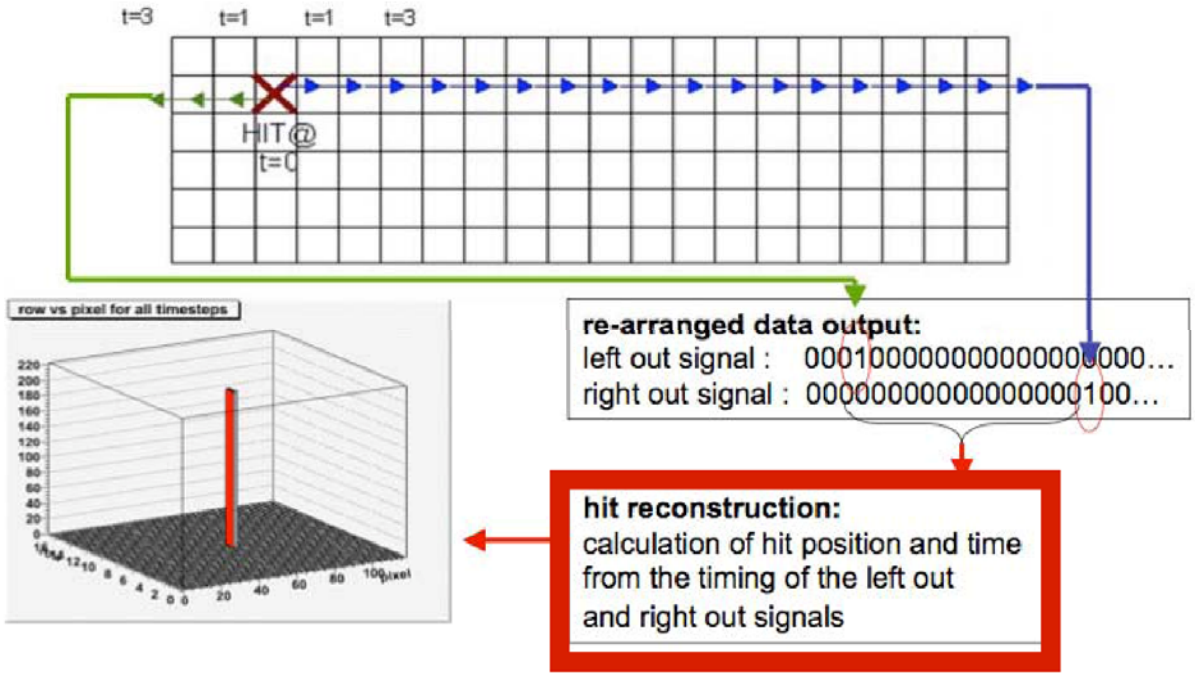


Unfortunately signal size
Fixed and small

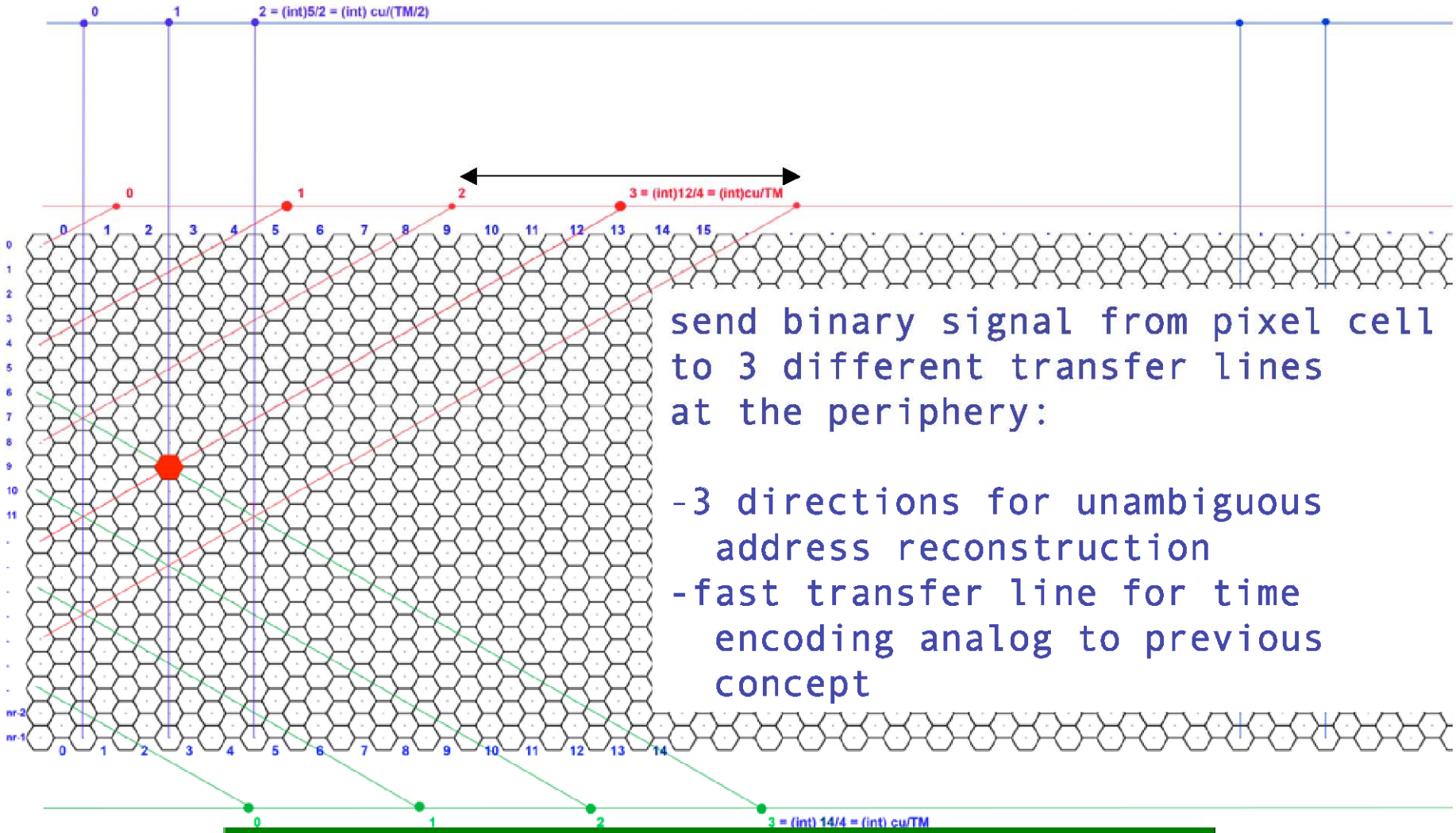
sBN0007 for details

hit reconstruction for a binary detector with time encoding

you are familiar with this:



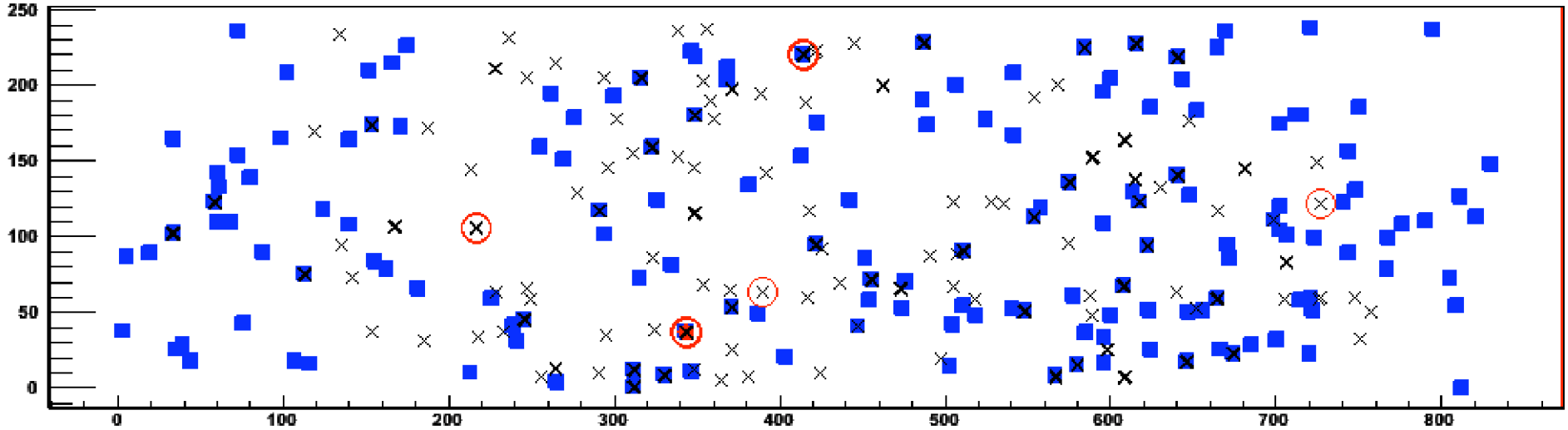
hexagonal pixel layout with external transfer lines



send binary signal from pixel cell to 3 different transfer lines at the periphery:

-3 directions for unambiguous address reconstruction
-fast transfer line for time encoding analog to previous concept

example event (TM = 12)



- background
- seeded hit
- x all reconsructed hits in time window
- reconstructed @ t_{trig}

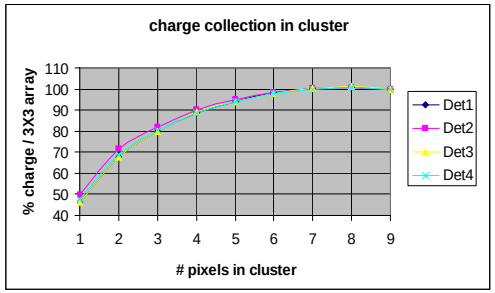
CMOS Option Summary

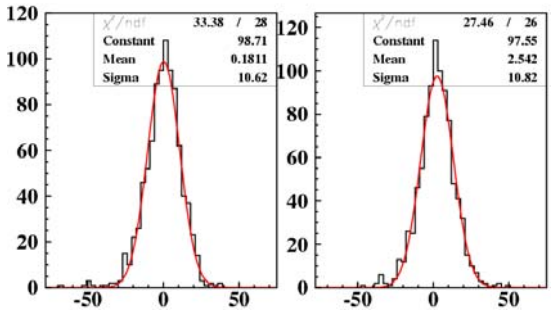
- Need to demonstrate binary can work
  - SNR is still an issue
  - SOI variant probably more realistic
    - Next OKI submission
    - TSMC 0.35um opto submission end of July
  - Issues of cross-talk, threshold dispersion

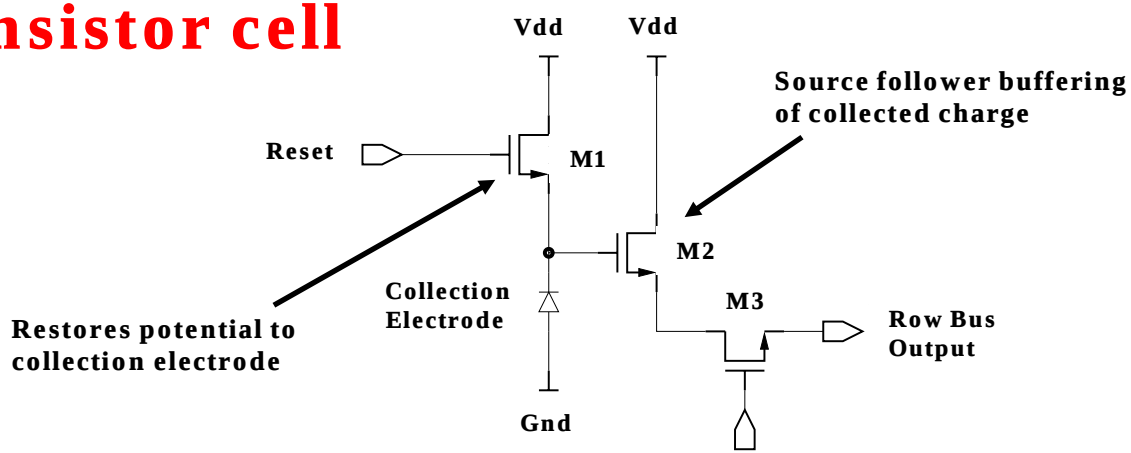
- Binary has possible benefit
  - Reduced data size
  - Intrinsic Resolution degradation not critical
  - Original benefit of commercial CMOS MAPS

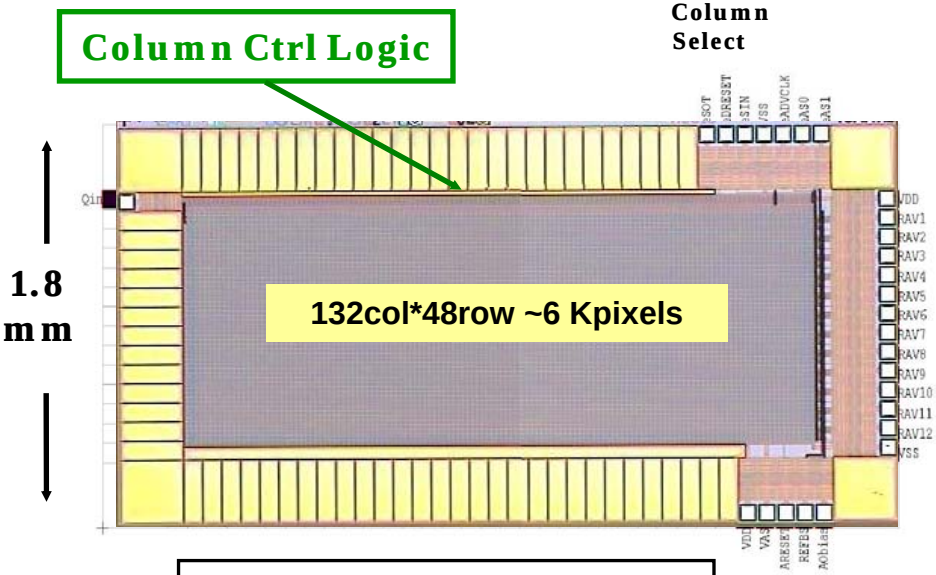
Cont. Acq. Pixels (CAP) 1 Prototype

CAP1: simple 3-transistor cell









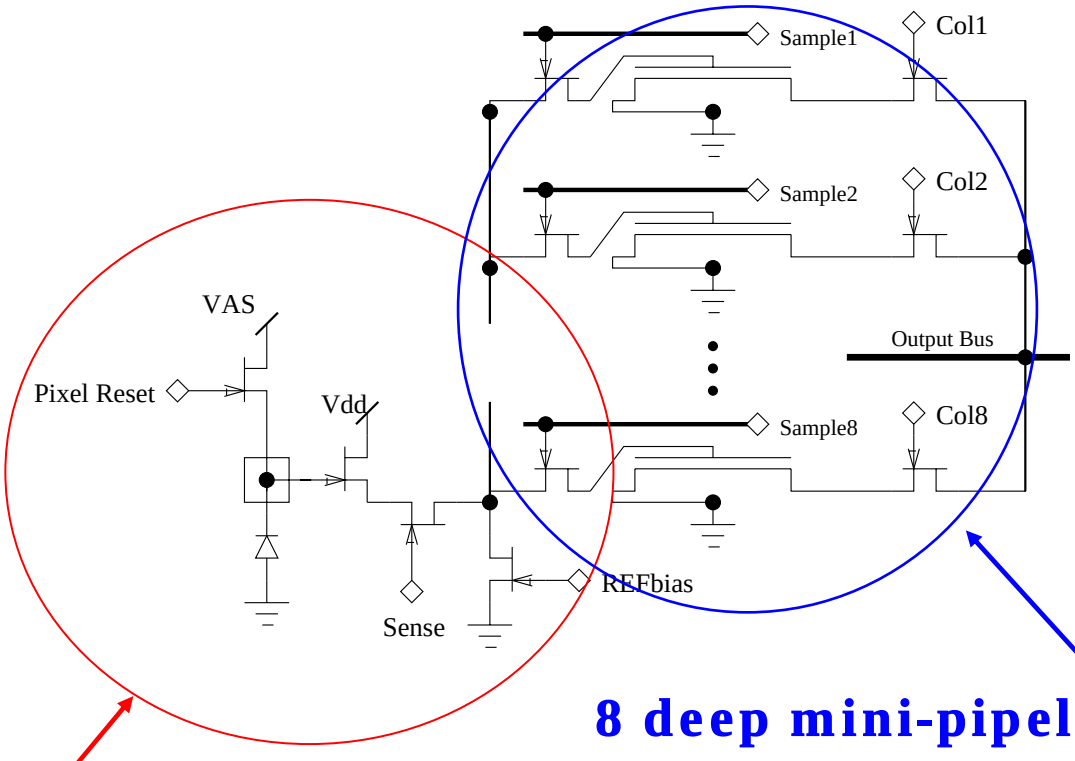
Pixel size:

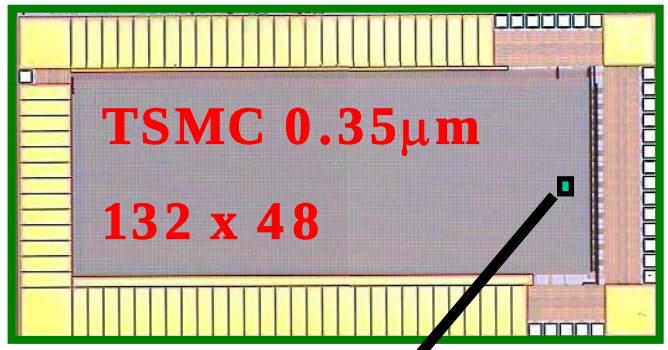
22.5 μm x 22.5 μm

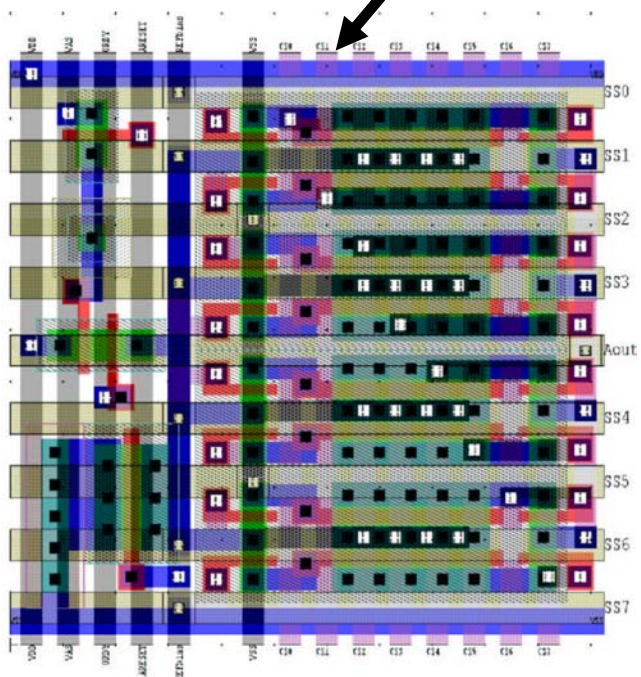
CAPs sample tested: all detectors (>15) function.

NIM A541:166-171 (2005)

CAP2 – Pipelined operation







3-transistor cell

8 deep mini-pipeline in each cell

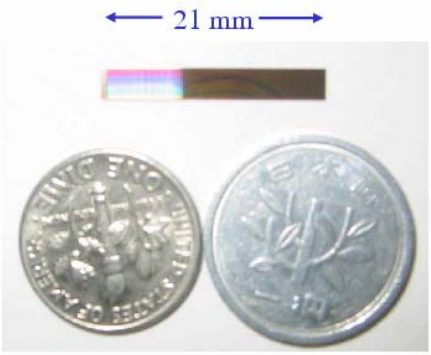
132x48=6336 channels 50688 samples

10µs frame acquisition speed achieved!

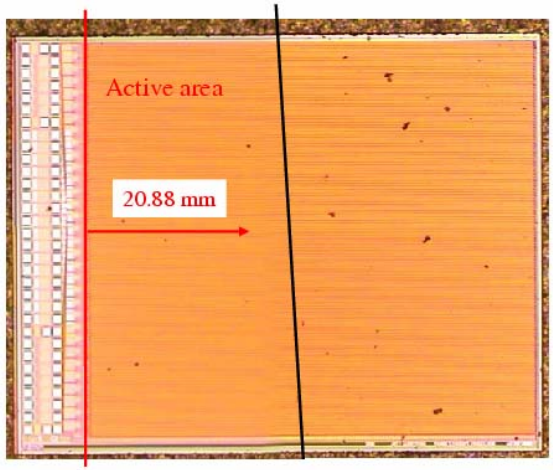
Pixel size 22.5 µm x 22.5 µm

[IEEE Trans.Nucl.Sci.**52** (2005) 1187]

CAP3: Full-size Detector Test/Lessons learned



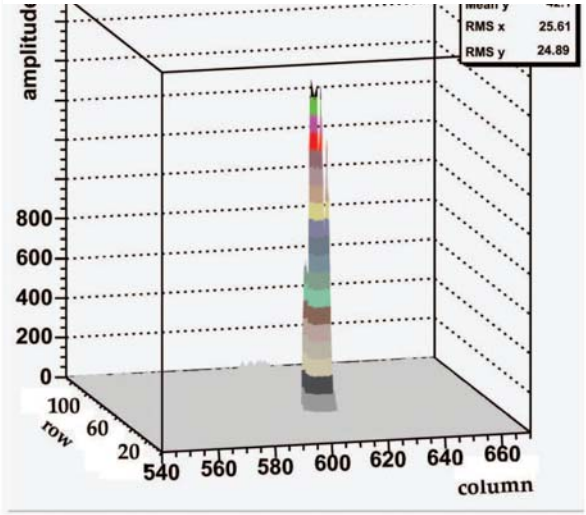
928 x 128 pixels = 118,784

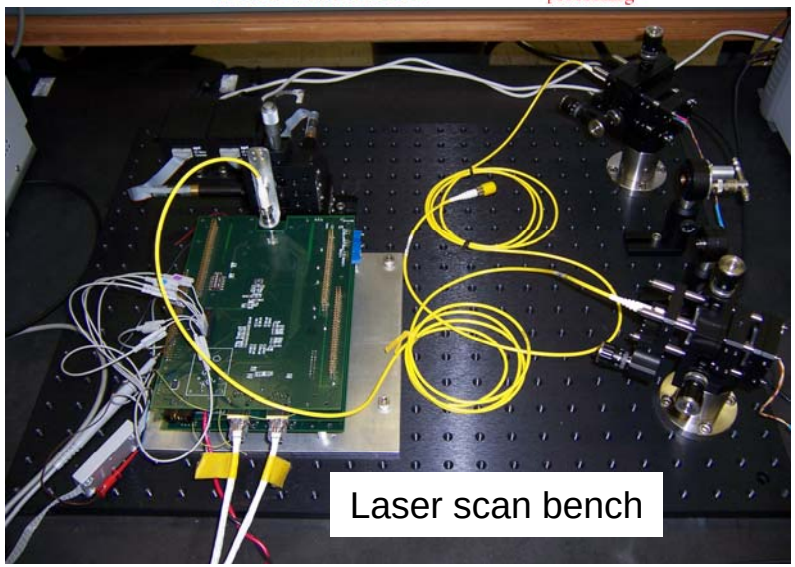


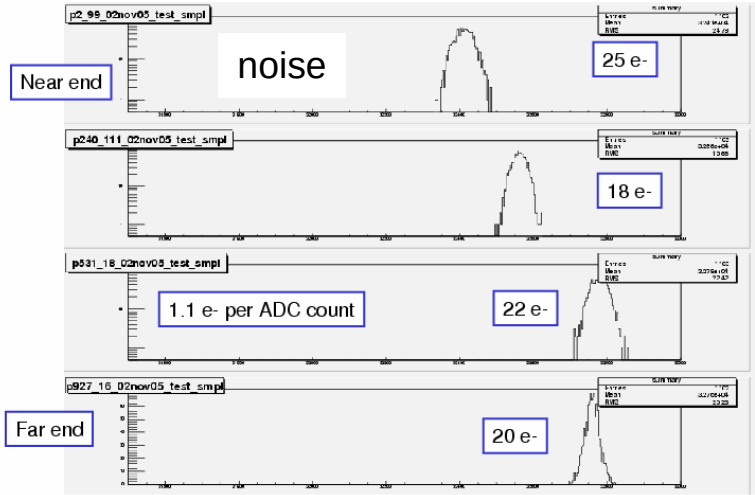
~4.3M transistors

>93% active without active edge processing

Laser spot (backside illumination)







Pixel Occupancy Scaling

- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm²
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm²
    - Reduction factor ~8400
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal loss:
    - 0.8μs SVD vs. 10μs PXD (could be improved)
    - Increase factor ~ 12.5
  - Grand total:
    - $10\% * 20 * 8400^{-1} * 12.5$
    - Can expect ~ 0.3% occupancy (no ghosting)

CAP5

BINARY READ OUT