COPPER Revision and New CPU

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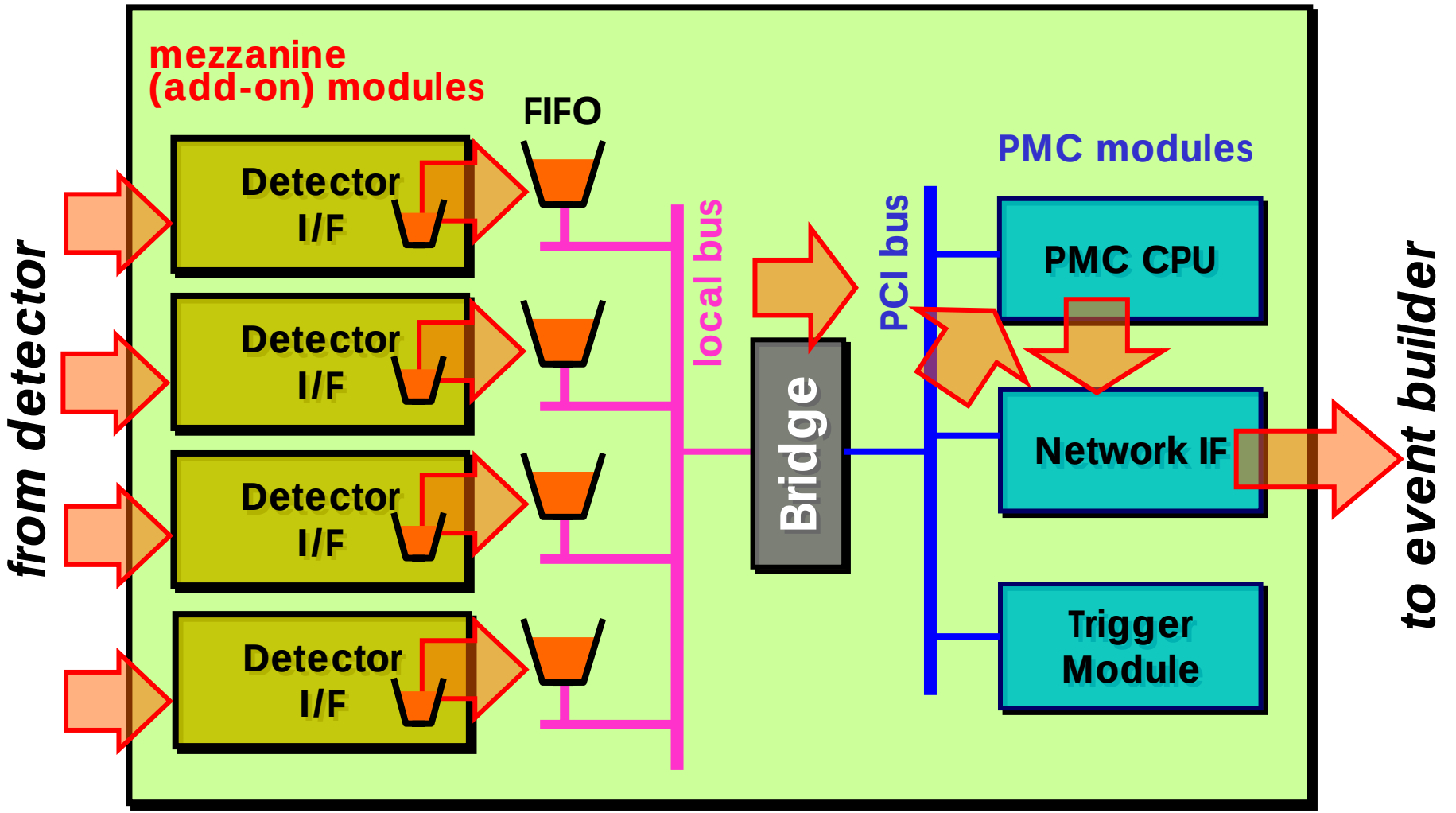
Part I: Introduction

Readout Electronics Block Diagram



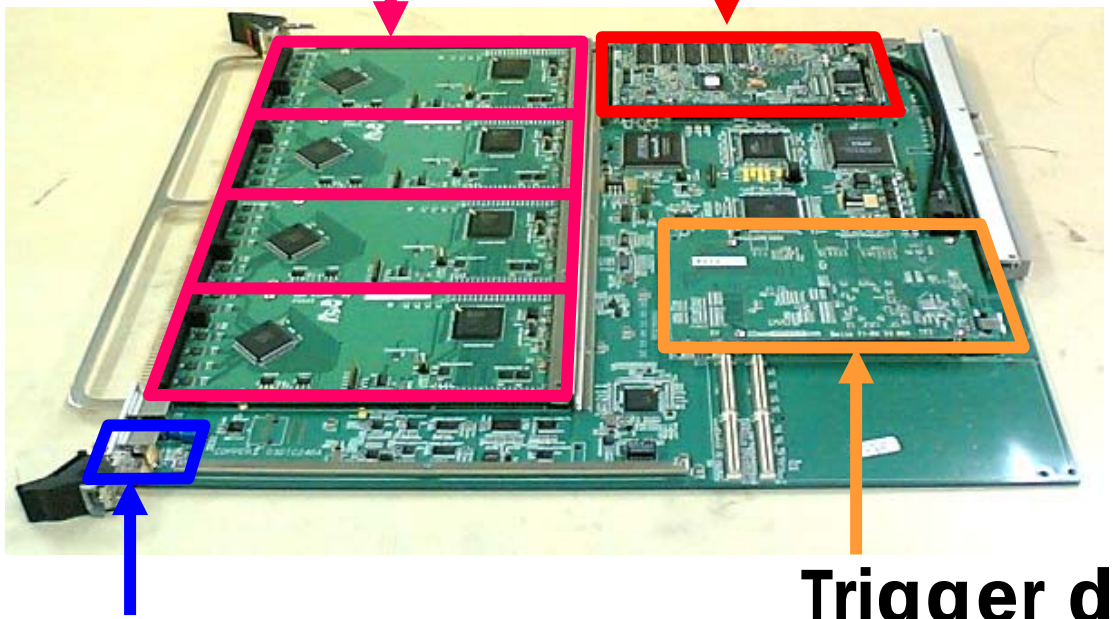
“COPPER-II”

Digitizer module x 4

Add-on modules for the COPPER

Online CPU module

VME9U



RadiSys EPC-6315

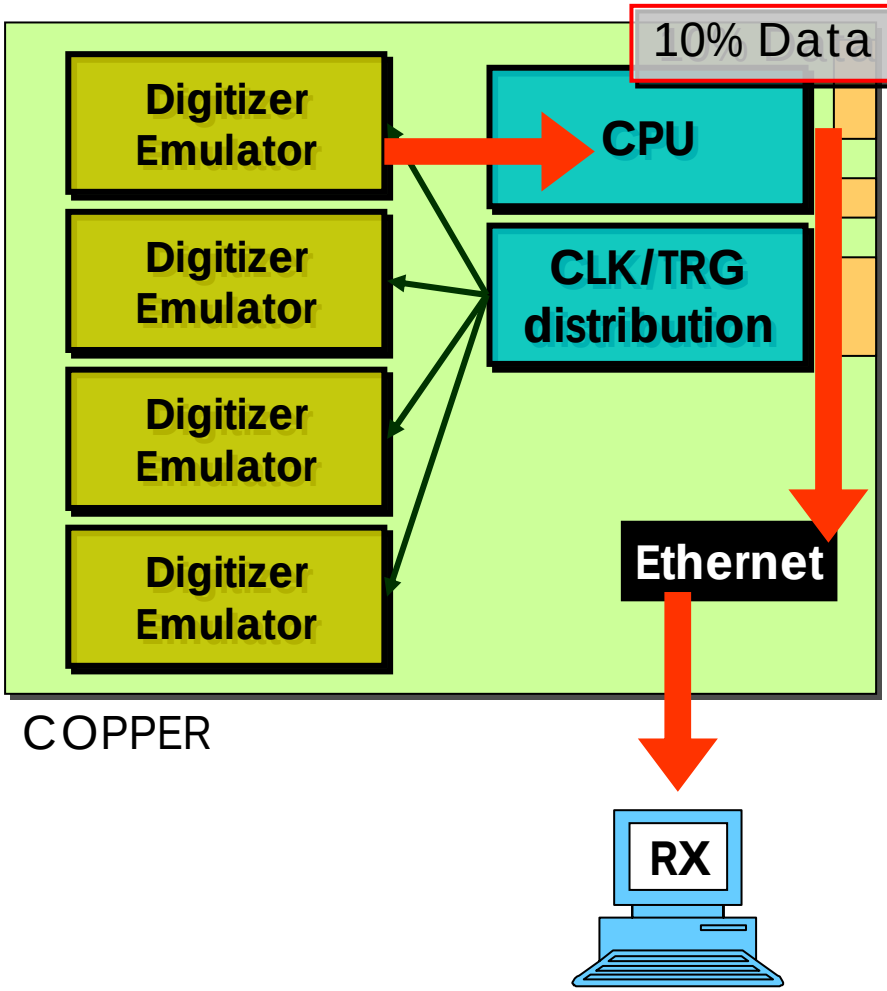
- **Intel P3 800 MHz**
- **256 MB memory**
- Network boot
- RedHat Linux 9

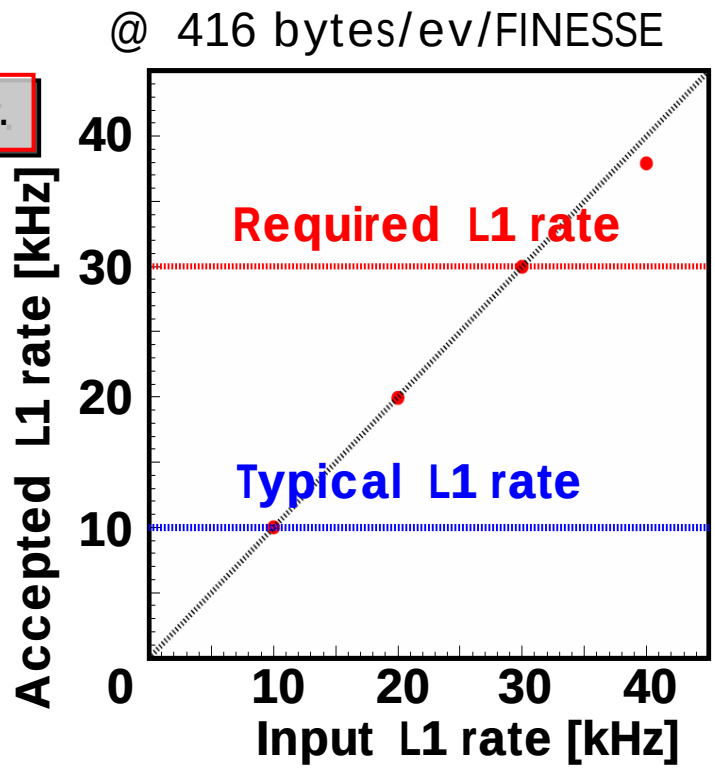
100BaseT port x 2

Data link & control link

Trigger distribution module

COPPER-II Performance Review





COPPER-II works w/ L1 rate >30 kHz

COPPER History in the Belle DAQ

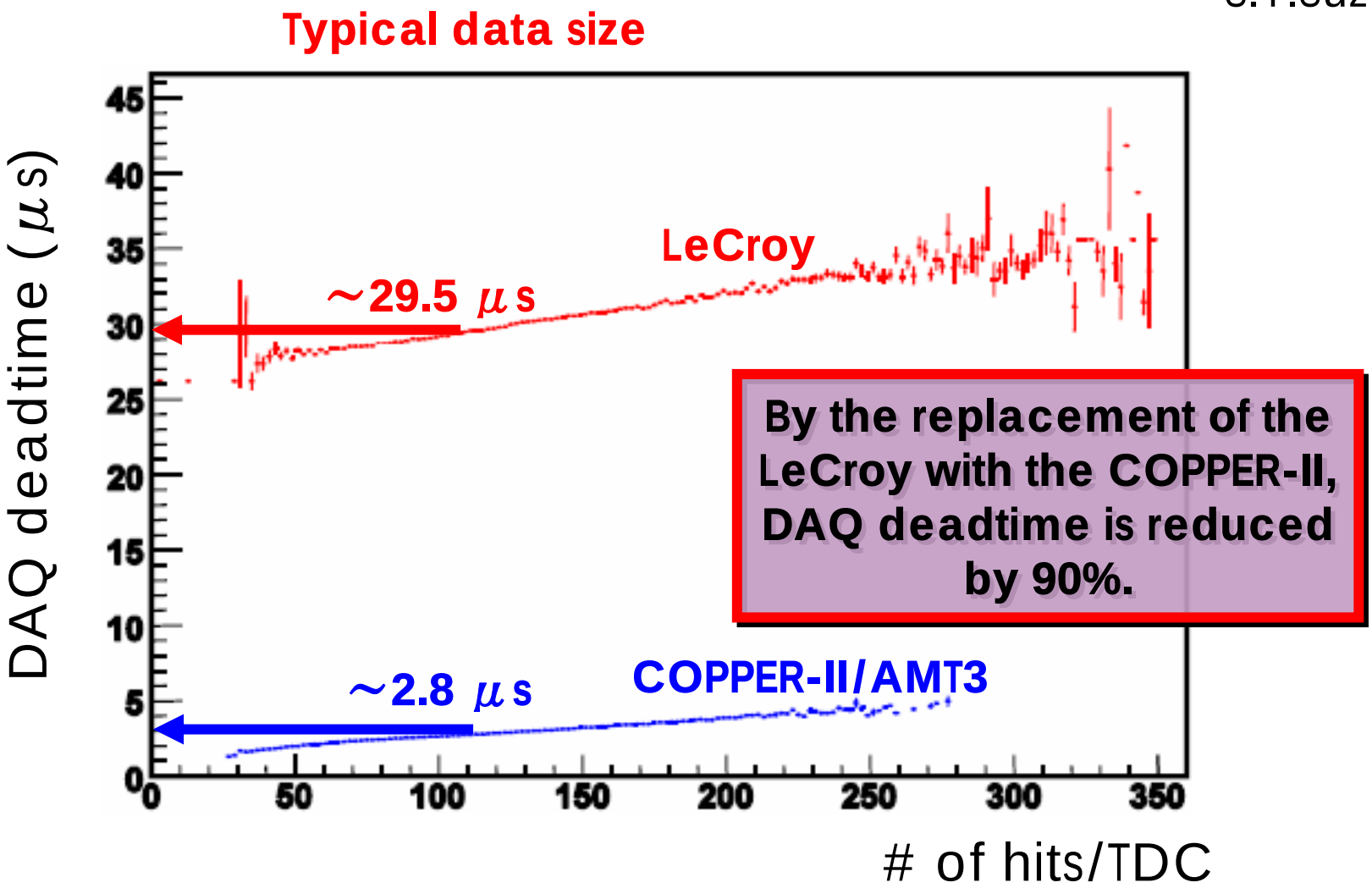
- **2002-2003**
  - Design started.
  - Prototype of the COPPER.
- **2004**
  - Upgrade to the COPPER-II.
  - Proved to work in severer L1 rate (~30 kHz) than the SuperBelle.
- **2005**
  - Debug on AMT3 FINESSE.
  - **EFC DAQ replaced with the COPPER-II's (6).**
  - Compatibility study btw the COPPER-II and the LeCroy.
- **2006**
  - Part of CDC DAQ replaced with the COPPER-II's.
  - More compatibility study.
  - Deadtime study.

Ready to replace all LeCroy DAQ

- **2007**
  - **Full CDC DAQ replaced with the COPPER-II's (89).**
  - **ACC DAQ replaced with the COPPER-II's (24).**
- **2008**
  - **TRG DAQ replaced with the COPPER-II's (26).**
  - **Study to replace KLM DAQ is going on.**

Deadtime Reduction by COPPER

S.Y.Suzuki



Part II: COPPER Revision

COPPER-II → "COPPER-3"

- **Some parts started to discontinue**
  → Need their replacement with up to date parts.
  Major motivation of the upgrade.

- As the technology evolves, price of some parts w/ the higher performance gets much lower:
  e.g. GbE controller.

- Fix some minor inconveniences: e.g. move/change switch positions and shapes for better access.

- Delete unused functions so far.

COPPER-II → COPPER-3

- **The most important rule of the upgrade:**

The COPPER-3 shall be fully compatible with the COPPER-II.

  - FINESSEs, device drivers, and readout software for the COPPER-II shall be used for the COPPER-3 without any modification at all.

List of Major Upgrade Items

1. Replace discontinued parts.

2. Replace discontinuing or out of date parts.
   - RoHS compliant parts.
   - Cyclone → Cyclone3.

3. Replace 100Base-T Ethernet controller (82559) w/ GbE controller (82541).

4. Normalize signal line lengths from the TTRX to each of the 4 FINESSEs.
   - SCLK, TRG etc.

5. Move VME signal receivers to much closer position to the VME J0 connector for more stable signal handling.

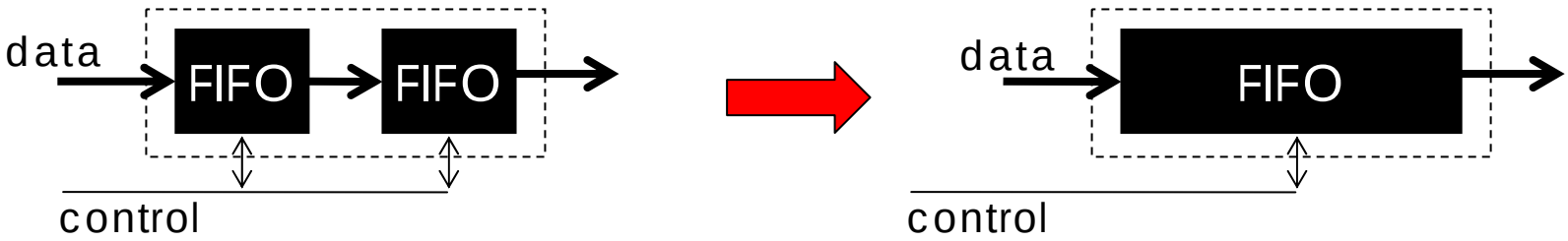
List of Major Upgrade Items

6. Change reset switch shape more accessible.
   – Present switch on the front panel is difficult to push.

7. Move VME base address config. switch to more accessible area.

8. Remove and simplify unused connectors/patterns originally intended for debug use.

9. Join 2 FIFOs to 1. Series of two FIFO chips were aligned to form a larger single FIFO so that we could select FIFO size at production.



10. Change front panel design.

COPPER-3 Short Term Schedule

- Jun. 2nd: Design work started by the company.
- Jun. 30th: Design and schematic chart drawing – **delayed**.
- Jul.4th: ----- TODAY -----
- Jul.18th: FPGA programming.
- Jul.28th: Pattern layout.
- Aug.8th: Board production.
- Aug.29th: Parts assembly.
- Sep.6th: Board verification.
- Sep.16th: Document writing.
- **Sep.26th: Delivery to KEK.**
- **Dec.31st: End of COPPER-3 study by KEK.**

COPPER-3 Long Term Schedule

JFY: Japanese Fiscal Year; from Apr. to Mar.

- **By JFY 2008**
  - Find out and fix most bugs in the COPPER-3 prototype.
    → Makes COPPER-3 ready for the mass production.
- **In JFY 2009**
  - Purchase ~20 COPPER-3. → Single-crate system test.
- **In JFY 2010-2011**
  - Purchase 200-300 COPPER-3. → Build up sBelle DAQ system.
- **In JFY 2012**
  - Start sBelle Operation.

Part III: New CPU

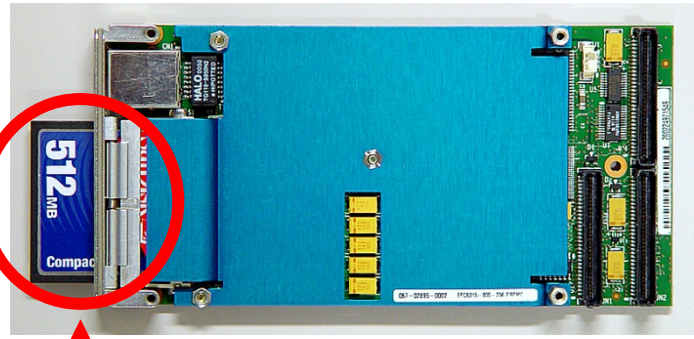
Roles of the COPPER CPU

- **Major roles related to the data handling:**
  - Readout data from 4 pipeline FIFOs on the COPPER.
  - Combine an event chunk from each of the FIFOs to form a single event record.
  - Provide online data monitoring.
  - Format the event record into the Belle standard.
  - Transfer the event record to an external readout PC of the COPPER via Ethernet.

- **Peripheral roles:**
  - Initialize COPPER itself, FINESSE, and TTRX.
  - Handles run control commands: “RUN-START” / “RUN-STOP” / “FATAL-CONDITION”, etc.
  - Etc.

RadiSys EPC-6315

- **EPC-6315 is regarded the standard CPU for the COPPER.**
- **Why EPC-6315?**
  - RadiSys EPC-6315 was the only commercially-available PrPMC (processor PMC) equipped with the Intel CPU when we started the COPPER R&D.
- **Specs:**
  - CPU: Intel PentiumIII 800 MHz
  - Memory: 256 MB.
  - The RJ-45 connector for the Ethernet.
  - RedHat Linux 7.3 or 9, or FedoraCore 1 Linux run on it.
  - Price: ~1,100 USD / module.

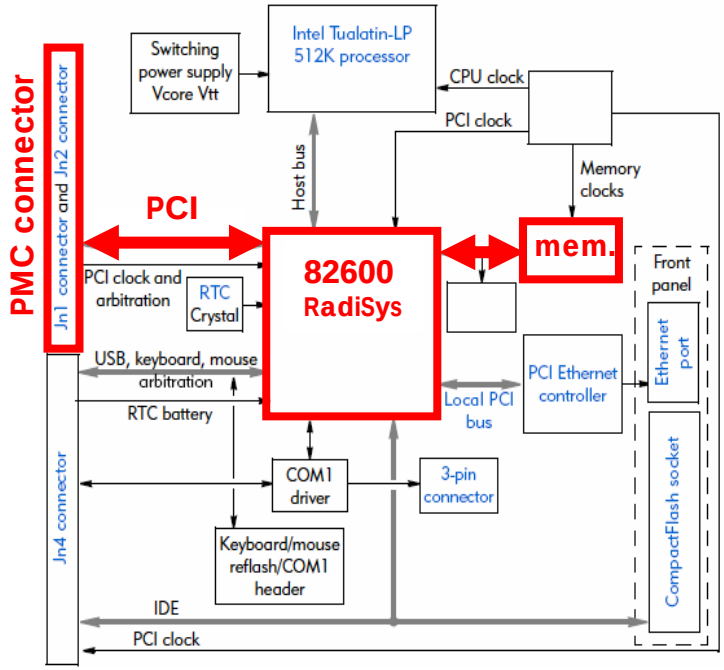


Bootable from CF card or from network.

Cons of the EPC-6315

- **The EPC-6315 is getting an out-of-date product; its prospect is not very promising.**
- **Chipset (RadiSys 82600) deteriorates the data transfer.**
  - PLX9054 → PMC memory
    - 112 Mbps (w/ DMA)
  - PLX9054 → EPC-6315 memory
    - 74 Mbps (w/ DMA)

The 82600 breaks data transfer every 32 bytes in the burst mode, which is the origin of the bottleneck. It cannot be disabled.



EPC-6315 block diagram

- **Also, we found that RadiSys was less professional in the customer communication…**

Other Possibilities of PrPMCs

M.Nakao

- **GE Fanuc PSL09 – new commercially available PrPMC**
  - CPU: Intel PentiumM 1.4 GHz.
  - Memory: 256 MB.
  - Price: ~2,000 USD / module.

Photo of PSL09 w/ heat sink removed

  - 10 COPPER-II's w/ PSL09 attached had been installed into the DAQ system and have been tested in the beam operation.
  - It is observed that they worked quite well. It can be one of the possible candidate of the next PrPMC.
  - I fairy have to say, we haven't examined if this PrPMC's chipset would be a bottleneck of the data transfer or not.

Other Possibilities of PrPMCs

- **Possibility of a custom CPU**
  - One Japanese company (Advanet) shows a strong interest to develop a new PrPMC.
  - According to their rough idea…
    - CPU: Intel Tolapai (code name) 600 MHz
      equivalent to PentiumM 900MHz.
    - Memory: 512MB-1GB.
    - R&D cost: ~100k USD.
    - Board price: ~1300 USD.
    - R&D will be finished within this fiscal year.

Looks a bit costly. We are to negotiate with them to find out the possible compromise.

- **We keep surveying any kind of better PrPMC.**

Summary

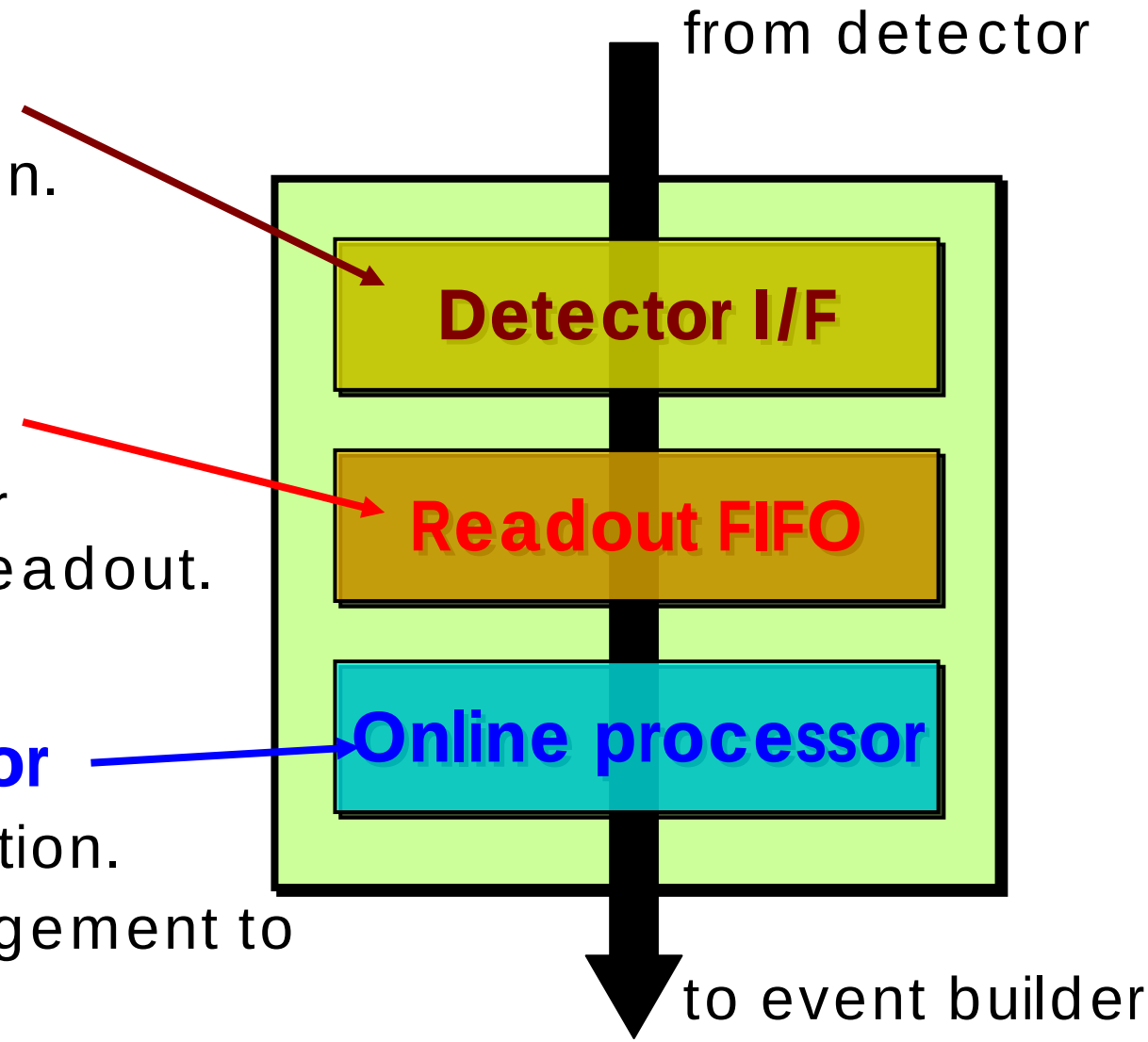
- The COPPER-II is to be upgraded to COPPER-3, which has 100% backward compatibility. Within this fiscal year, we will make it ready toward the mass production.

- Because of some problems, we are searching for the next PrPMC with which the RadiSys's EPC-6315 is replaced. Good performance of the GE Fanuc's PSL09 is proved in the beam operation; the PSL09 is one of the candidates. Beside that, we are searching for possibility of the custom PrPMC.

Backup Slides

Readout Electronics Overview

- **Detector I/F**
  - Signal digitization.
  - L1 pipeline.
- **Readout FIFO**
  - Event buffers for asynchronous readout.
- **Online processor**
  - Data size reduction.
  - Data link management to event builder.



Design Concept

- **Modules**
  - Detector I/F
    - User defined cards for analog part only, minimizing the R&D cost.
  - Data reduction CPU
    - Commercially available PMC module, no hardware development cost.

Low Cost Design

- **Common platform**
  - DAQ software can be generalized.

Profile of CPU Usage

@ 416 bytes/ev/ADC-module

- **User time: ~2%**
- **System time: ~20%**
- **Idle time: ~78% = CPU power that is equivalent to P3 ~600MHz is still available**

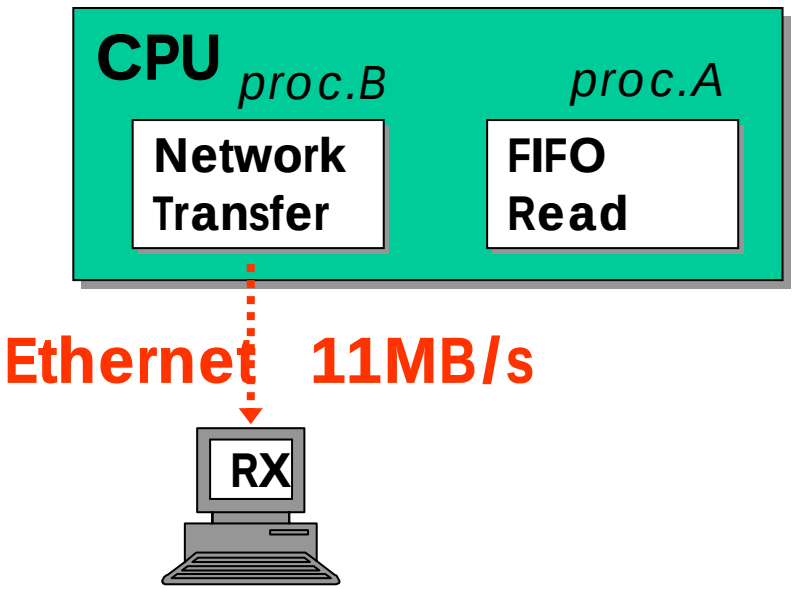
- **Large idle time fraction indicates the PCI bus works at the full performance.**
  - 416 bytes / ADC-module / ev × 40 kHz × 4 ADC modules = **67 MB/s**.

Performance Degradation by Network Use

@ 416 bytes/ev/ADC-module

CPU user time: ~2%
CPU system time: ~20%
CPU idle time: ~78%

Maximum accepted trigger rate: 40 kHz



CPU user time: ~5%
CPU system time: ~31%
CPU idle time: ~64%

Maximum accepted trigger rate: 32 kHz

Still works well.