DAQ Overview

R.Itoh, KEK

Target performance and requirements

- Expected luminosity @ SuperKEKB ~ 2.0 x $10^{35}/cm^2/sec$ (first stage)

- Keep the same L1 trigger policy as that of Belle

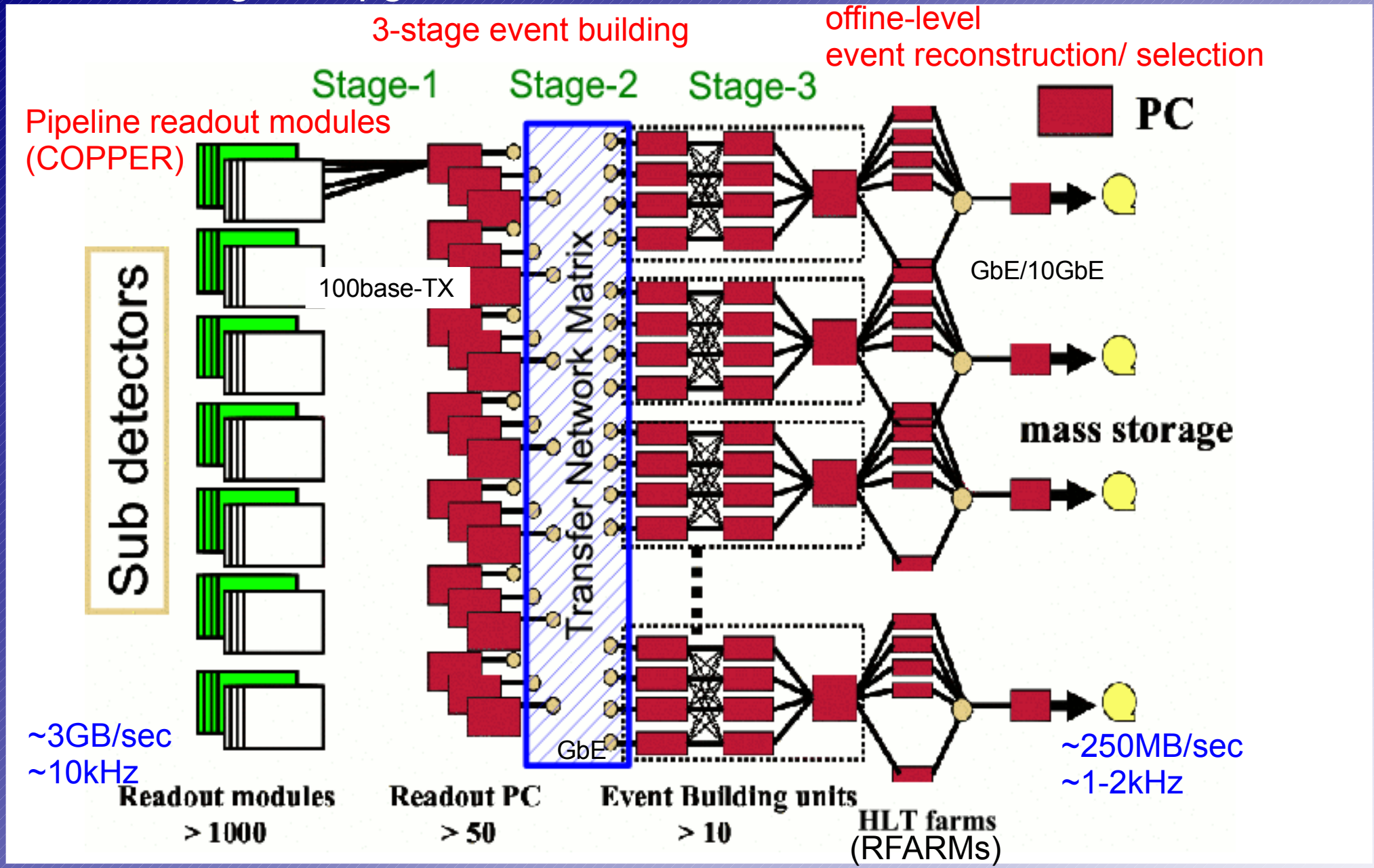
	Current Belle	Upgraded KEKB
Typical L1 rate	0.5kHz	10kHz
(Maximum L1 rate	~1kHz	~30kHz)
L1 data size(in)	40kB/ev	300kB/ev
flow rate(in)	20MB/sec	3GB/sec
reduction	1	1/3
data size(out)	40kB/ev	100kB/ev
flow rate(out)	20MB/sec	1GB/sec
L3+HLT reduction	1/2	~1/10
Storage badwidth	20MB/sec (including full rec. results by RFARM)	250MB/sec

*** Powerful data reduction at each step is the key.**

Note: Pixel readout is not taken into account in this estimation

Global design of upgraded DAQ

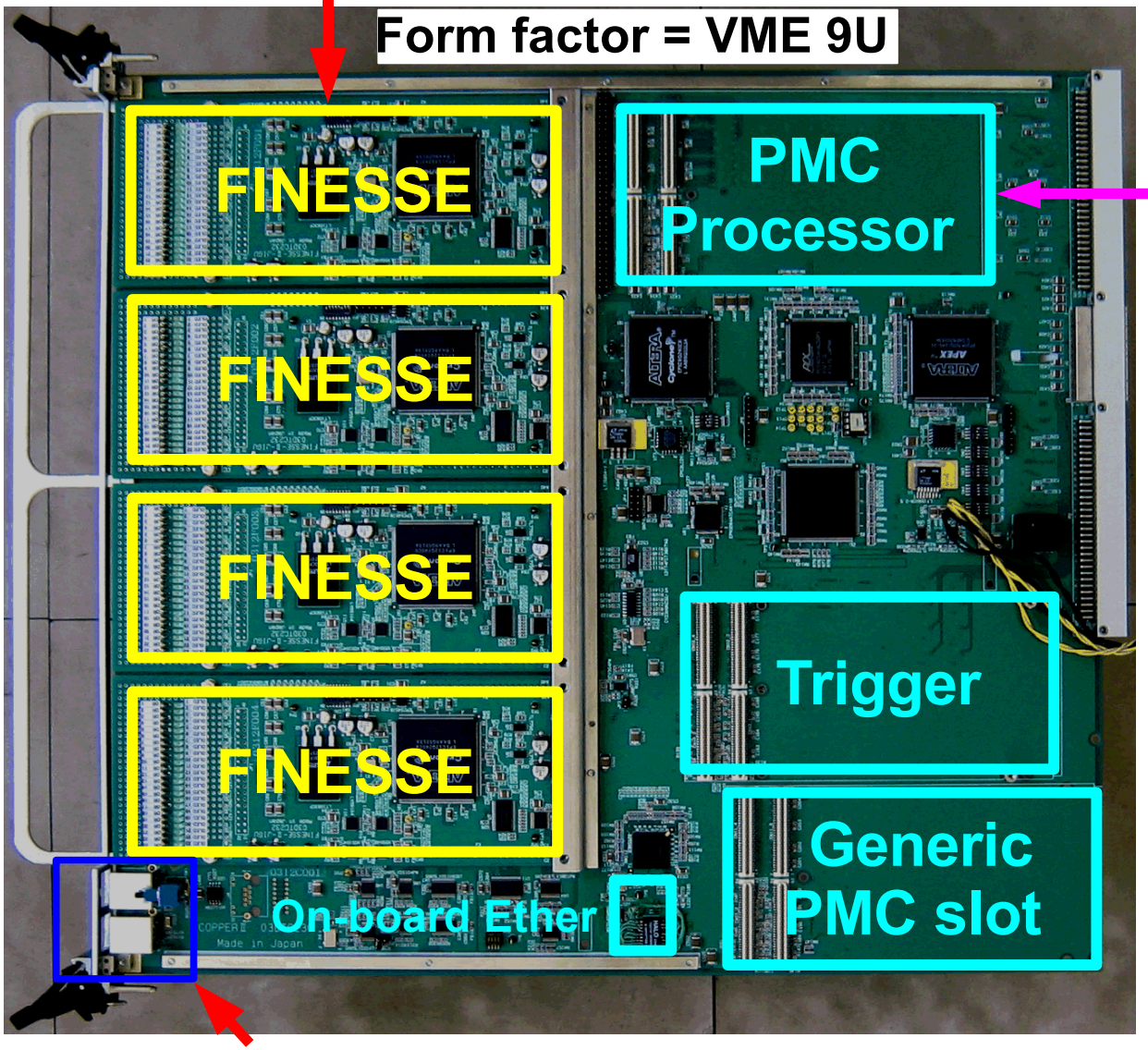
"Smooth" upgrade from existing DAQ



* We will keep using current data flow/control software for down stream after COPPERs to minimize new developments

Unified Pipeline Readout Module (COPPER)

Digitizer cards (implemented as daughter cards)



two100base-TX ports
(for control and data flow)

CPU card
(operated by Linux)

RadiSys
EPC-6315

- **Intel PentiumIII 800 MHz** w/ **256 MB memory**.
- Network booted
- RedHat Linux 9

GE-FANUC
PSL-09
- Intel PentiumM 1.4GHz

Digitizers and Front-end readout

- Belle's signal digitizing : Unified scheme (except for SVD)
  = Q-to-T + multihit TDC
  all placed in E-hut

SuperKEKB : different digitizers for different detectors

SVD: APV25 readout placed in E-hut
CDC: ASD-chip based readout located near detector
PID: Special ASIC located near detector
ECL: Wave-form sampling digitizer located near detector
KLM: not yet decided
PXL: no info for now

** Most of detector groups are planning to place front-end electronics including digitizers near detector.*

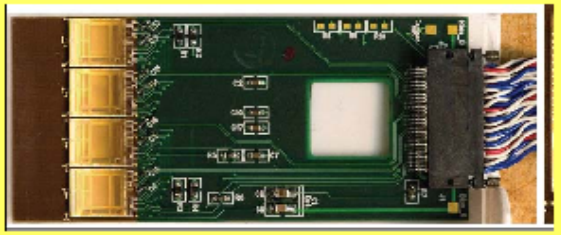
- DAQ group's idea :
  Use COPPERs as “unified readout modules” between digitizers and event builder units.

Readout scheme of each detector

1. SVD
   - APV25 based readout. The design is already fixed as a part of SVD3.
   - FINESSE interface is also designed. Prototype available. (parallel data transfer over metal wires)

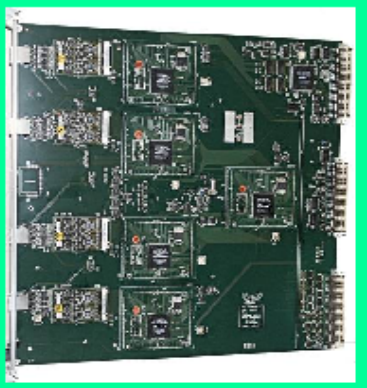
- We have been working to prepare Pipeline readout sensor module for SVD3

Hybrid card with 4 APV25 chips
Operated with 40MHz clock (Princeton)

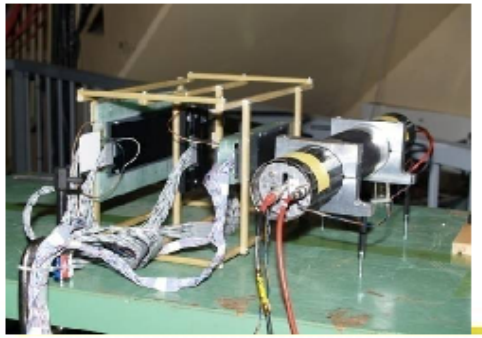


FADC: 40MHz digitization
Online sparsification with FPGA

(Vienna)



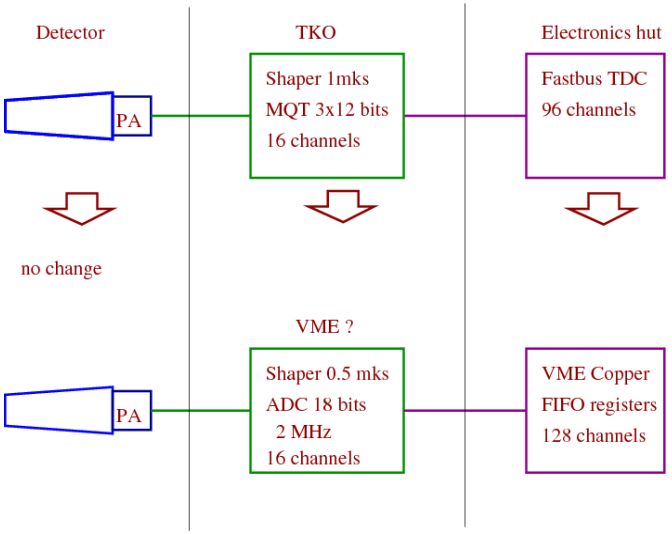
Beamtest done in KEK in Nov 2007
in KEK Fuji testbeam line 3GeV electron



Confirm the capability of
online sparsification algorithm
The result will come soon

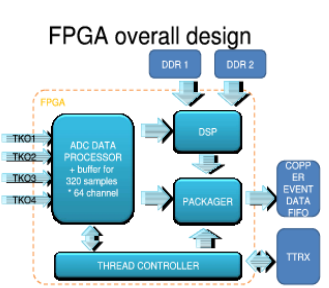
2. ECL

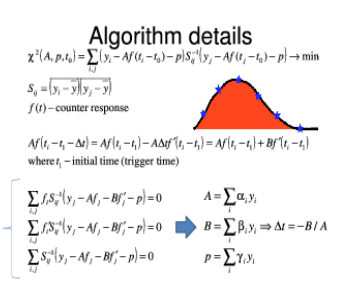
Electronics modification(barrel)

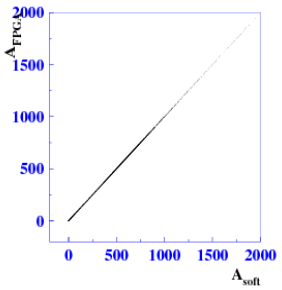


FINESSE status

- HOSHIN produced 16-channel FINNESE in March 2006.
- Tandem 64-channel FINNESE was developed and two modules has been produced in HOSHIN.
- The algorithm of energy and time reconstruction was implemented.



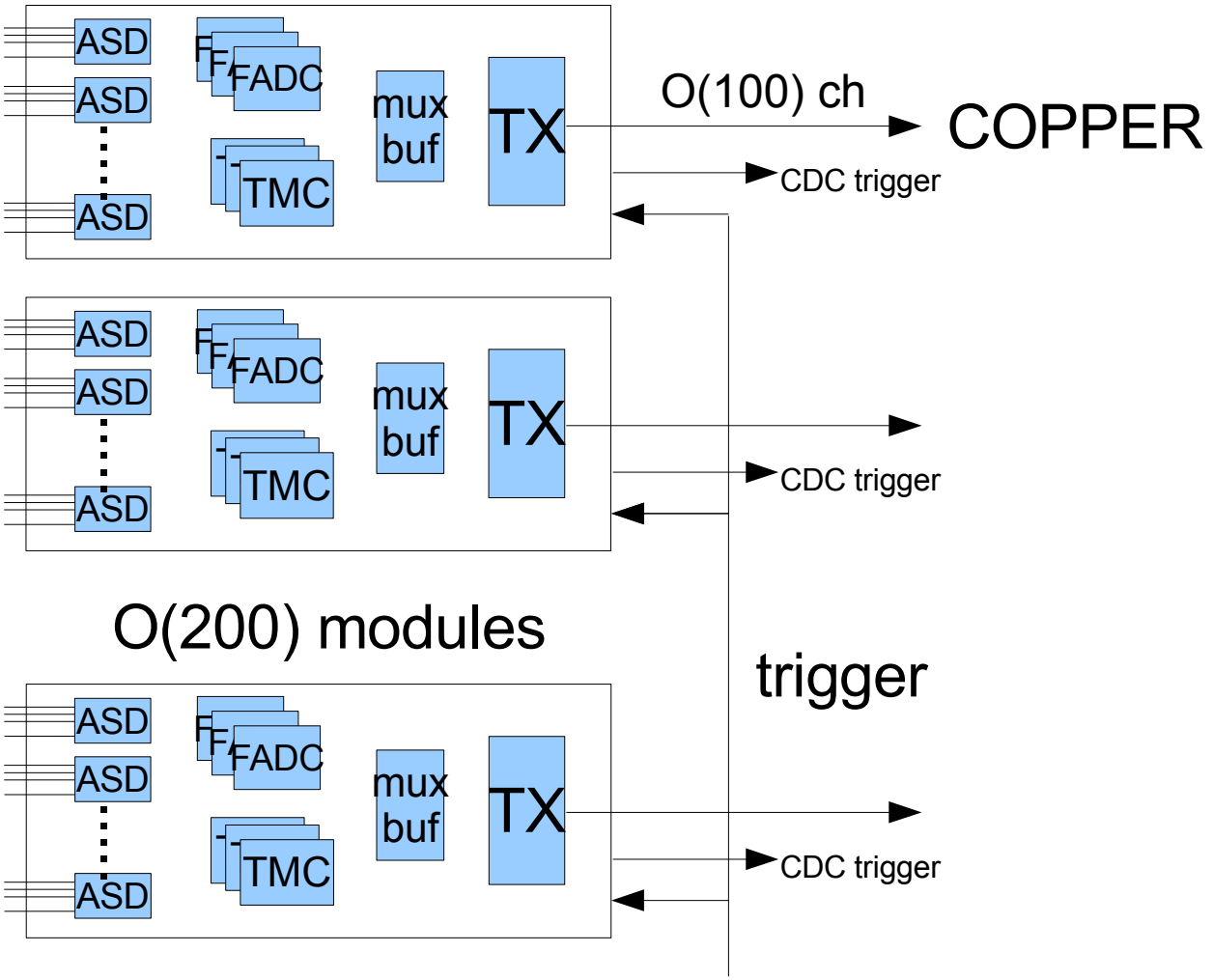




- The algorithm gives the same results as software calculations

* Prototype of new frontend + digitizers + FINESSE is available
* “Feature extraction” of wave form is performed on FINESSE.
  -> difficult to move to unified data transfer scheme.....
* But they need to span huge number of cables.
  -> they are asking the possibility to place COPPER-VME crate near detector. <- DAQ group cannot manage!

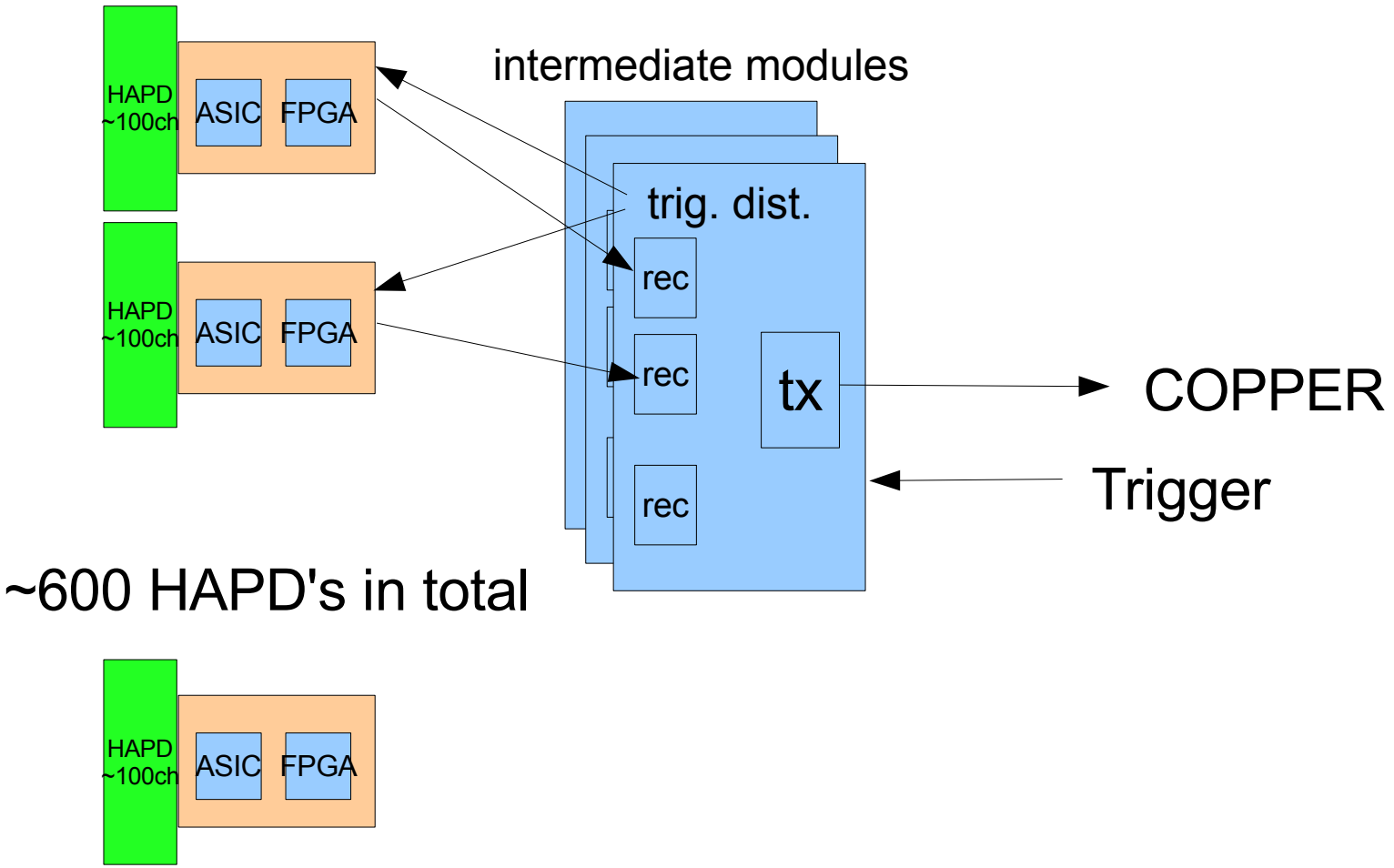
3. CDC



- Still at the conceptual design stage
- Readout boards are placed on the end-plate
  -> special form factor?

4. PID

ex. A-RICH



~600 HAPD's in total

TOP can be similar. iTOP??

5. KLM

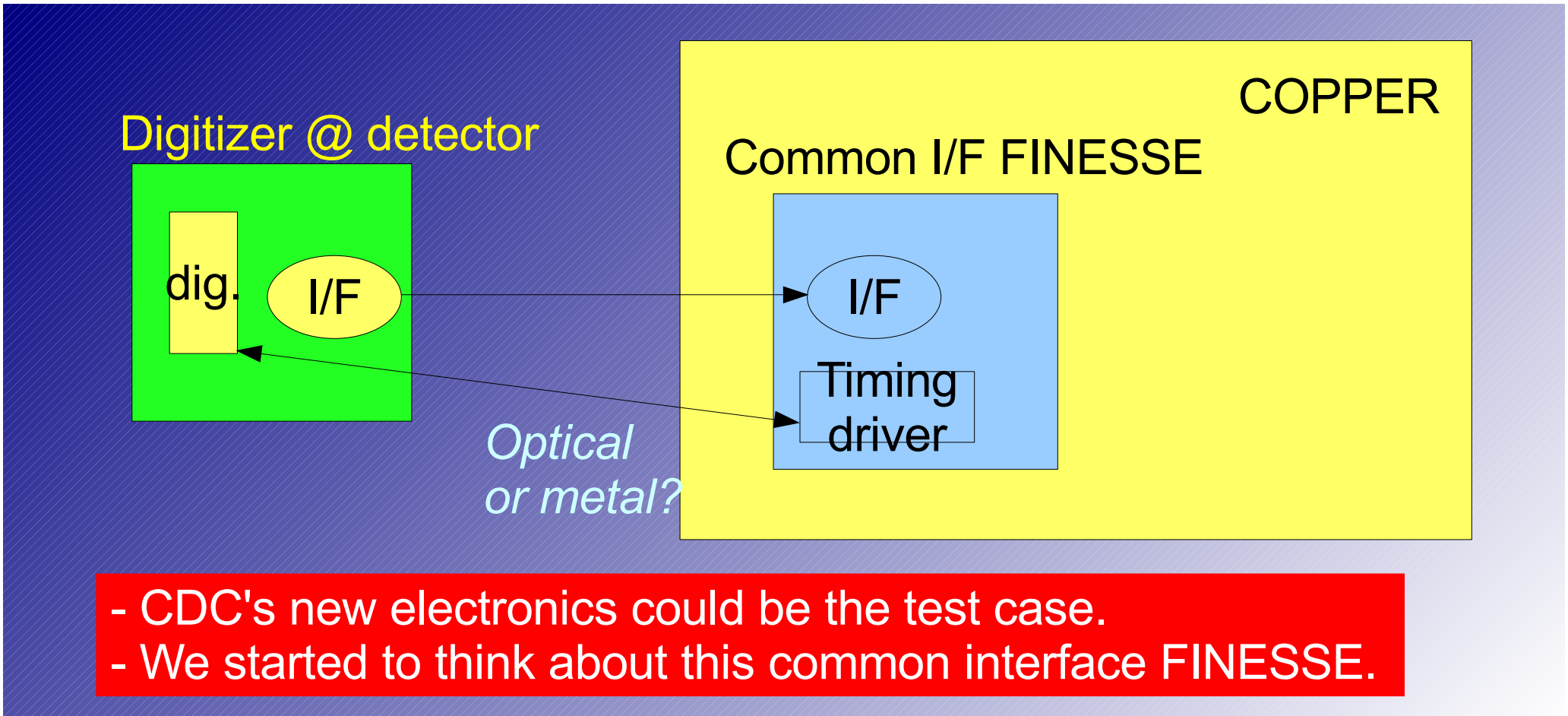
- Barrel : current plan is to recycle current readout electronics
  with COPPER-TDCs
  (In case of RPCs are used)

- Endcap : possibility of new readout if scintillation tile is adopted.
  -> could be similar to A-RICH.

Idea of common interface FINESSE

- It is desired to prepare a common interface FINESSE to connect external digitizers.

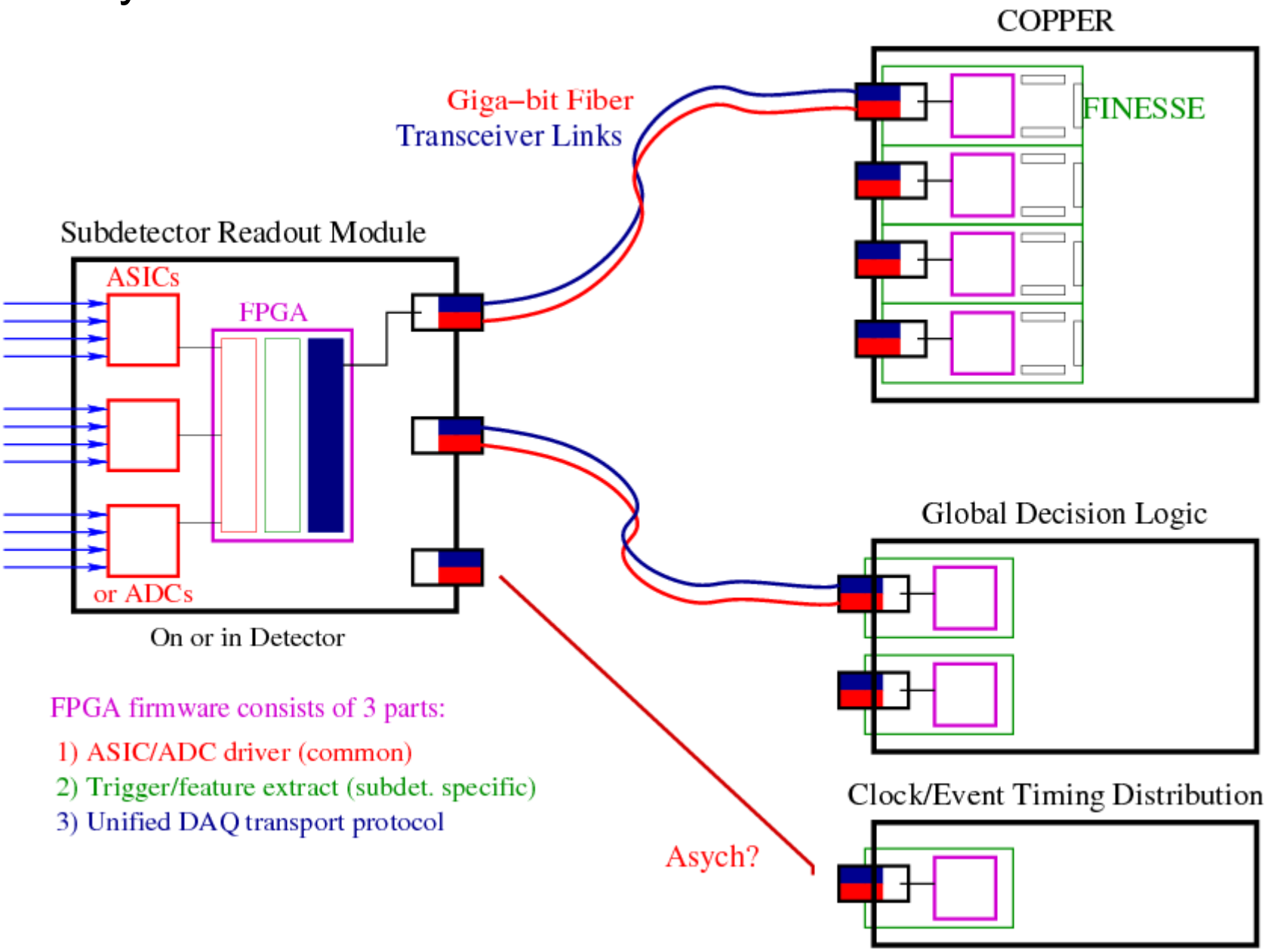
- Need to develop
  * timing distribution scheme (over long cables)
  * standard data transfer protocol



- CDC's new electronics could be the test case.
- We started to think about this common interface FINESSE.

Unification of readout scheme

Proposal by G.Varner



Several different aspects

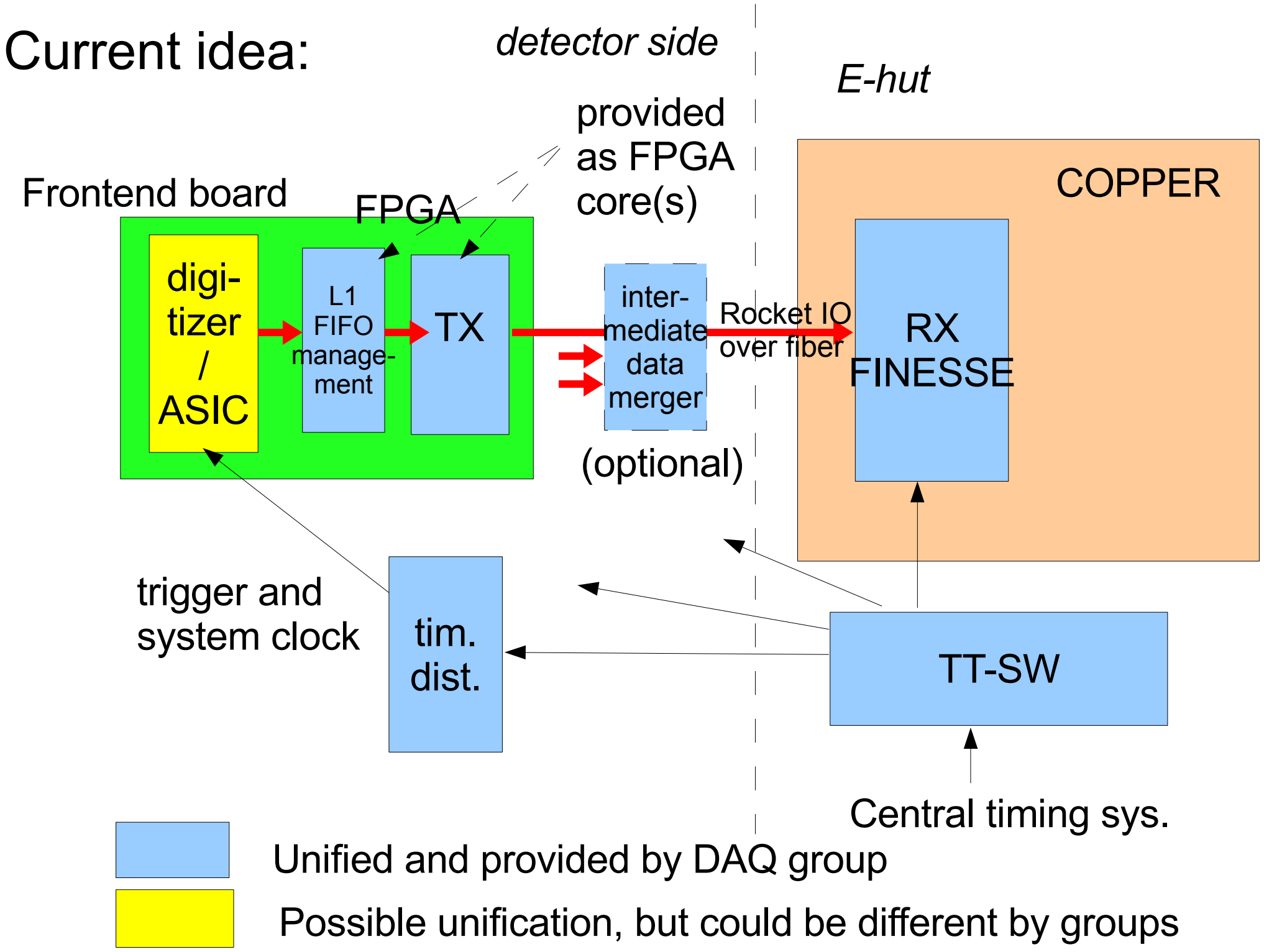
1. Unification of digitizers
    * Digitizer: ASIC, FADC, TDC, etc.
    * Unified L1 buffer handling

2. Unification of data transfer to COPPER
    * Protocol : Rocket IO, SiTCP, ...

3. Trigger distribution and handshake
    * Extension of TT-RX scheme : event-by-event sync.
    * Fully asynchronous (free running mode)

4. Unification of subtrigger signal collection
    * Rocket IO based communication

Trigger part


Current idea:
detector side
E-hut
provided as FPGA core(s)
Frontend board
FPGA
digi-tizer / ASIC
L1 FIFO manage-ment
TX
inter-mediate data merger
(optional)
Rocket IO over fiber
COPPER
RX FINESSE
trigger and system clock
tim. dist.
TT-SW
Central timing sys.
Unified and provided by DAQ group
Possible unification, but could be different by groups

Status

- All detector subgroups (except PXD) agreed on
  1) COPPER is used as the common readout module for all frontend electronics.
  2) A common device (TX and RX) is used for the data transfer between frontend electronics and COPPERs

* SVD and ECL groups already had their own designs for the data transfer
  -> they are flexible to change their design to meet with this common readout scheme.

* COPPER design is revised for the “sustainability” beyond 2010.
  - Use of “sustainable” FPGA chips as possible.
  - Minor upgrades:
    * Faster CPU cards
    * GbE interface <- 100baseT

Current issues:

- Under discussion on
  1) Unified treatment of digitizers -> Gary's talk
  2) The design of
     - data transfer protocol
     - timing distribution and handshake
       -> Nakao-san's talk
     <- feed back from BES III experience -> Liu-san's talk

- On going : COPPER revision -> Higuchi-san's talk

- Not discussed yet:
  * Asynchronous (free running) DAQ
  * Renovation of event building software, etc.

Discussions

1. Unification of digitizers
   - G.Varner is curently trying to keep in touch with each detector subgroup to pursue this possibility.
   - How realistic? Impression by each detector subgroup is helpful.

2. Inclusion on Pixel detector
   - Huge! data size is expected (~MB/event order!!!)
   - Possibility of data size reduction at frontend -> How much?
   - Manageable by COPPER strategy?
   - COPPER CPUs are useful for the further data reduction?