- I would like to thank Prof. Y. Sakai and Dr. Y. Iwasaki for their kind help in BESIII trigger design, and I am happy that we have this chance to share our experience of BESIII in KEKB Trigger and DAQ design.

High Speed Signal/Data Transmission in BESIII Trigger and PANDA TDAQ Systems

Zhen'An LIU
Trigger Group, IHEP Beijing

2nd Open meeting for the KEKB proto-collaboration
July 3-4th 2008

Outline

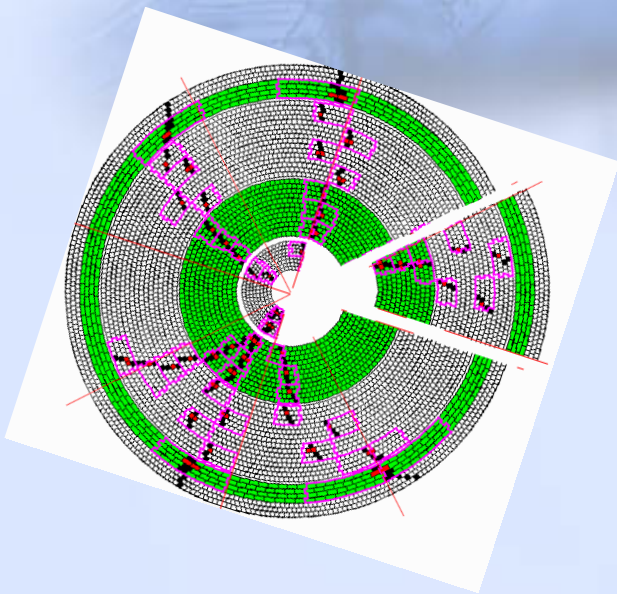
- **Background infor for BESIII trigger**
- **Study of High speed signal transmission in BESIII trigger**
- **BESIII trigger**
- **PANDA TDAQ**
- **Computer Node**
- **Proof of Concept Application: HADES DAQ Upgrade**
- **Comments and conclusion**

Key points in BESIII trigger Design

- Optical isolation with FEE, to prevent from ground loop current interference
- Most latest FPGAs, Boards with simplicity, high reliability
- FPGA online downloadable via VME
- Generalized hardware, firmware for different function, for easy maintenance
- Scheme optimization with simulation

Difficulties for MDC tracking

	1	2	3	4	
SL 1	40	44	48	56	/16
SL 2	64	72	80	80	/16
SL 3	76	76	88	88	/8
SL 4	100	100	112	112	/16
SL 5	128	128	128	128	/16
SL10	128/256	128/256	128/256	128/256	/16



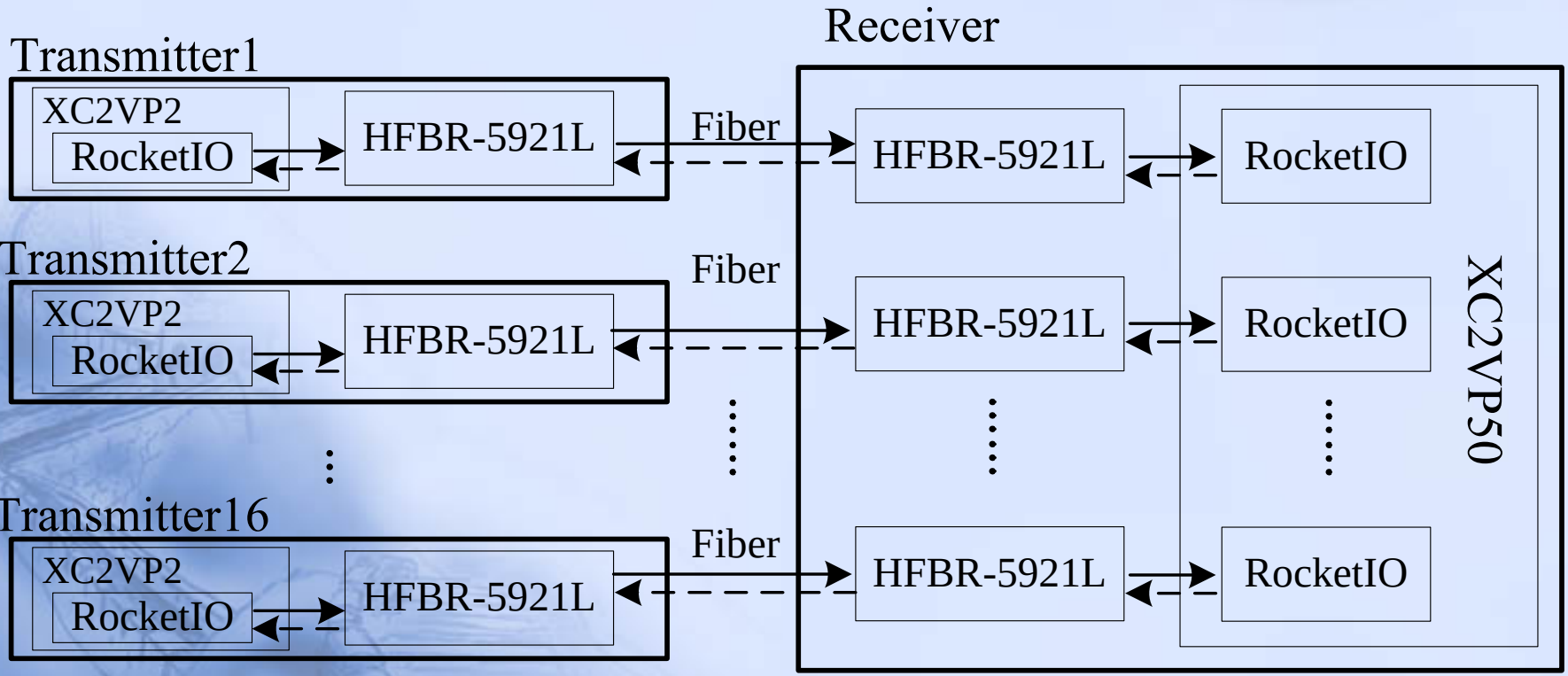
Difficulties

- **Bad number of wires for both axial and stero layers (trigger point of view, Hard to define Sector/board border for signal input)**
- **Hard to input signals via 9U front and rare pannels**
- **Too many sharing signals for neighbor boards**

Solution:

- **RocketIO for input signals (**32bits/ch, 8b/10b**)**
- **private VME J3 Backplane for sharing signals**

Study of High speed signal transmission in BESIII trigger



MFT (MDC Fiber Transmitter)

- 2796 hits signals from MDC QT boards are collected in MFT, 32 channels per MFT
- Virtex-II Pro FPGA: XC2VP2
- Fuctions:
  - Stretching to 500ns
  - Synchronization + alignment signals(private Protocol)
  - Serialization(8b/10b)

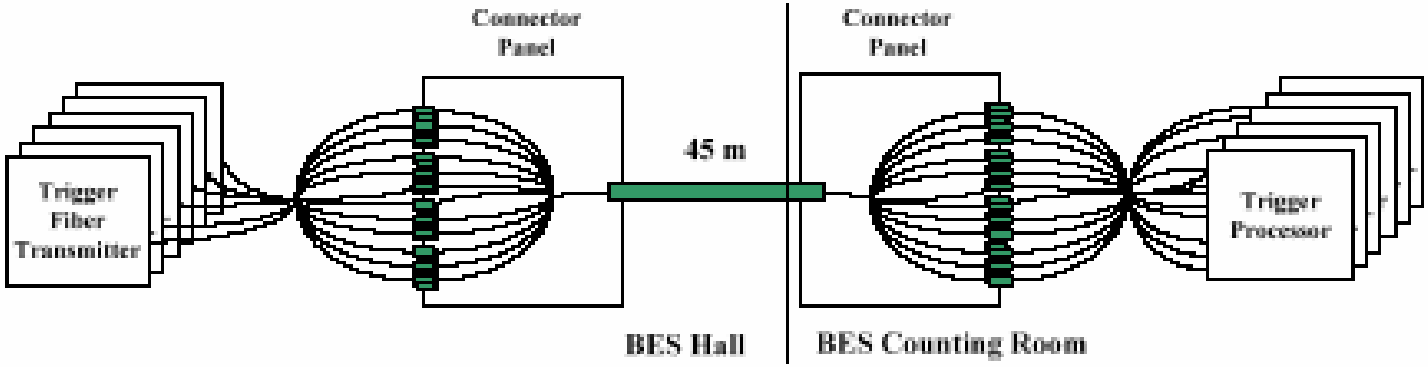


Fig.2. Organization of the optical link

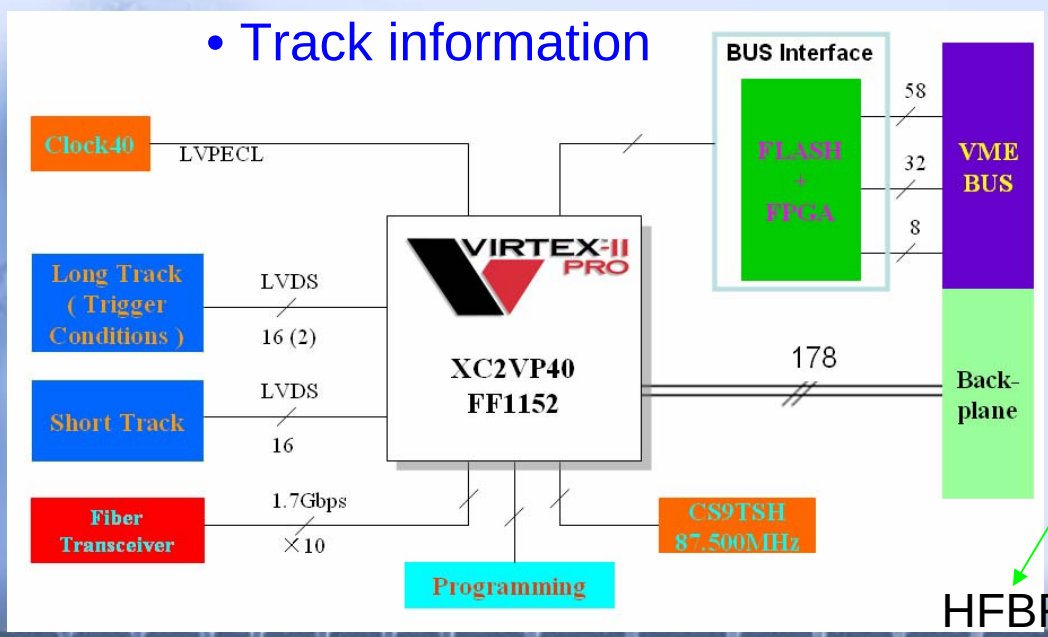
TKF (TracK Finder)

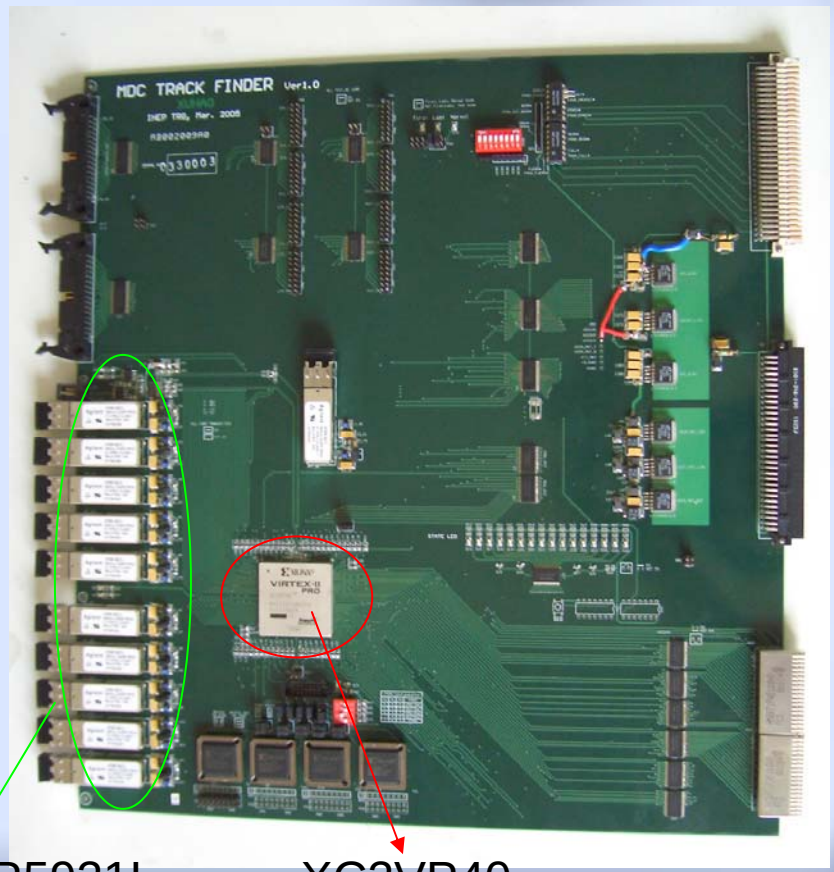
XC2VP40 : FF1152, 804 user IOs, 43,632 logic cells, 3,456Kbit BRAM, 12 RocketIOs, 2 PowerPCs, 192 multiplier blocks

10 layers 9UVME PCB

Functions:

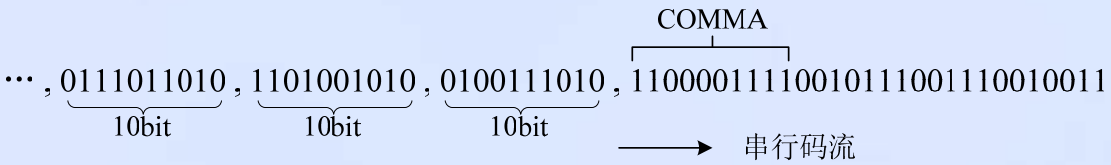
- Deserialization
- Channel alignment
- TSF
- TF
- Track information

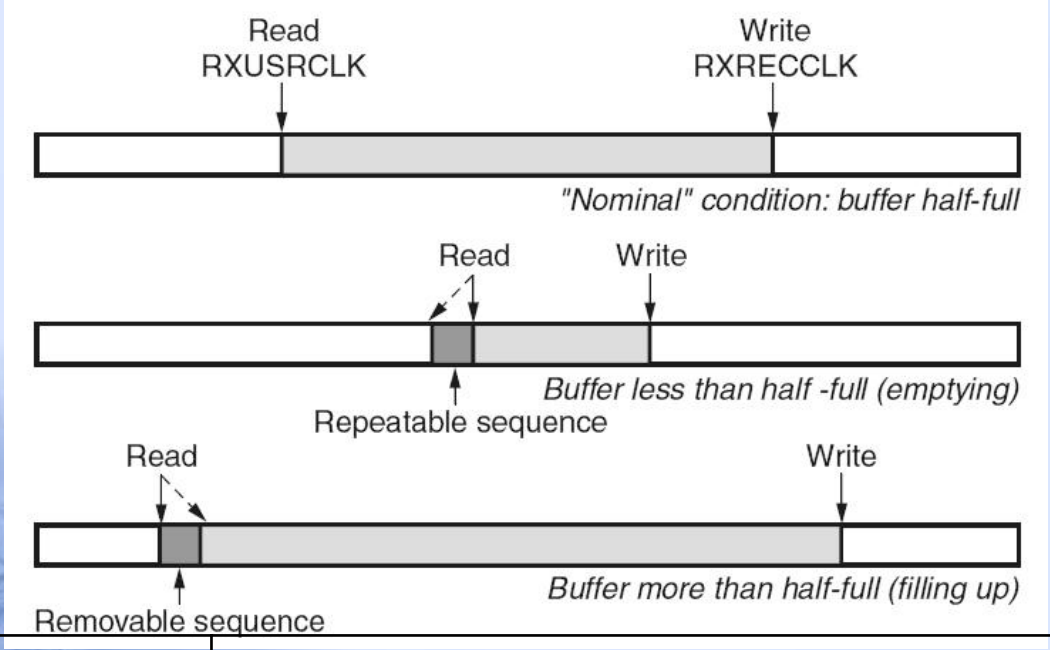




HFBR5921L XC2VP40

Clock correction



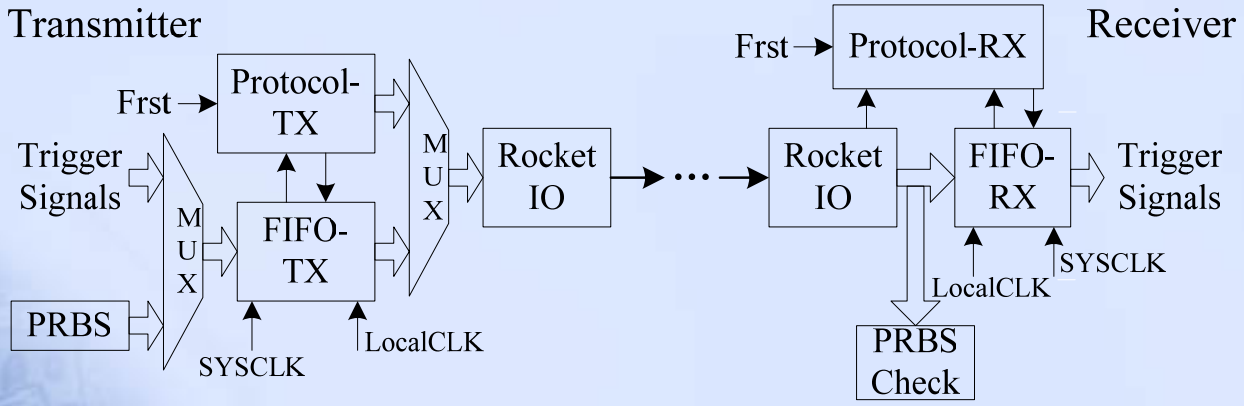


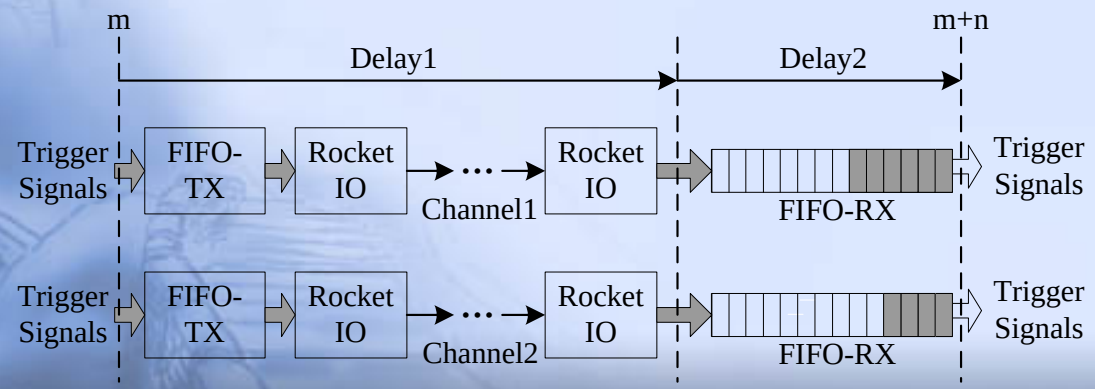
- K codes
  - COMMA
  - IDLE
- RXRECCLK
- RXUSRCLK

	Bytes Allowed Between Clock Correction Sequences			
REFCLK Stability	Remove1IDLE Sequences:	Remove2IDLE Sequences:	Remove3IDLE Sequences:	Remove4IDLE Sequences:
100 ppm	5,000(√)	10,000	15,000	20,000
50 ppm	10,000	20,000	30,000	40,000
20 ppm	25,000	50,000	75,000	100,000

Data alignment

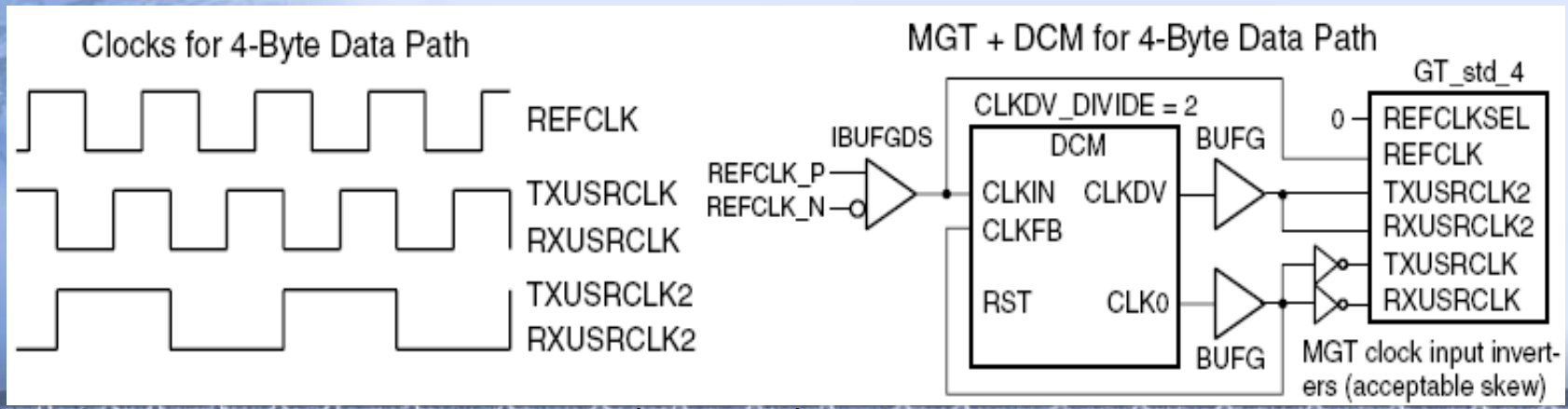
- Continuous
- Parallel bits transmitted in same clock => recovered also in same Clock
- Special private protocol





Clocks

- Crystal
  - Must follow the recommendation
- Use built-in DCM
- Clocks
  - REFCLK
  - USRCLK
  - USRCLK2

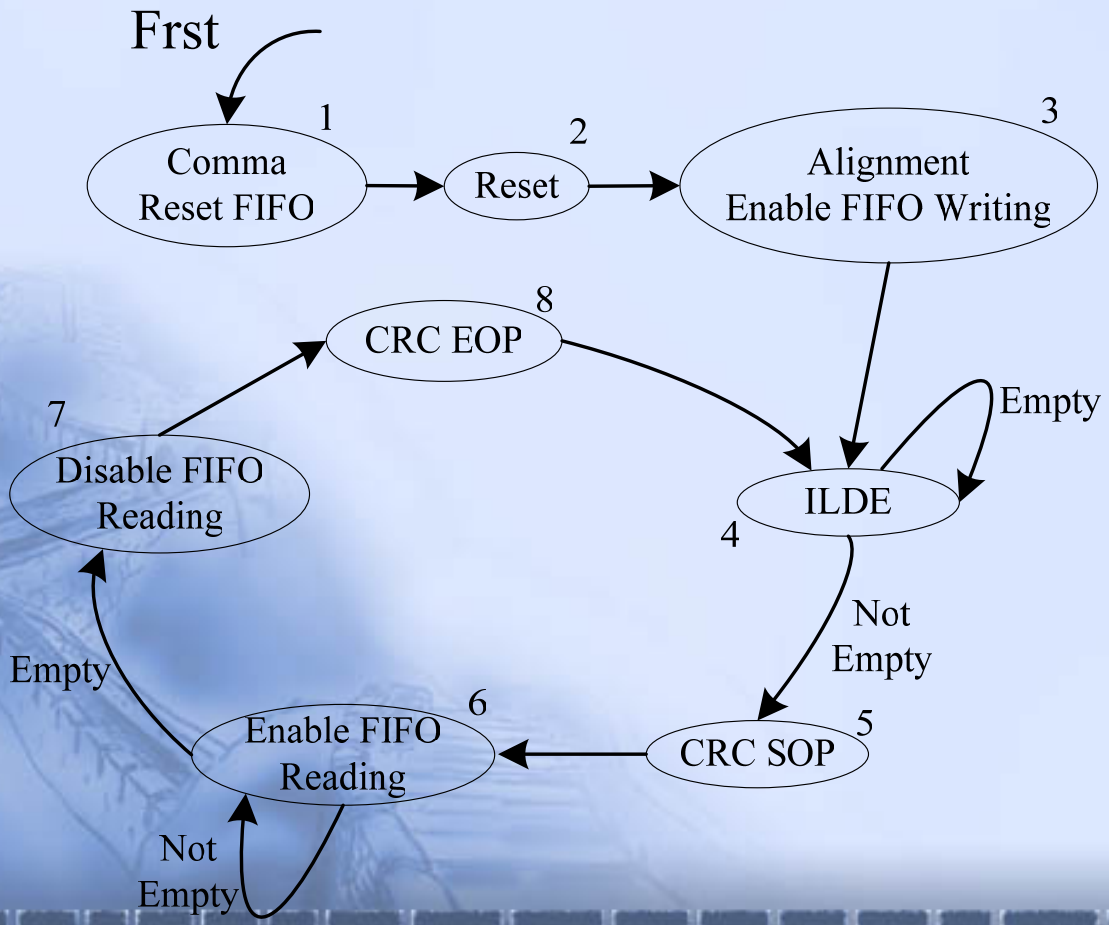


Example of RocketIO Instantiation

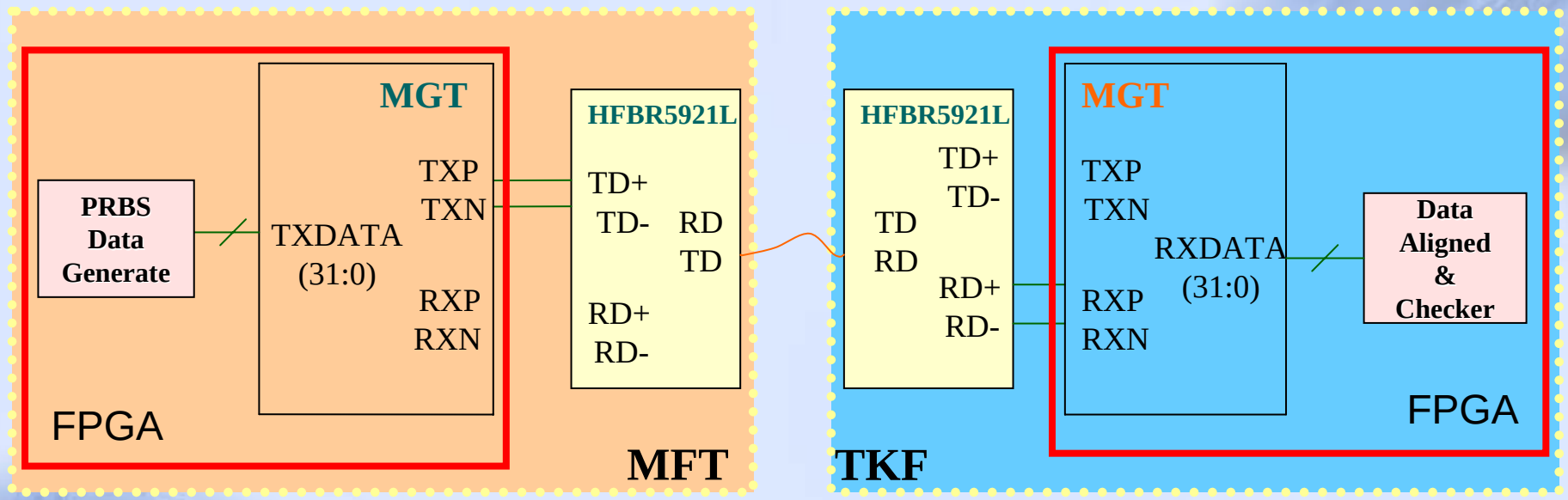
```
RocketIO_1 : GT_CUSTOM
  generic map(  CRC_END_OF_PKT => "K29_7",
                CRC_FORMAT => "USER_MODE",
                CRC_START_OF_PKT => "K27_7",
                TX_CRC_USE => TRUE,
                TX_DATA_WIDTH => 4,
                                                    …                    );
      port map (                    REFCLK=>REFCLK_IN,
          TXUSRCLK=>TXUSRCLK_IN,
          TXUSRCLK2=>TXUSRCLK2_IN,
          TXCHARISK(3 downto 0)=>TXCHARISK_IN(3 downto 0),
          TXDATA(31 downto 0)=>TXDATA_IN(31 downto 0),
          TXFORCECRCERR=>TXFORCECRC_IN,
          TXN=>TXN_OUT,
          TXP=>TXP_OUT,
                                                    …                    );
```

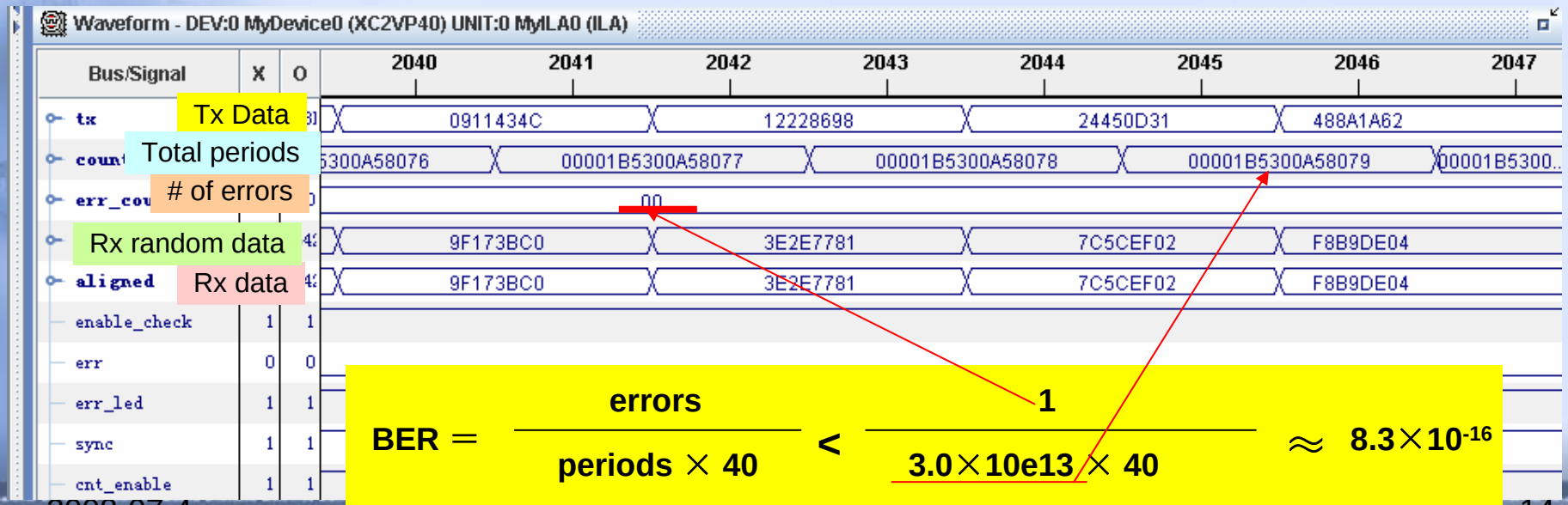
Transmission protocol

- Transmitter side
- Receiver side



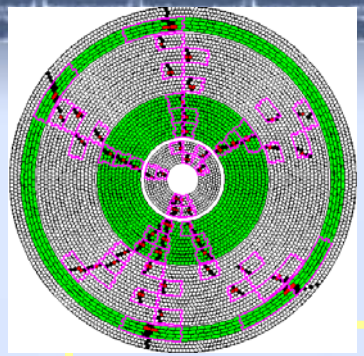
Good reliability with RocketIO

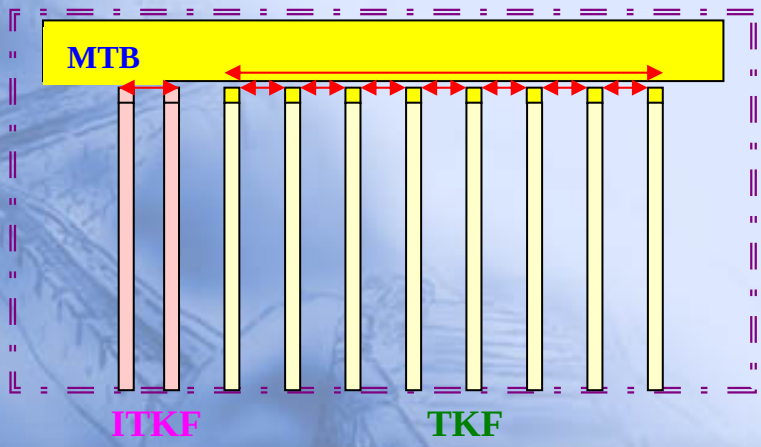




$$BER = \frac{errors}{periods \times 40} < \frac{1}{3.0\times10e13 \times 40} \approx 8.3\times10^{-16}$$

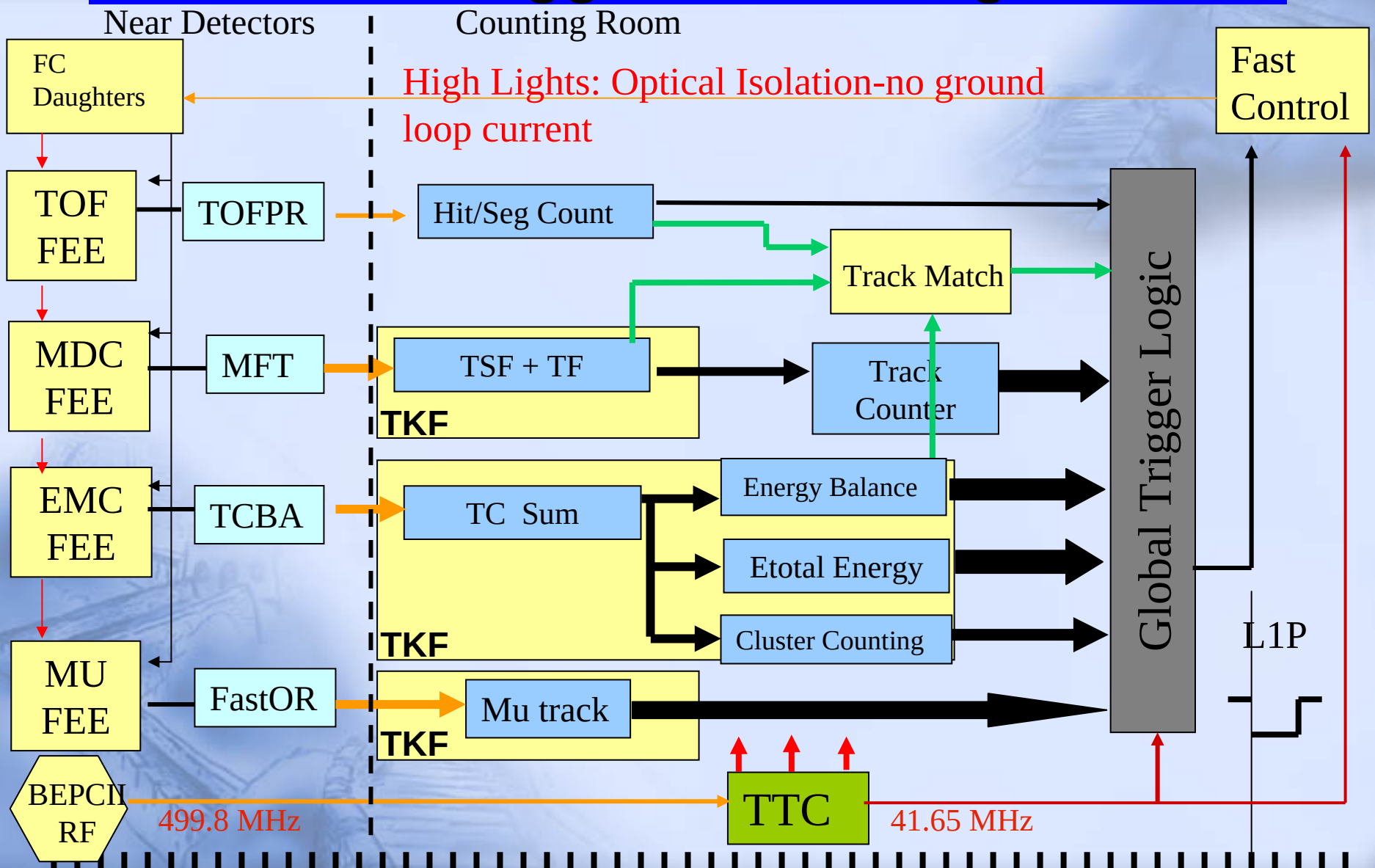
MDC Sub-Trigger





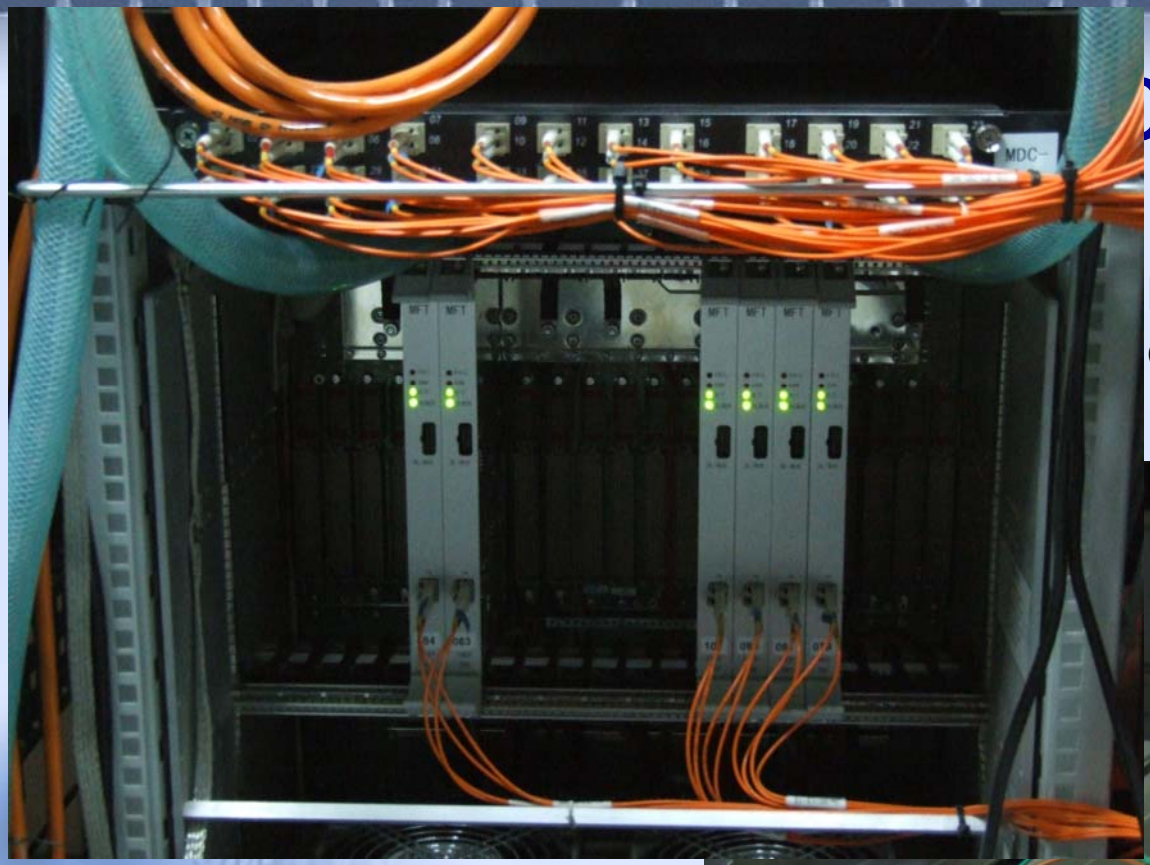
	Type of PCB	Board name	# of boards	FPGA firmware
MDC Fiber Transmitter	1	**MFT**	96	1
TracK Finder	1	**ITKF**	1	1
		TKF	8	8
TracK Counter	1	**LTKC**	1	1
		STKC	1	1
MDC Trigger Backplane	1	**MTB**	1	
Total	4	6	108	12

BESIII trigger Block diagram

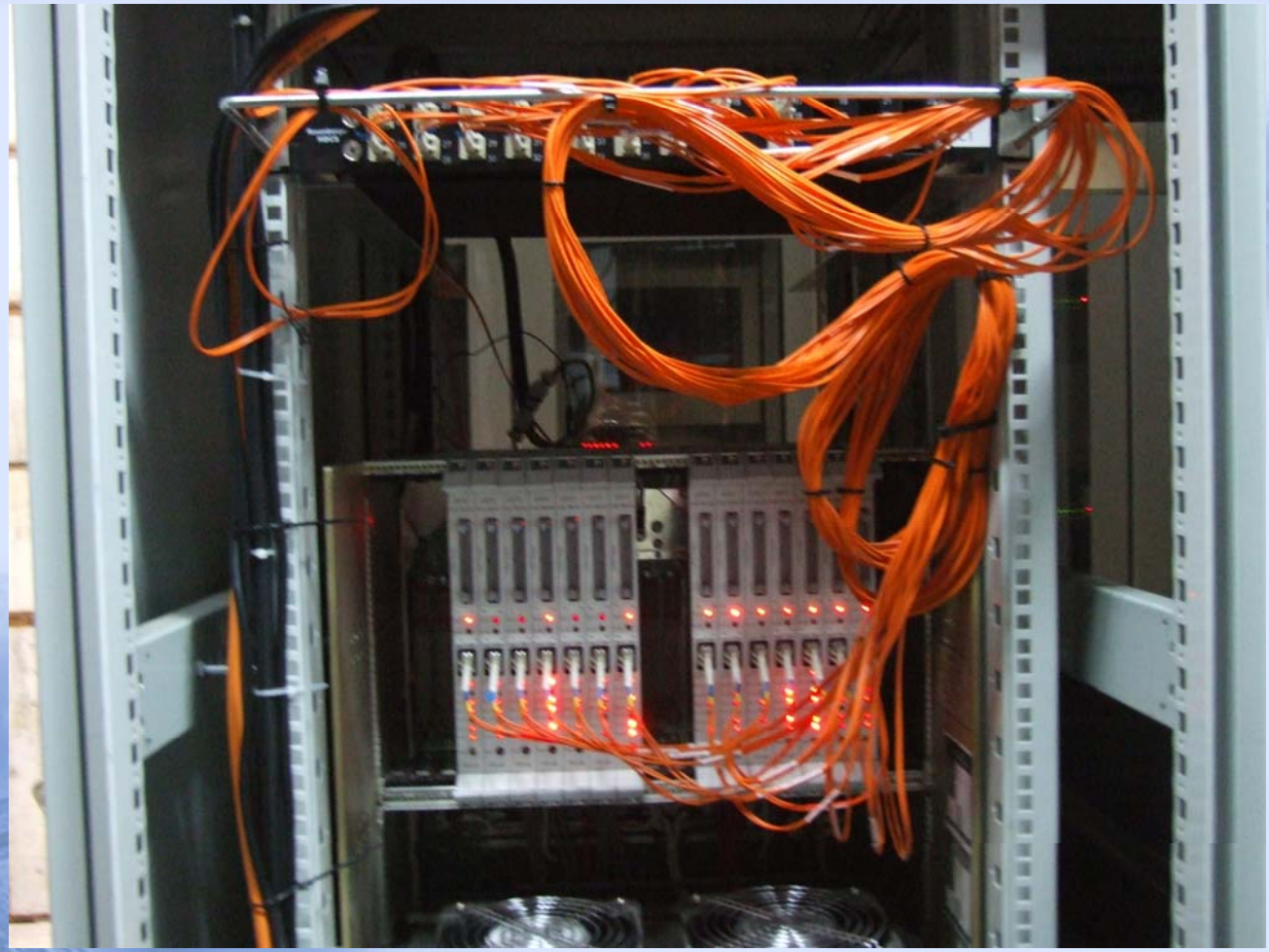


on

MFTs in FEE crate

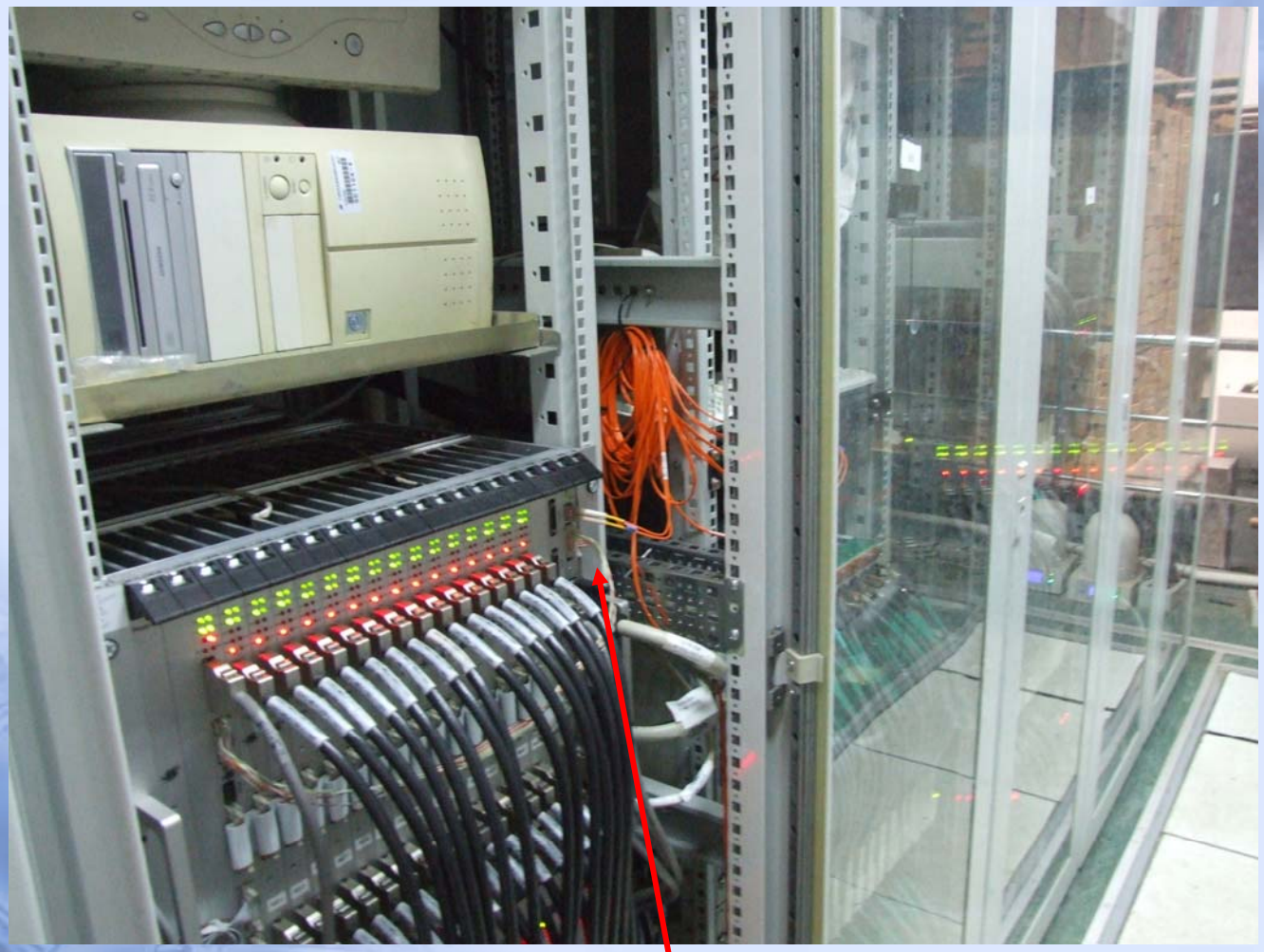


Jumper Box



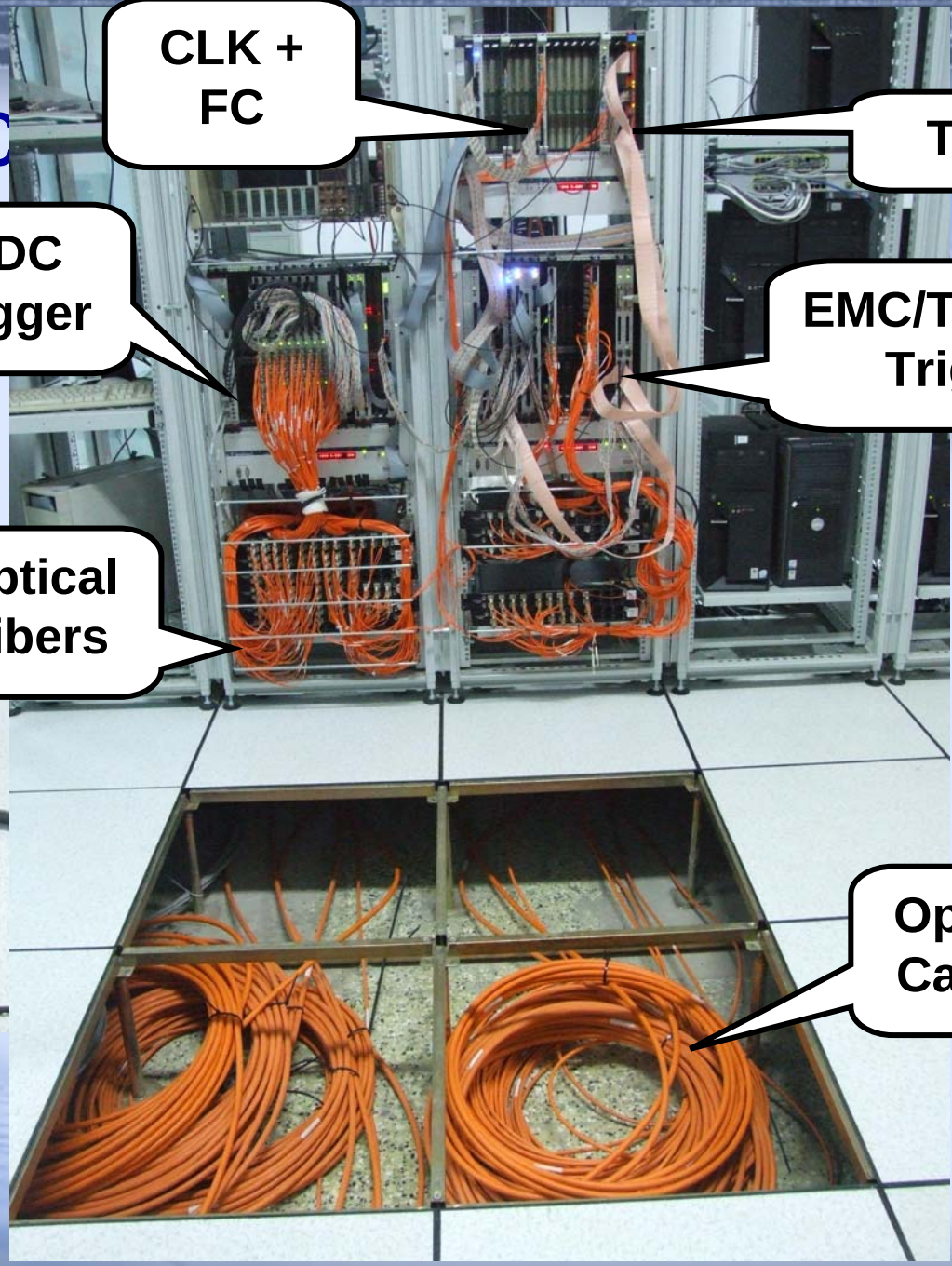
TOFPR

Installation



TCBA: EMC preprocessor and transmitter

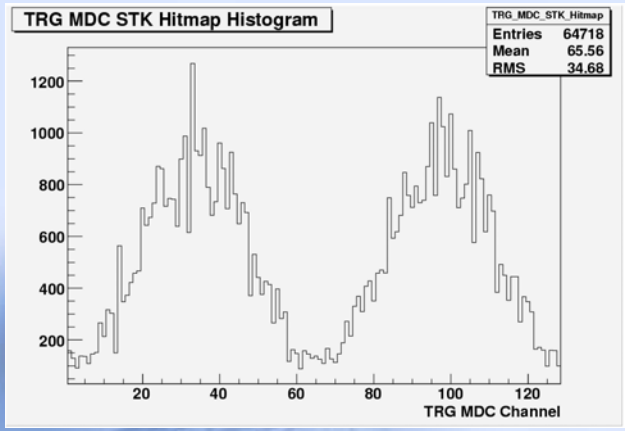
Installation c

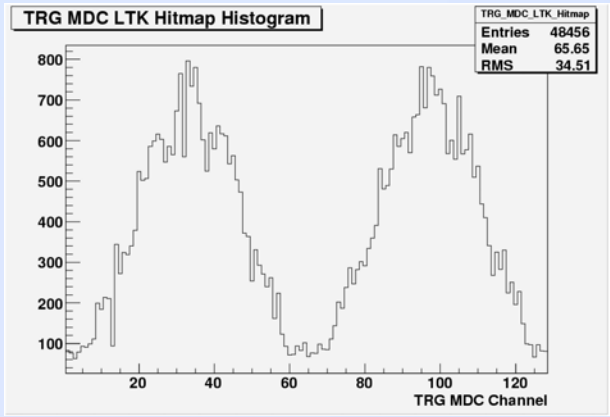


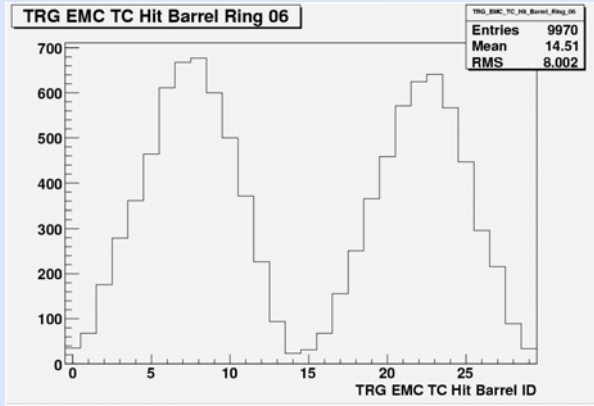
Opt-Cable under

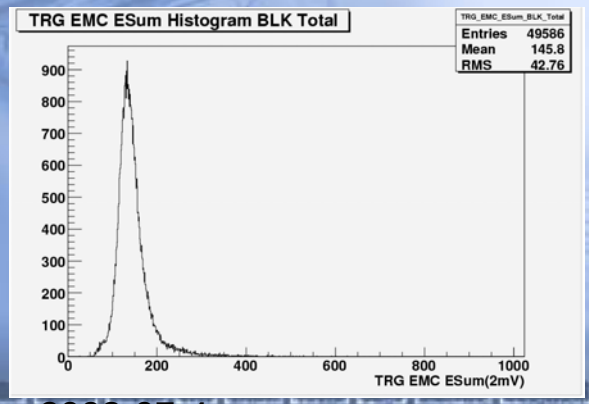
Status of BESIII trigger

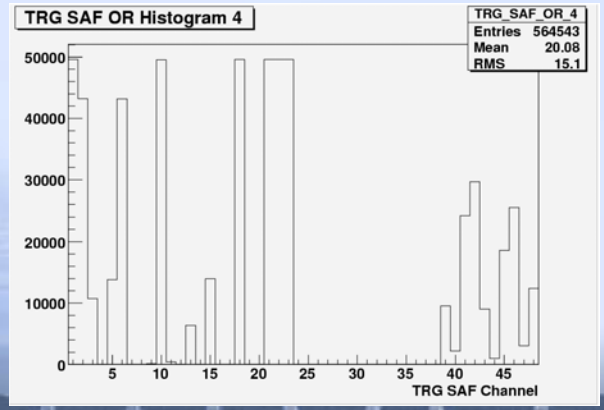
- Successful in Cosmic-ray test
- Commissioning with BEPCII

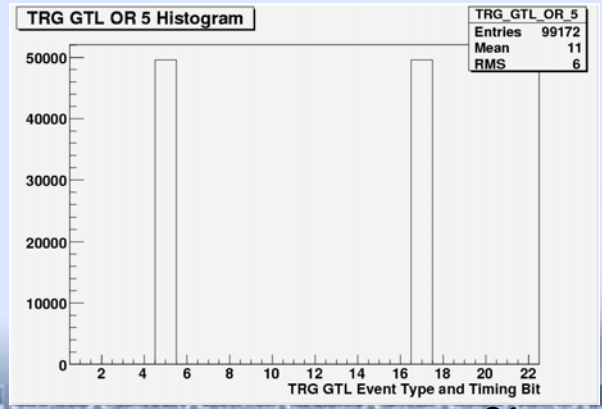








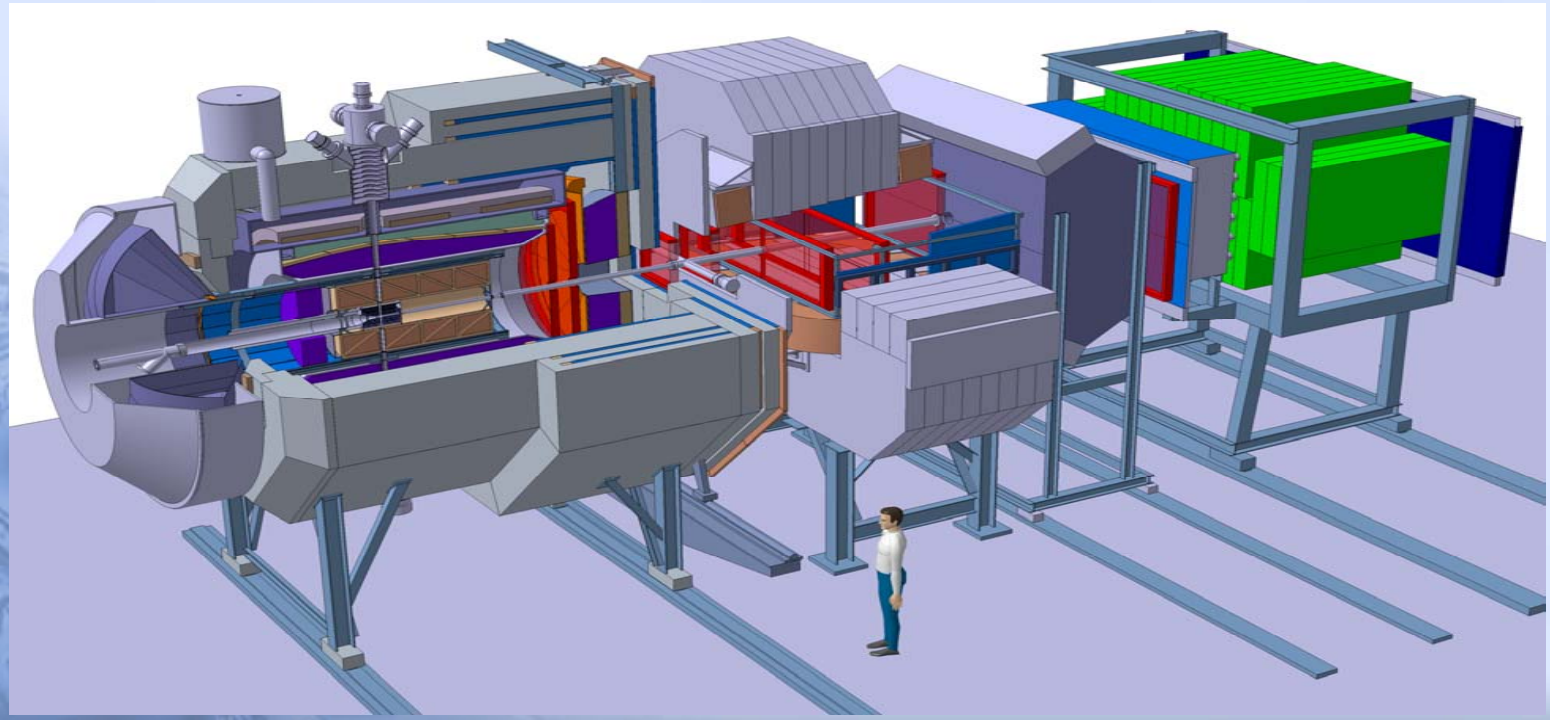




PANDA: DAQ Requirements

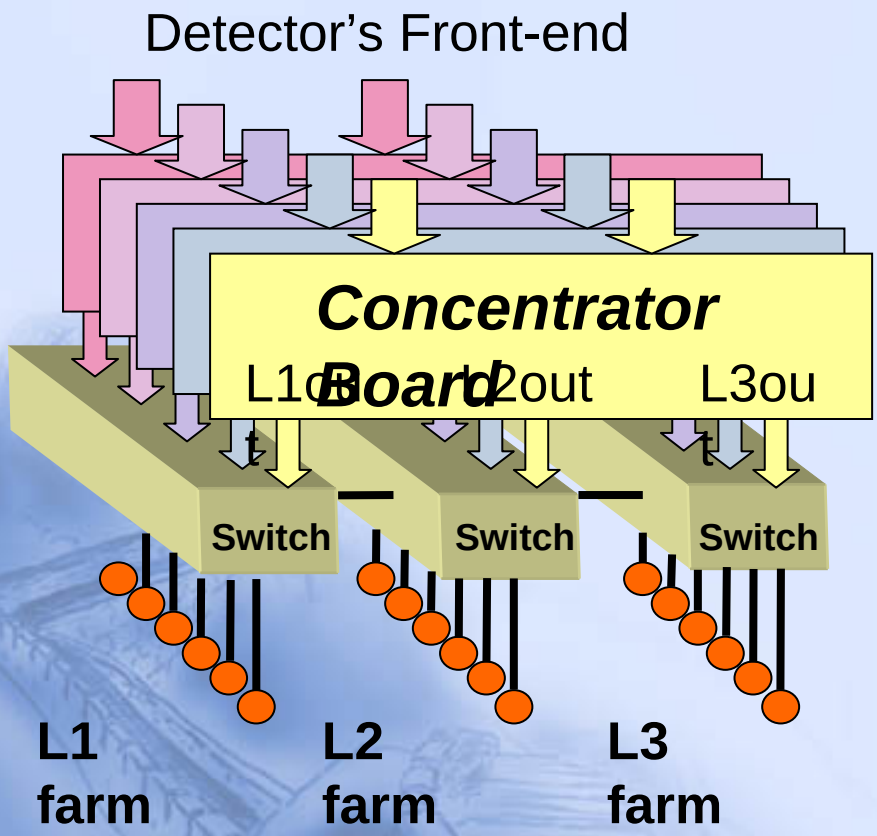
- Interactions: 10**7 Hz
- Data: 200GB/s
- Continuously Sampling ADC
- No hardware trigger

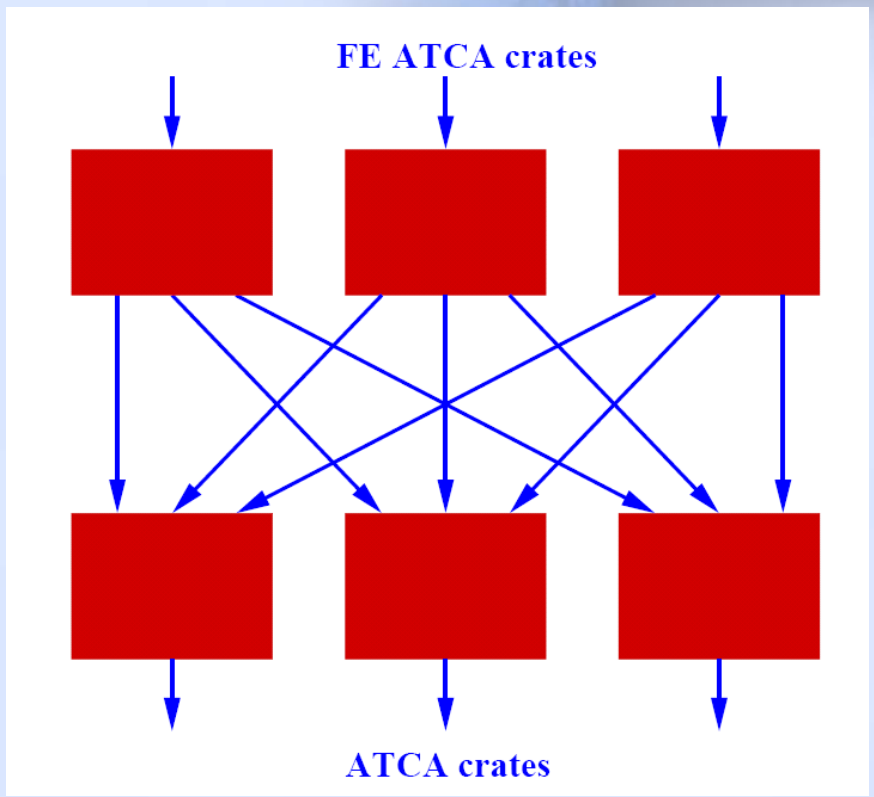
- Hi Speed Devices
- Large Buffers
- Large Bandwidth



PANDA DAQ & Trigger

+ 2 Alternative DAQ Concepts Still Under Discussion

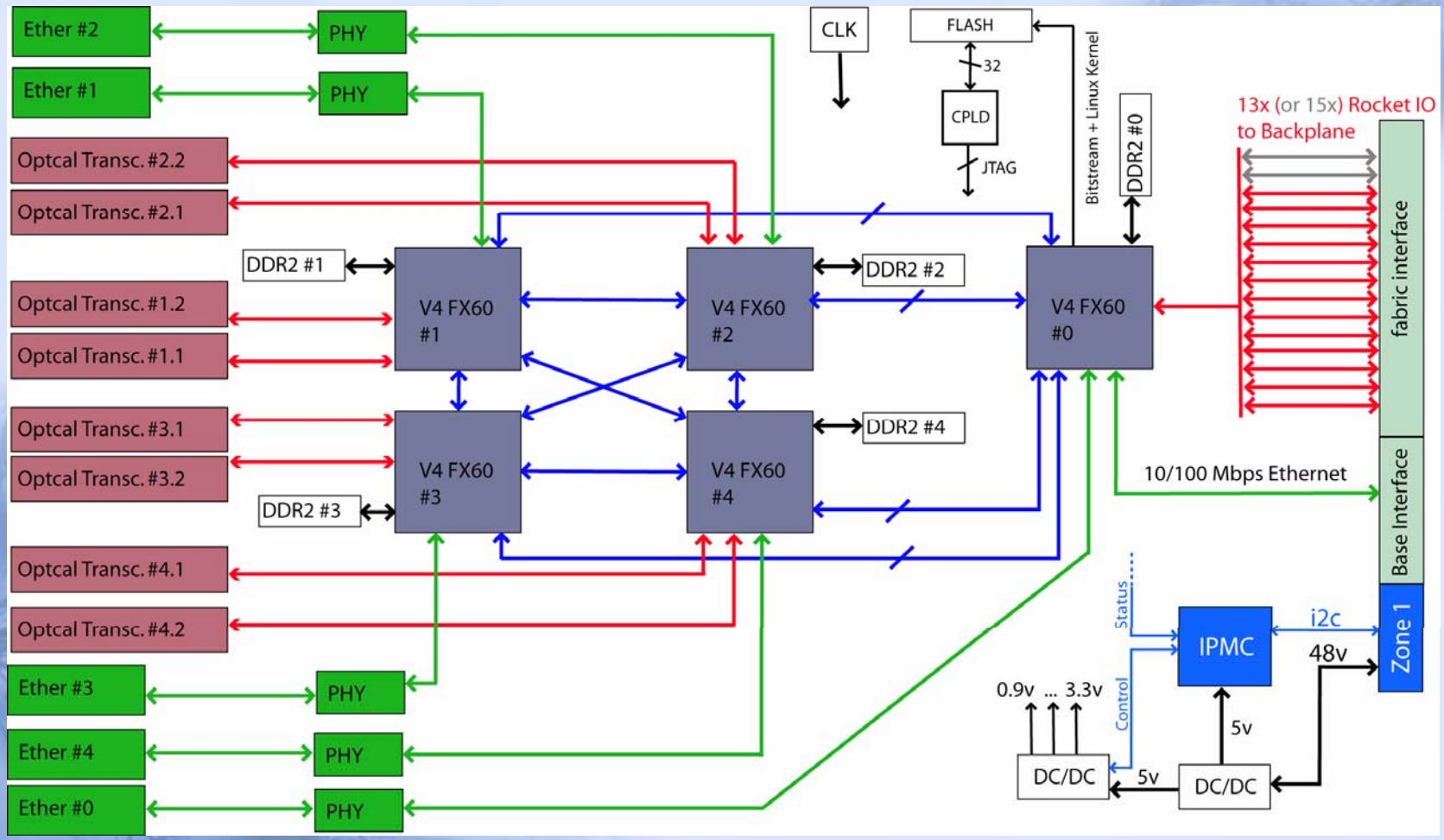




The Compute Node(CN)

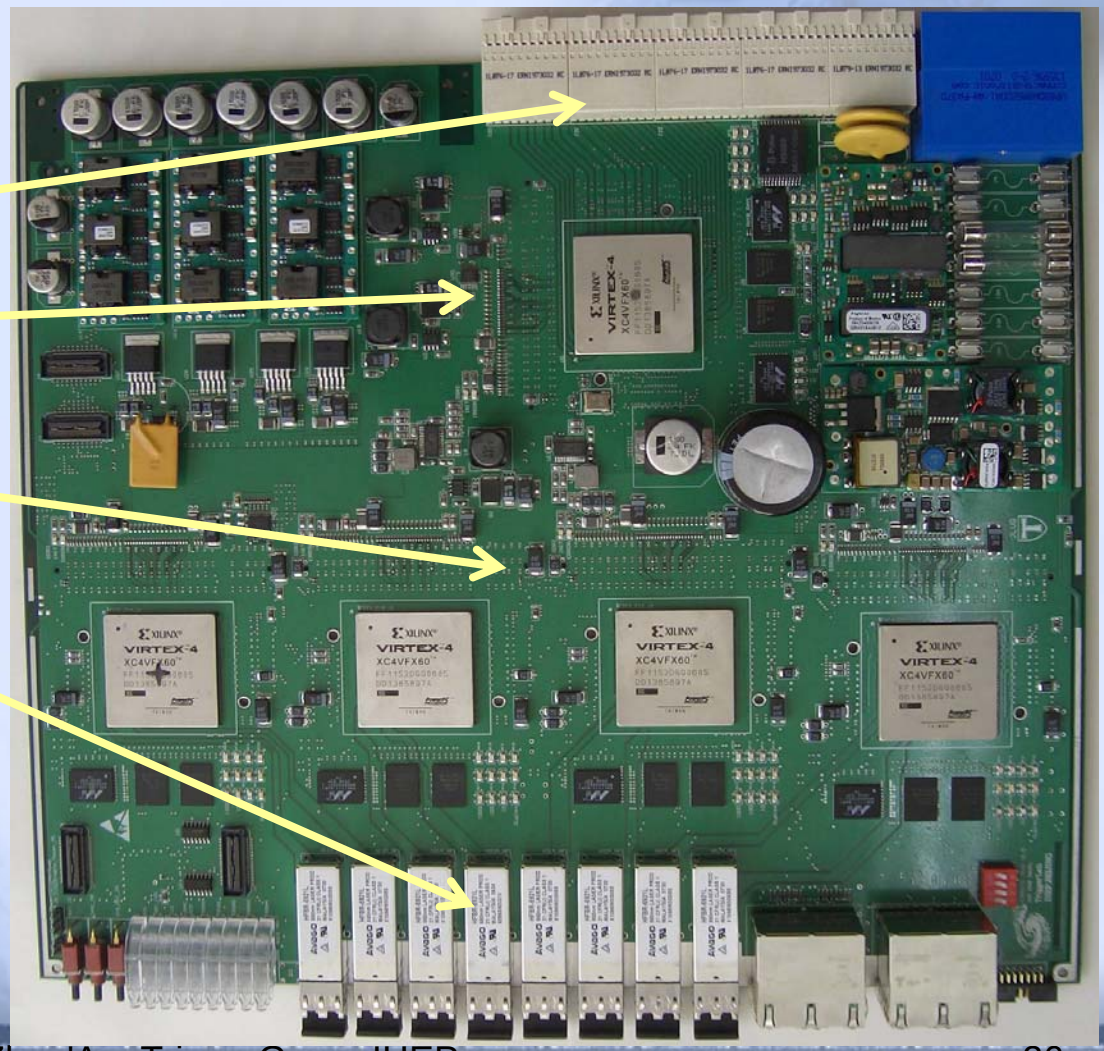
- 5 Virtex4 FX60 FPGA
  - Large Computer Power
- 10 GB DDR2 RAM (2GB per FPGA)
  - Buffering capabilities
- 2 Embedded PowerPC in each FPGA
  - Slow control
- 32Gbit/s Bandwidth
  - 13x RocketIO to backplane
  - 5x Gbit Ethernet Front Pannel
  - 1x Gbit Ethernet Backplane
  - 8x Optical Links
- ATCA Compliant
  - Manageability

The Compute Node



Prototype of the CN by IHEP Beijing

- Backplane
- FPGA #0
- FPGA #1-4
- Front Panel
  - Optical Links
  - Ethernet Plugs



Proof of Concept Application: HADES DAQ Upgrade

- Est.: 2009
- Read Out – Trigger
  - TRB
  - Faster Readout
- Trigger and Data
  - Optical Links
- Include Tracking in Trigger
- 12 Compute Node
  - 1 Full ATCA shelf

COMPUTE NODE

- Online Tracking
- RICH & TOF
  - Matching with Tracking
- Event Building on FPGA
- Others
  - Remote Upgrade
  - IPMI

Motivation/Aim

Produce a Configurable and Scalable Hardware Platform for Multiple Applications & Experiments

- Capable of High Performance Computing
- Large Bandwidth
- Real Time processing
  - Trigger
- Flexibility: Reusable
  - HADES - BESIII - PANDA
- Scalability
  - Flexible network topology

Comments and Conclusion

- RocketIO can be used for HS transmission at KEKB
- Awareness to KEKB TDAQ design:
  - System clock
  - Larger trigger latency
    - Latency by RocketIO (SEDES takes time)
    - Needs larger pipeline buffer in FEE
  - Synch. + alignment
    - Uncertainty in recovered clock
    - Opt-cable length difference
    - Opt-transceiver difference

Thanks!