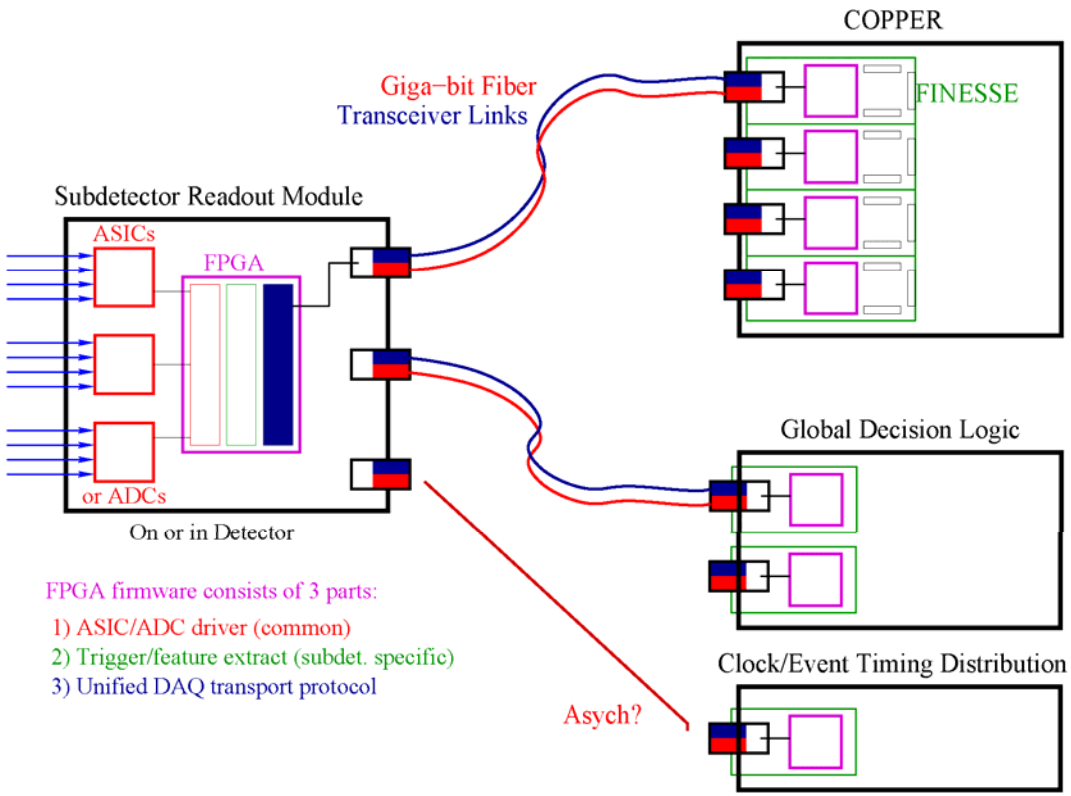
Possible ASIC Options within a Common Readout Infrastructure



Gary S. Varner and Larry L. Ruckman

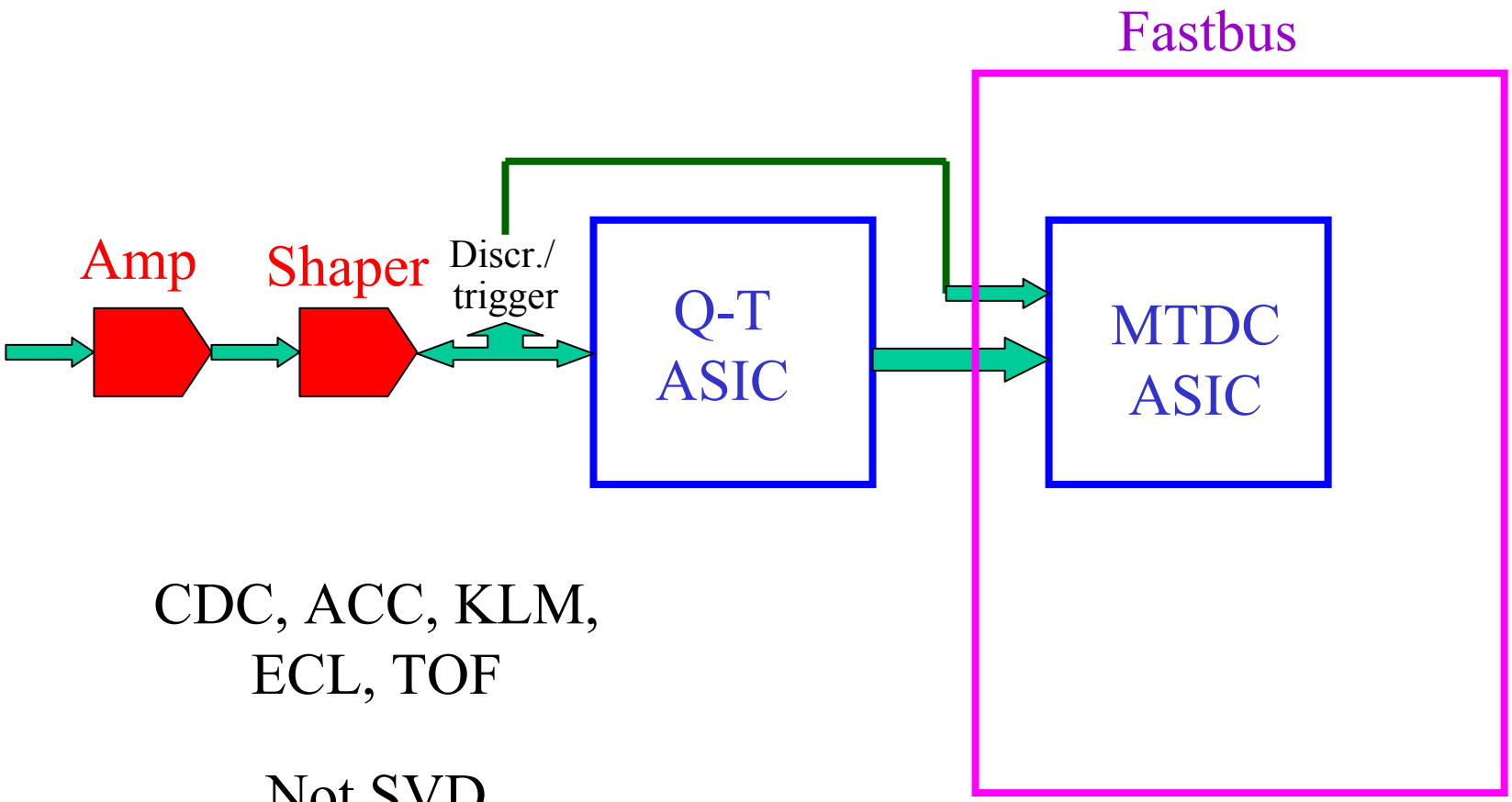
OCM2 Trg/DAQ Parallel Session

July 4th, 2008

Today's Topics

- There are two separate issues
  - Common trigger/clock/data link
  - Possible common/related readout ASICs/firmware/software
- Many subdetector-specific details
  - Just highlight some issues
  - Separate discussions with subdetector groups (if interested)
- Precision Timing
  - Better clock distribution – follow ps timing development
  - Better T0 determination
- System approach
  - Defer specifics of implementation
  - Suggest a common approach

A Common Approach for Belle



CDC, ACC, KLM,
ECL, TOF

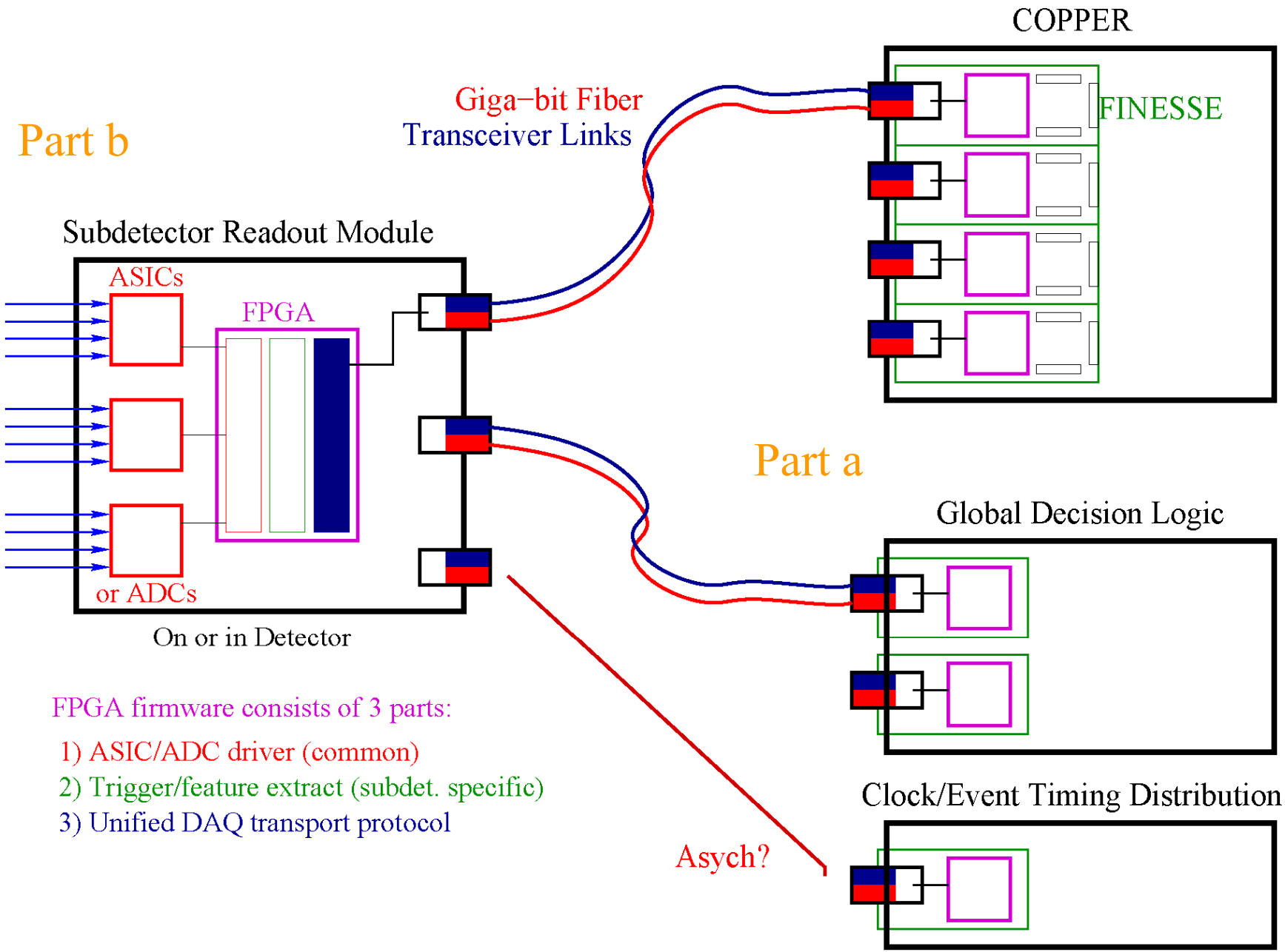
Not SVD

Upgrades:

Fastbus → COPPER

MTD132A → AMT3

Proposed Common Approach for Belle++

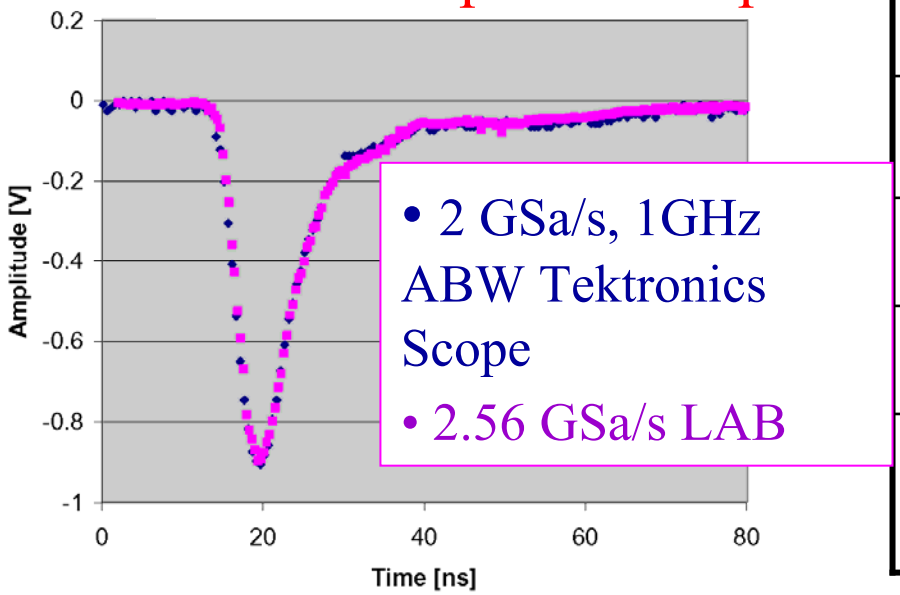


FPGA firmware consists of 3 parts:

1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

Key Enabling Technology

"oscilloscope on a chip"

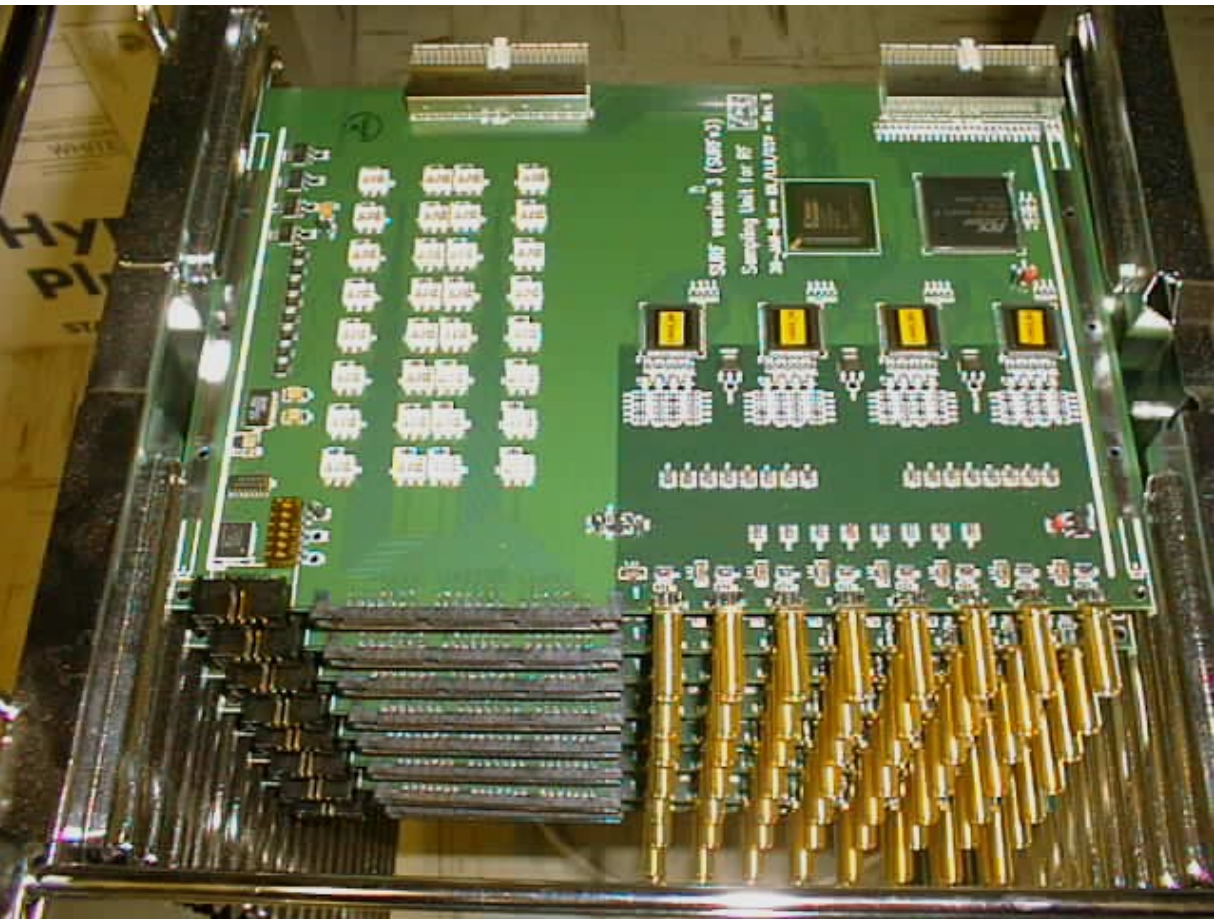


- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

	LABRADOR	Commercial
Sampling speed	1-3.7 GSa/s	2 GSa/s
Bits/ENOBs	12/9-10	8/7.4
Power/Chan.	<= 0.05W	5-10W
Cost/Ch.	< $10 (vol)	> 1k$

1. PoS PD07: 026, 2006
2. NIM A583: 447-460, 2007
3. NIM A591: 534-545, 2008
4. arXiv: 0805.2225 (submitted NIM A)

Other Enabling Technologies

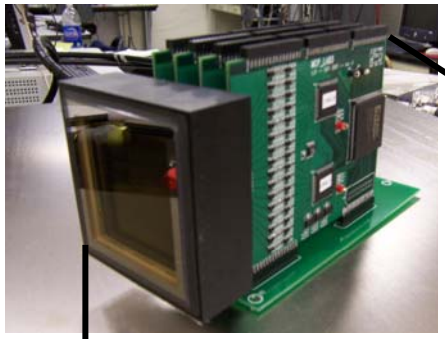


FPGA as:

1) Discriminator
2) ADC
3) TDC
4) Event FIFO
5) Feature extract
6) SerDes fiber

1. Journal Instr. 1: P07001, 2006
2. Journal Instr. 2: P04006, 2007
3. “PRO timing encoding”, in preparation

Test System Readout Block Diagram



Giga-bit Fiber

Photo-Sensor

BLAB2

BLAB2

BLAB2

BLAB2

MCP MAIN

x7

cPCI CARD

cPCI Crate (Linux)

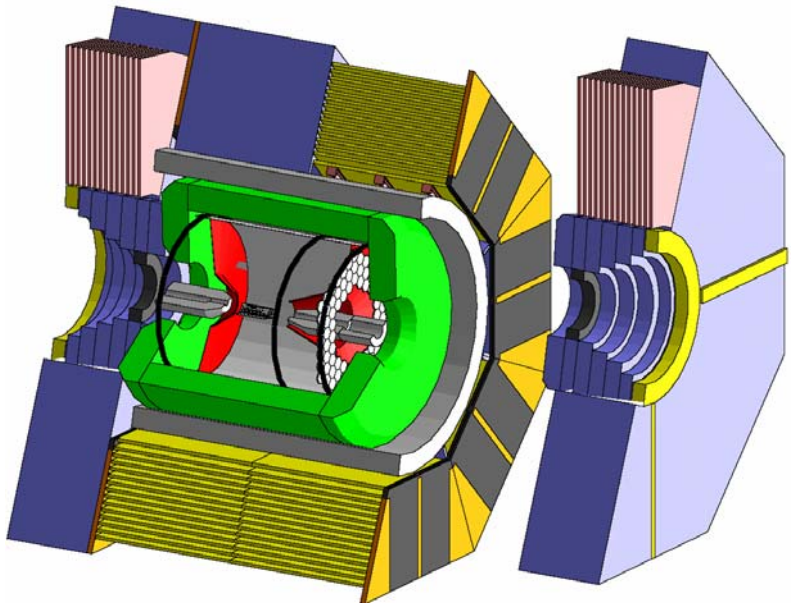
COPPER

- Up to 7x64 channels per cPCI card
- Up to 32,256 channels/cPCI crate

Very cost effective, board hardware already exists

Possible ASIC Options

Subdetector	ASIC	ref. ASIC	Location	FPGA link
PXD	**TBD**	**TBD**	hybrid/dock	yes
SVD3	APV25		E-hut	no
new SVD	BSR/KUPID	APV25	hybrid/dock	yes
CDC	BCA	TARGET	in detector	yes
PID SiPMT	BCA	TARGET	in detector	yes
PID HP-PMT	HPBA	BLAB2	in detector	yes
ECL	N/A		on detector	yes
Scint. KLM	BCA	TARGET	in detector	yes
VFV	BCA	TARGET	in detector	yes

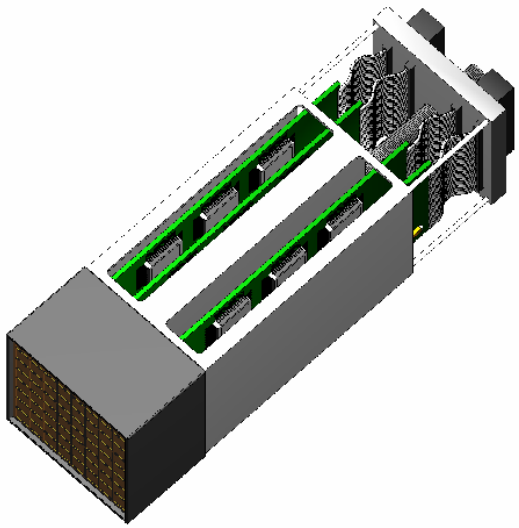


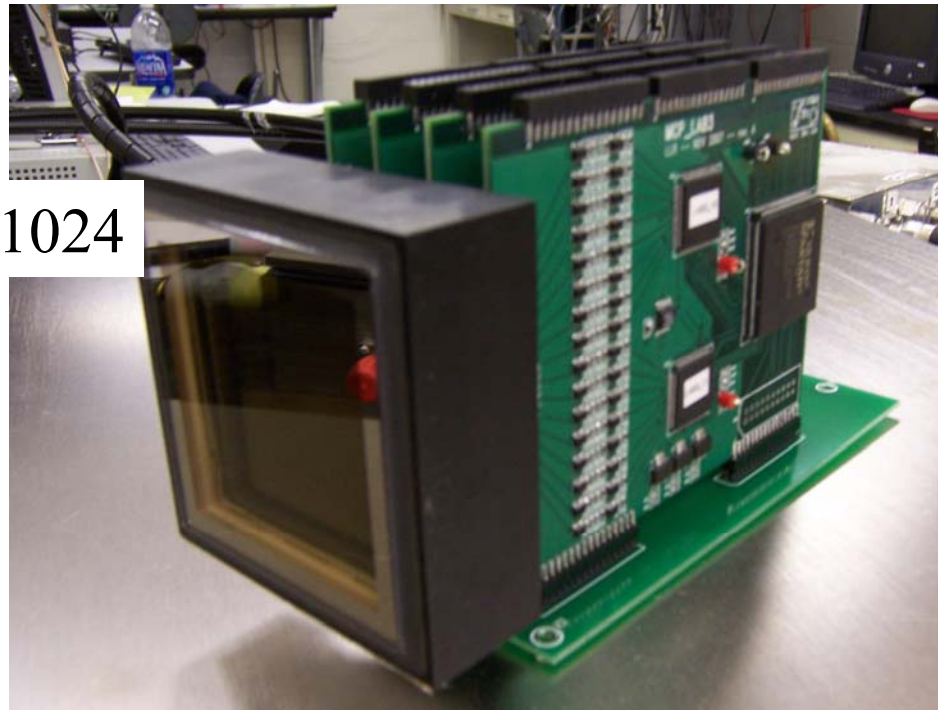
Starting Place: BLAB2 & "PD scale" readout

- **Initial Target: New TOP/iTOP/f-DIRC Readout System**

TABLE II: *BLAB2 ASIC Specifications.*

Item	*Value*
Photodetector Input Channels	16
Linear sampling arrays/channel	~~2~~ 6
Storage cells/linear array	~~512~~ 1024
Sampling speed (Giga-samples/s)	2.0 - 10.0
Outputs (Wilkinson)	32

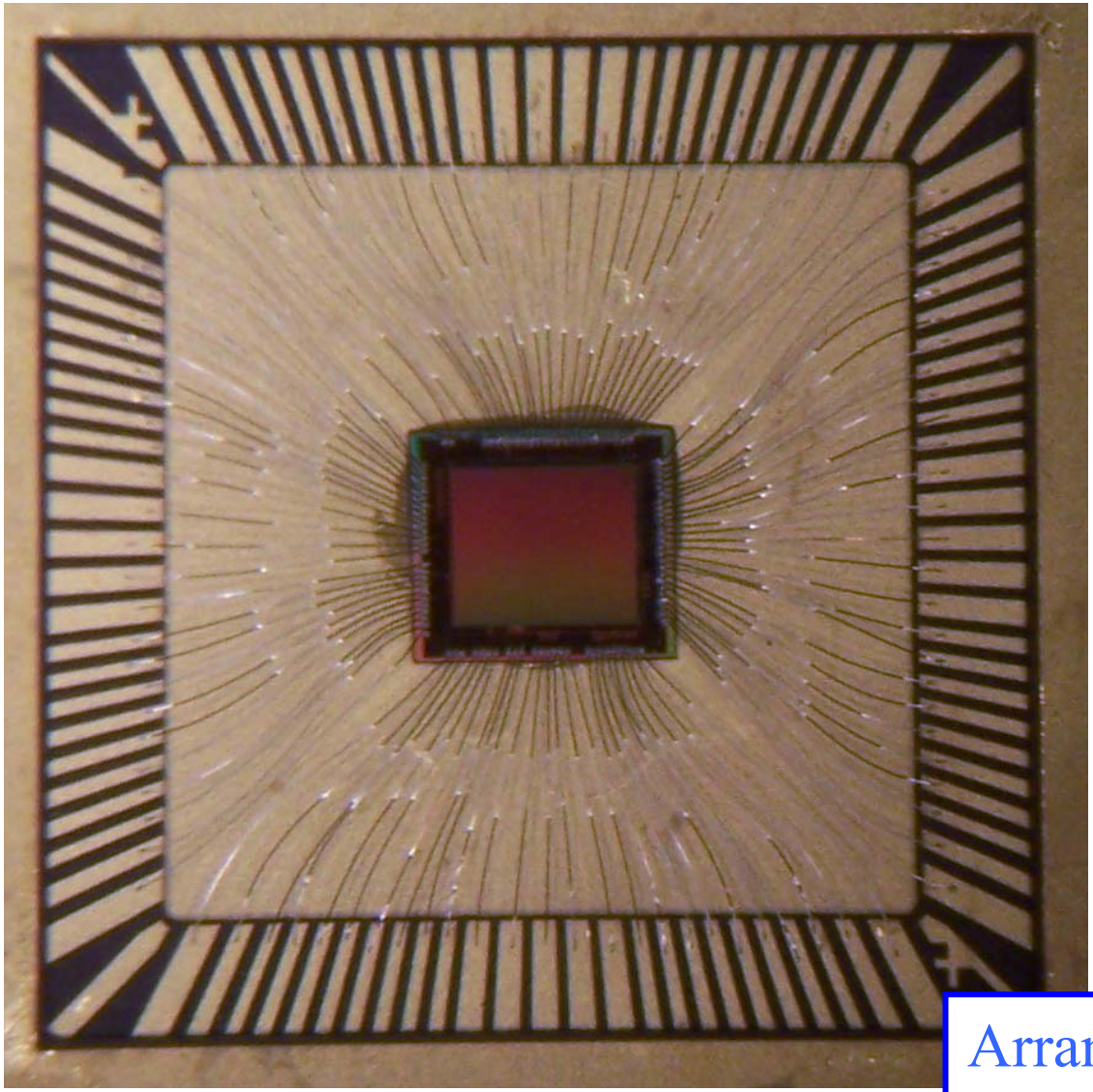




Gen. 0 Prototype (LAB3)

Submitted for fabrication: June, 2008 (avail autumn)

Design Basis: Buffered LABRADOR (BLAB1) ASIC

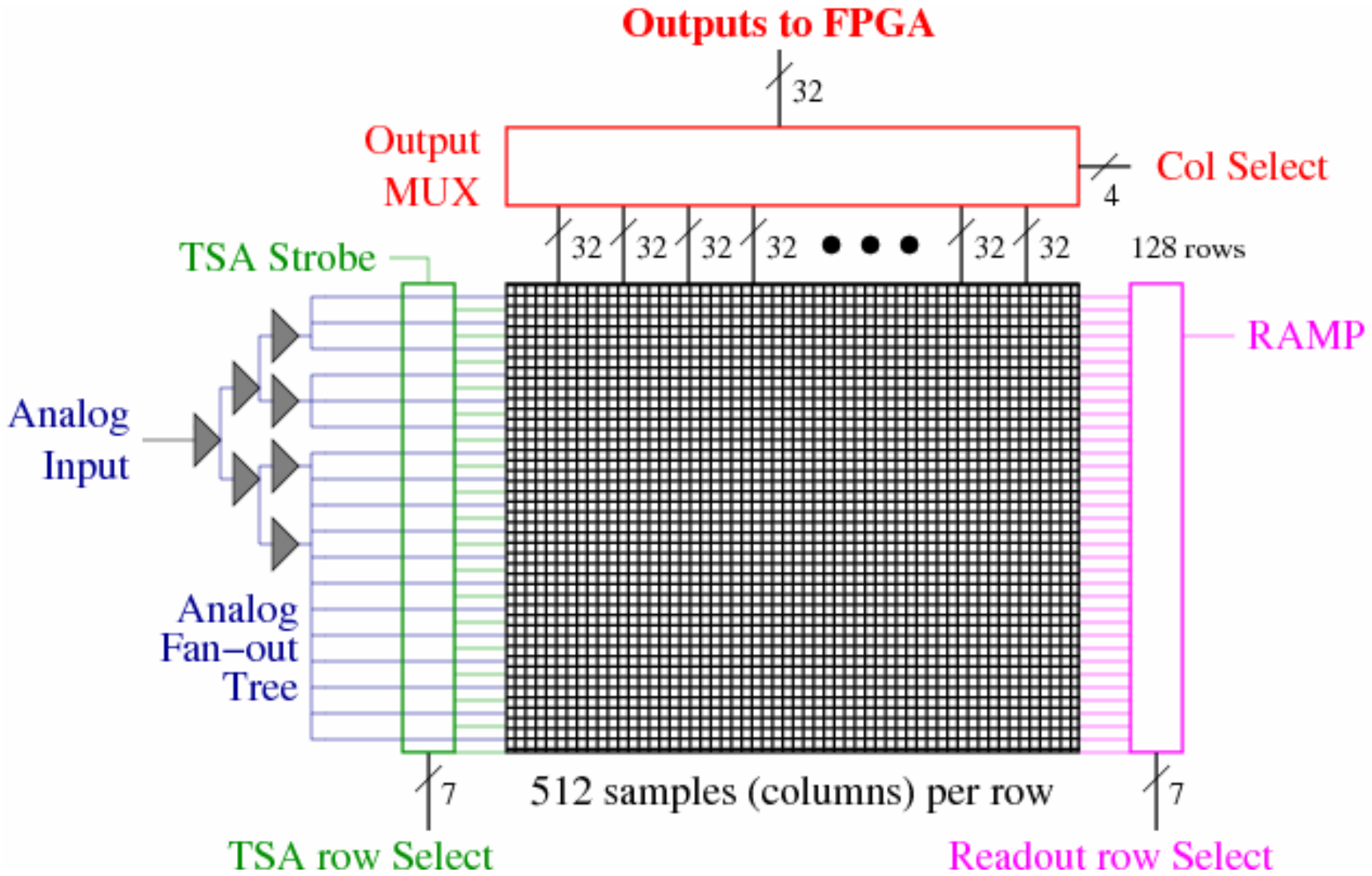


3mm x 2.8mm, TSMC 0.25um

- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

Arranged as 128 x 512 samples
Simultaneous Write/Read

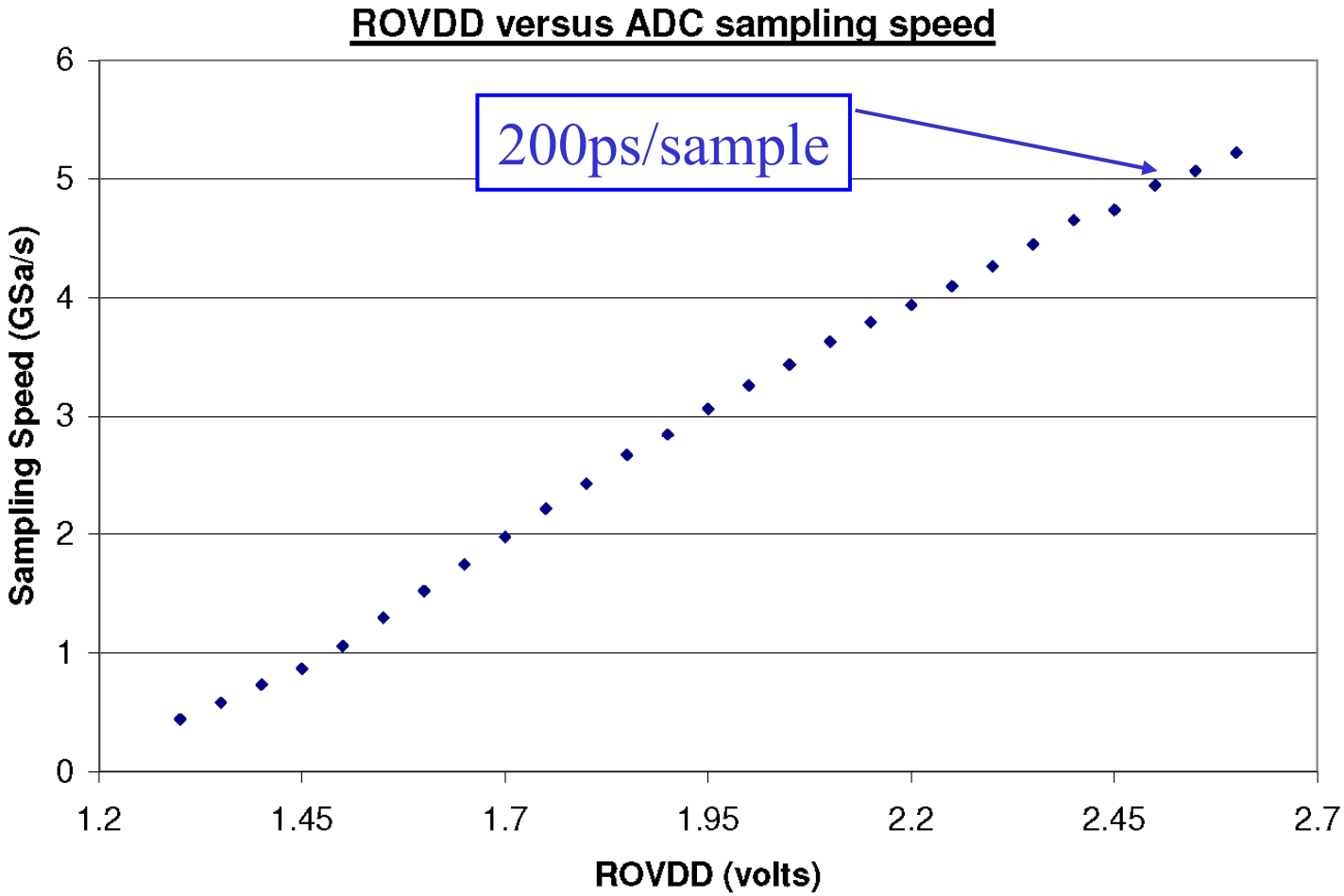
BLAB1 Architecture



FPGA-based TDC: 10-bits in 1us (300ps resolution)

BLAB1 Sampling Speed

Can store 13us at 5GSa/s (before wrapping around)



Single sample:
200/SQRT(12)
~ 58ps

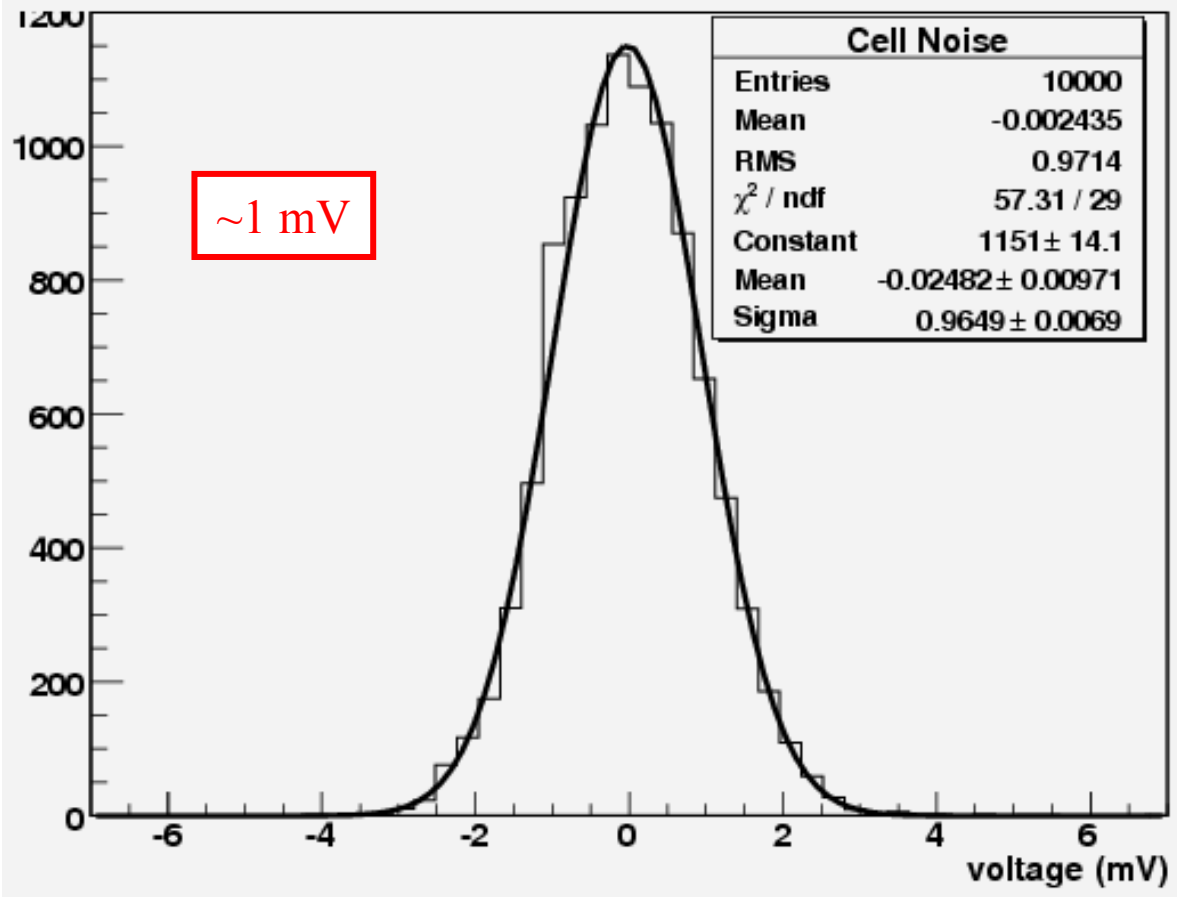
In practice, have often been using 512 samples

Buffered LABRADOR (BLAB1) ASIC

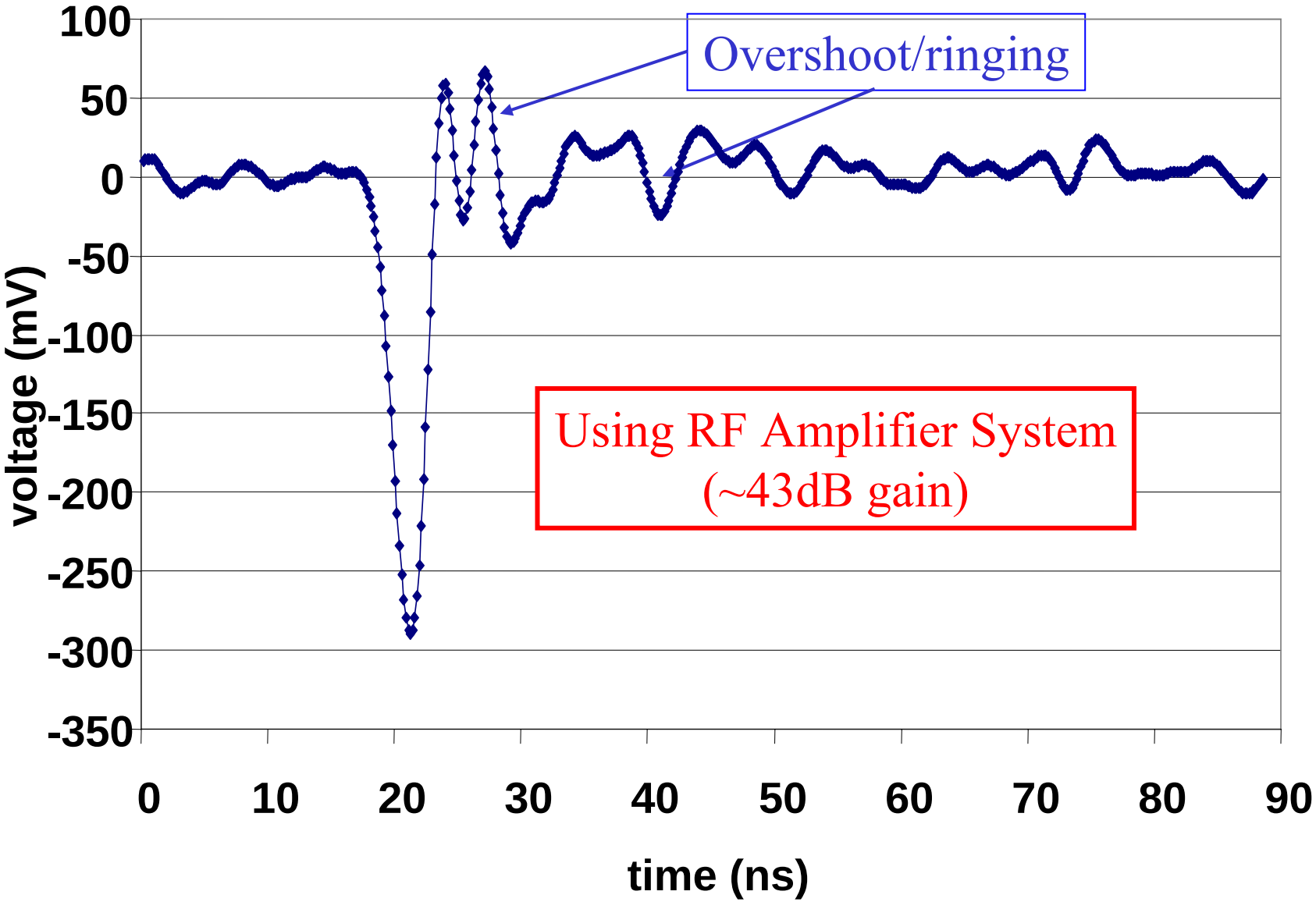
- 10 real bits of dynamic range, single-shot

Measured Noise

1.6V dynamic range



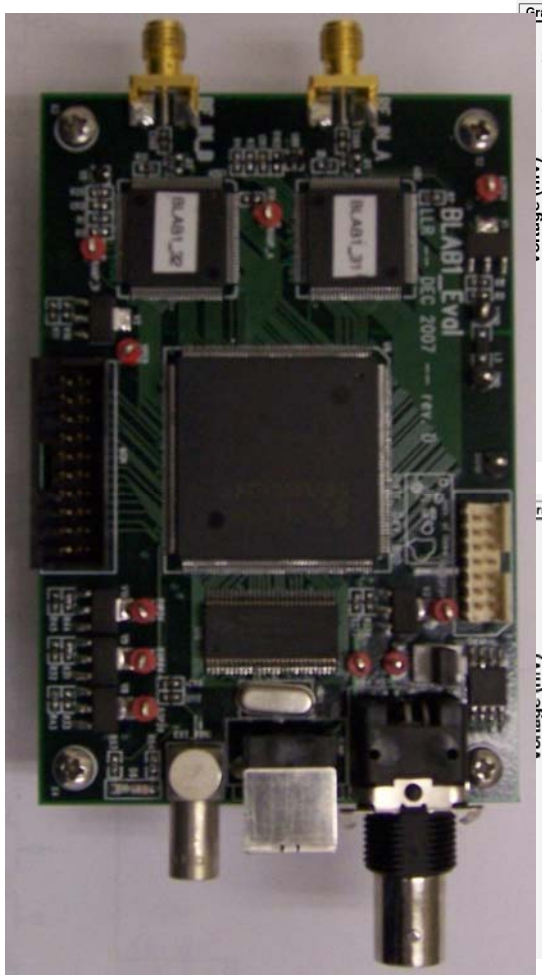
Typical single p.e. signal [Burle]

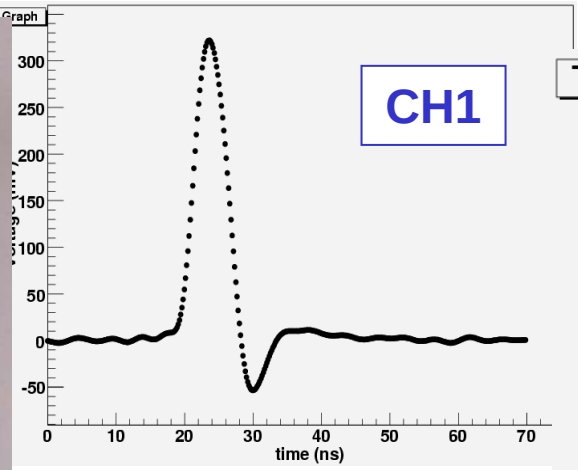


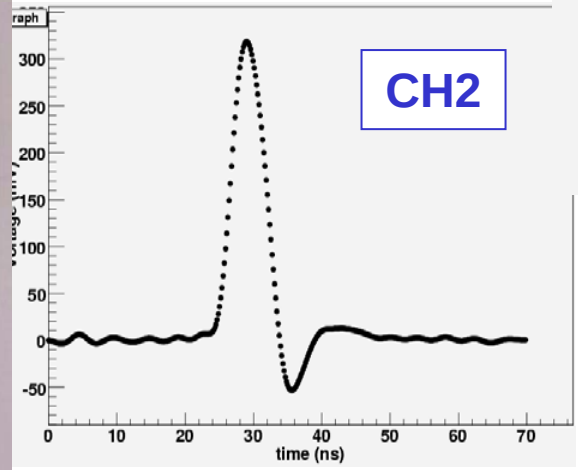
Excellent Timing Performance

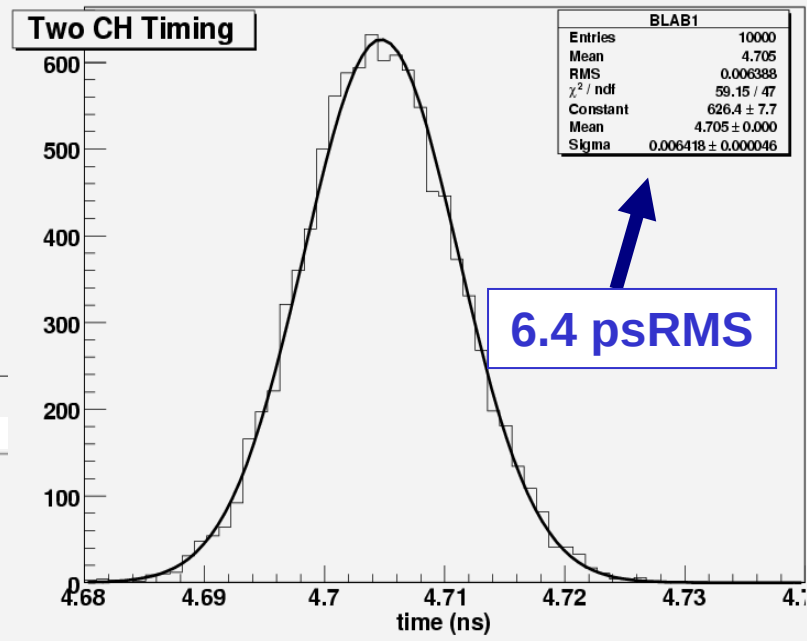
- Two separate BLAB1 ASIC with a common sampling strobe
- RF split the Agilent pulse with additional cable delay in the 2nd channel

Example of tailoring to need



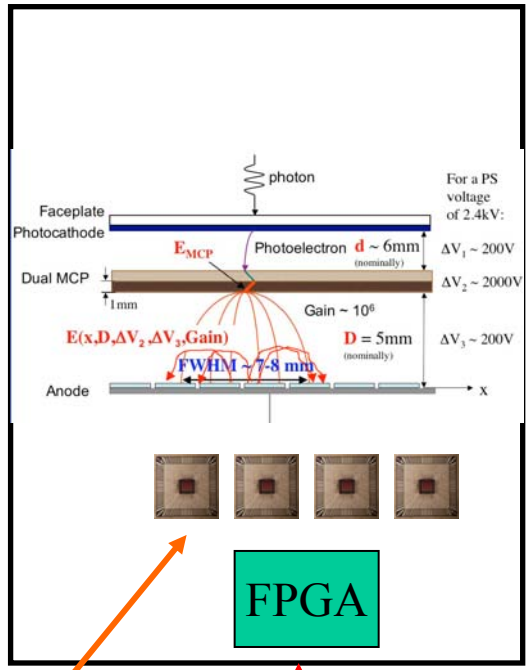






Typical System Specifications

8k	samples/channel (~8us trig latency)
16	channels/TARGET ASIC
4	TARGET ASIC
~9	bits resolution
32	samples in window (~32ns)
~1	GSa/s
2k	word (9 bits) Event size
16	us to read all samples (zero sup.)
50	kHz sustained L1 readout



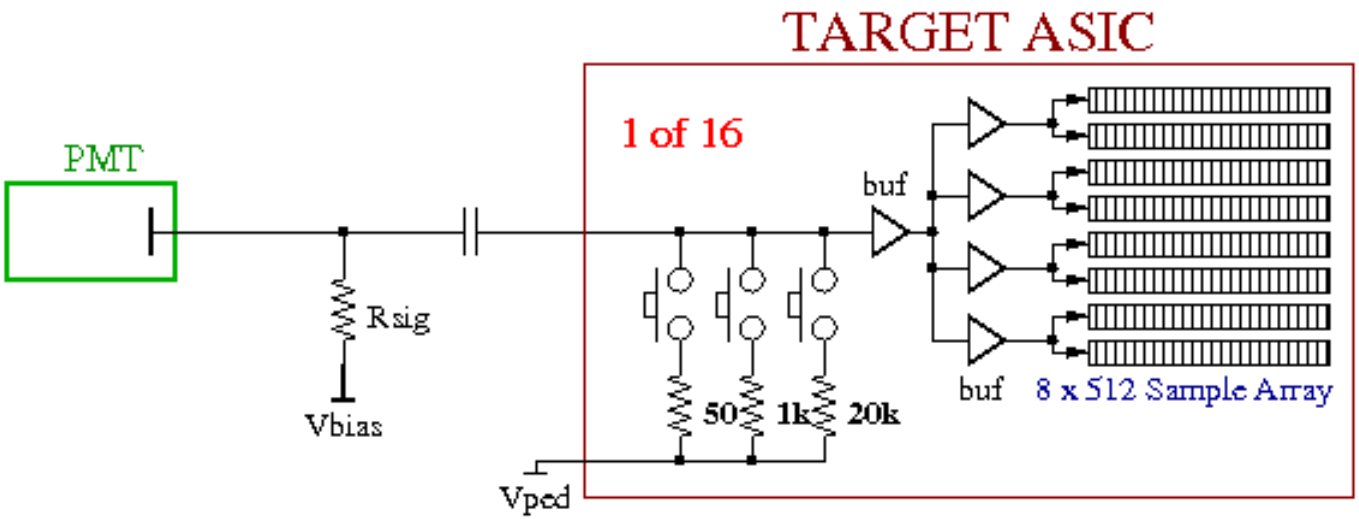
4x TARGET

FINESSE

- Readout link
  - Initially USB2 [>50kHz Event sustained (20Mbit/s)?]
  - Fiber links to make TARGET RO limited and use to collect trigger information

Need to specify ASIC requirements

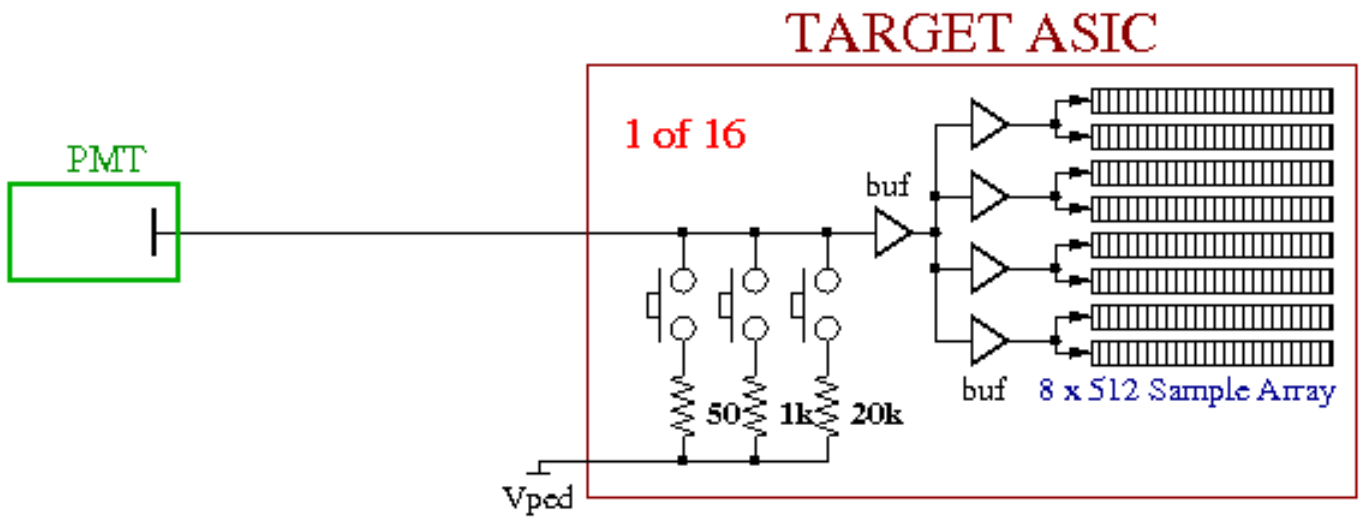
- E.g. What gain needed?
  - At 10^6 gain, each p.e. = 160 fC
  - In typical ~5ns pulse, Vpeak = dQ/dt * R = 32uA * R = 32mV * R [kΩ]
- AC Coupling mode



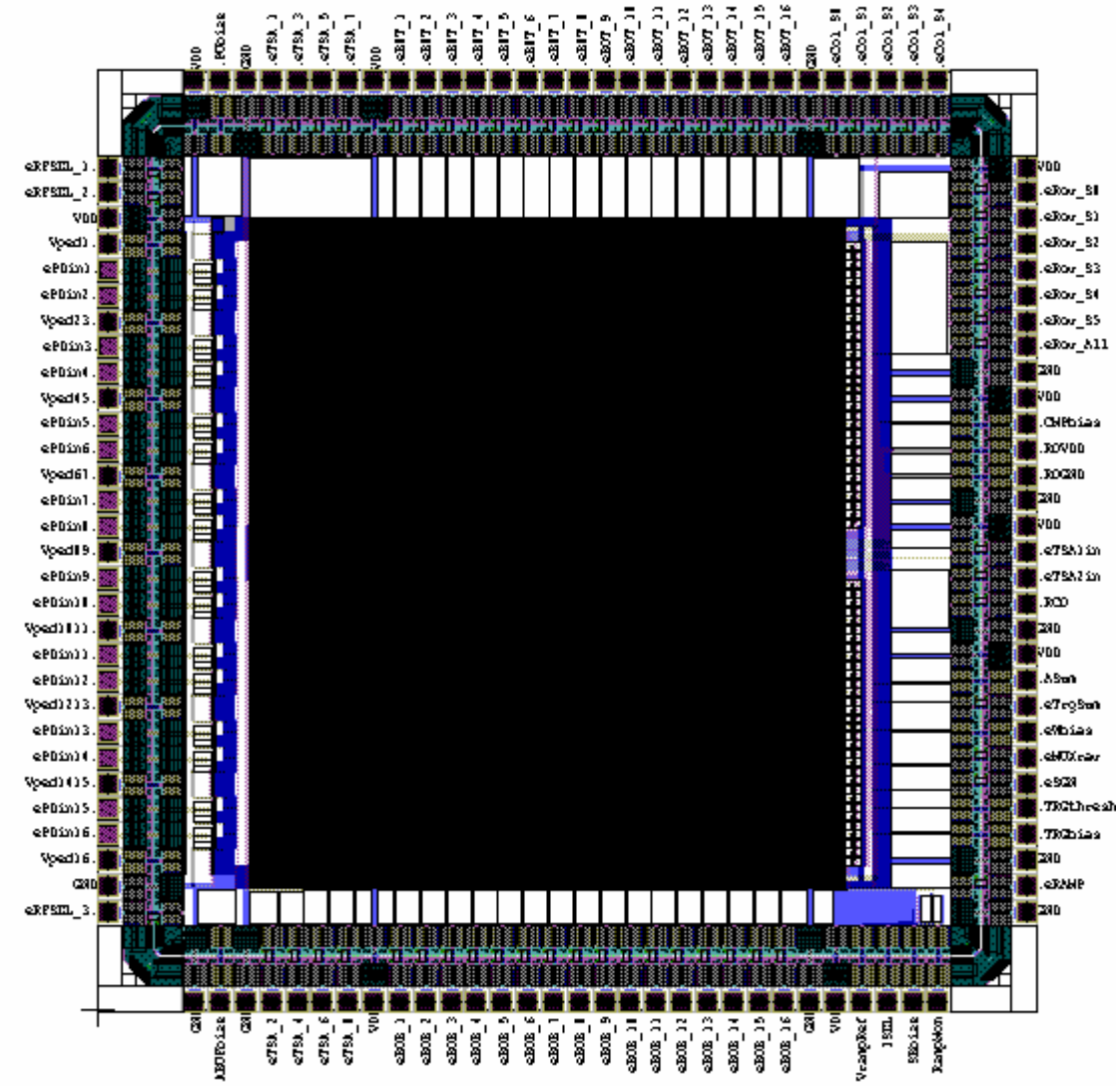
Signal Amplitude

Gain Estimate	
Rterm	**1 p.e. peak**
50	1mV
1k	20mV
20k	400mV

- DC Coupling mode (reduced dynamic Range)

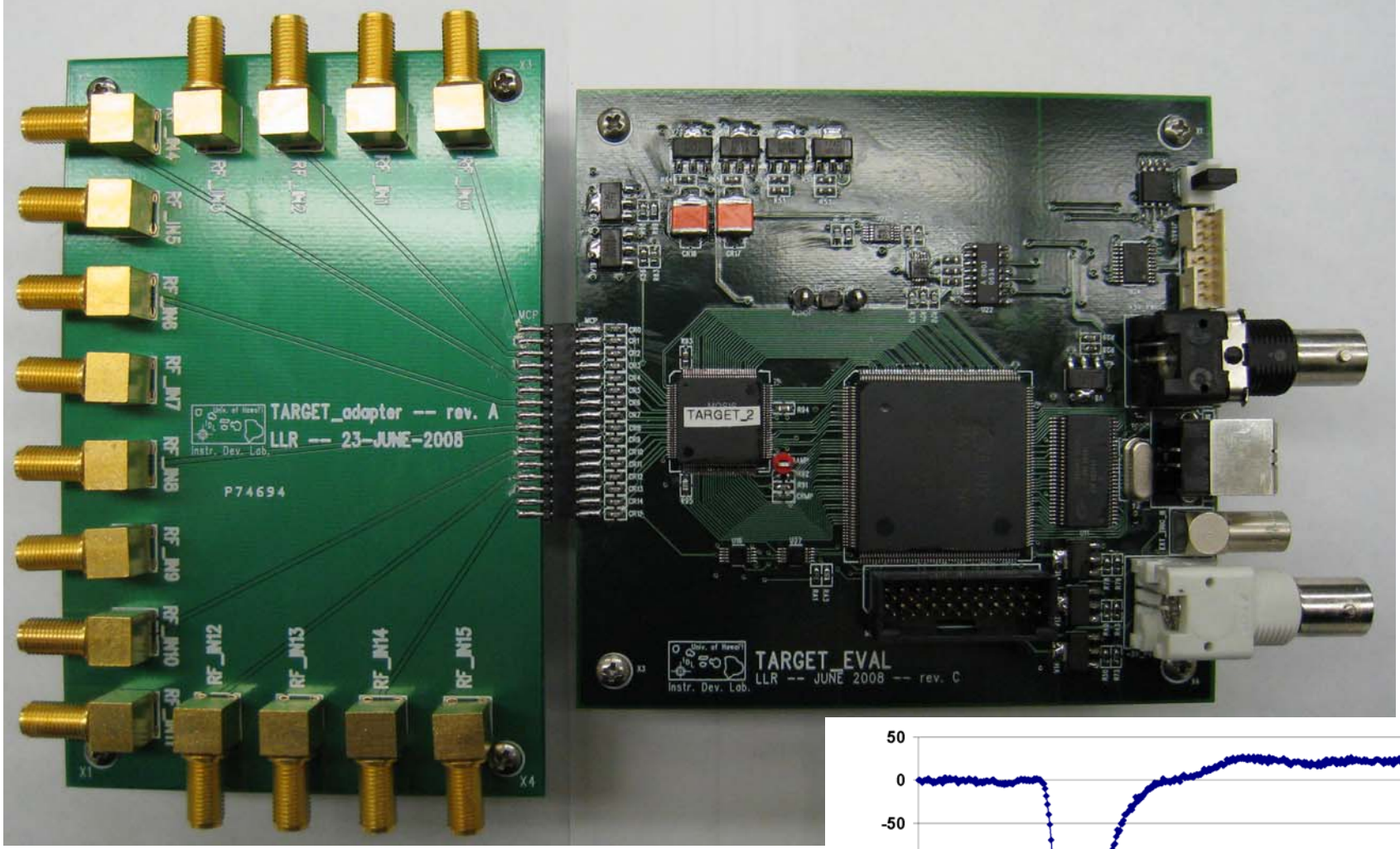


Design Reference: TARGET ASIC

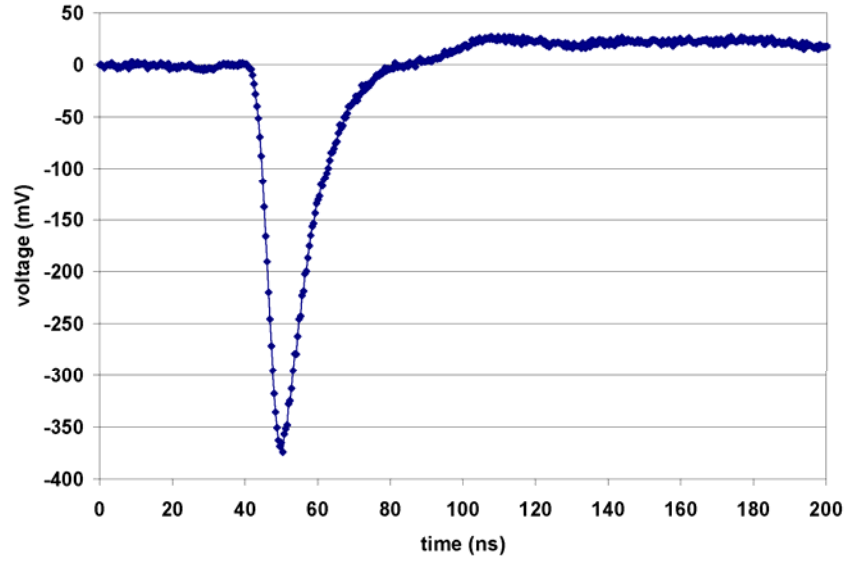


- ~3 x 3 mm die
- 4k samples (8x rows interleave)
- Multi-hit buffering
- Fast-scan readout mode

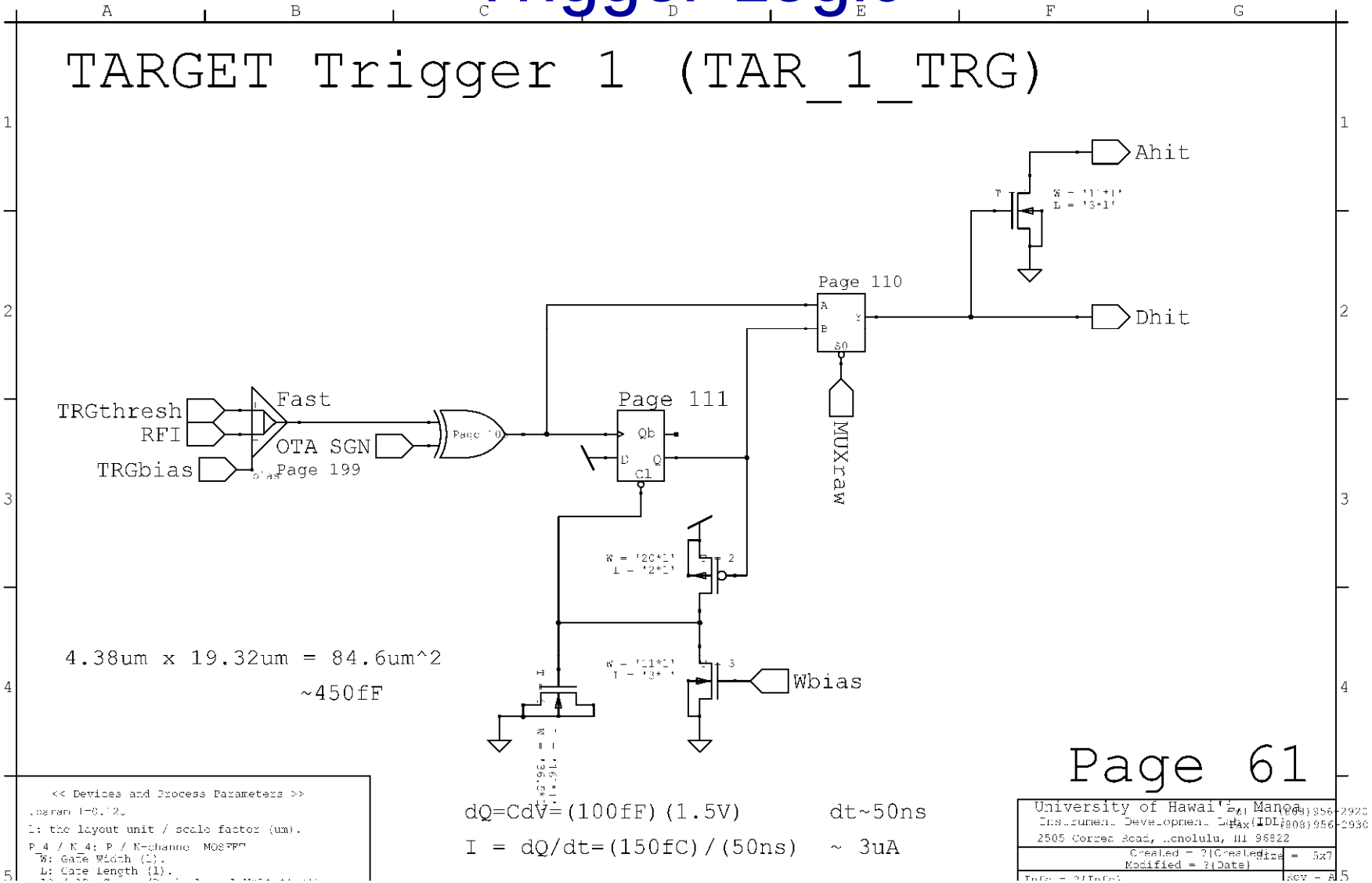
- 16 channel waveform recording
- Trigger prototype



Evaluation Board: TARGET ASIC

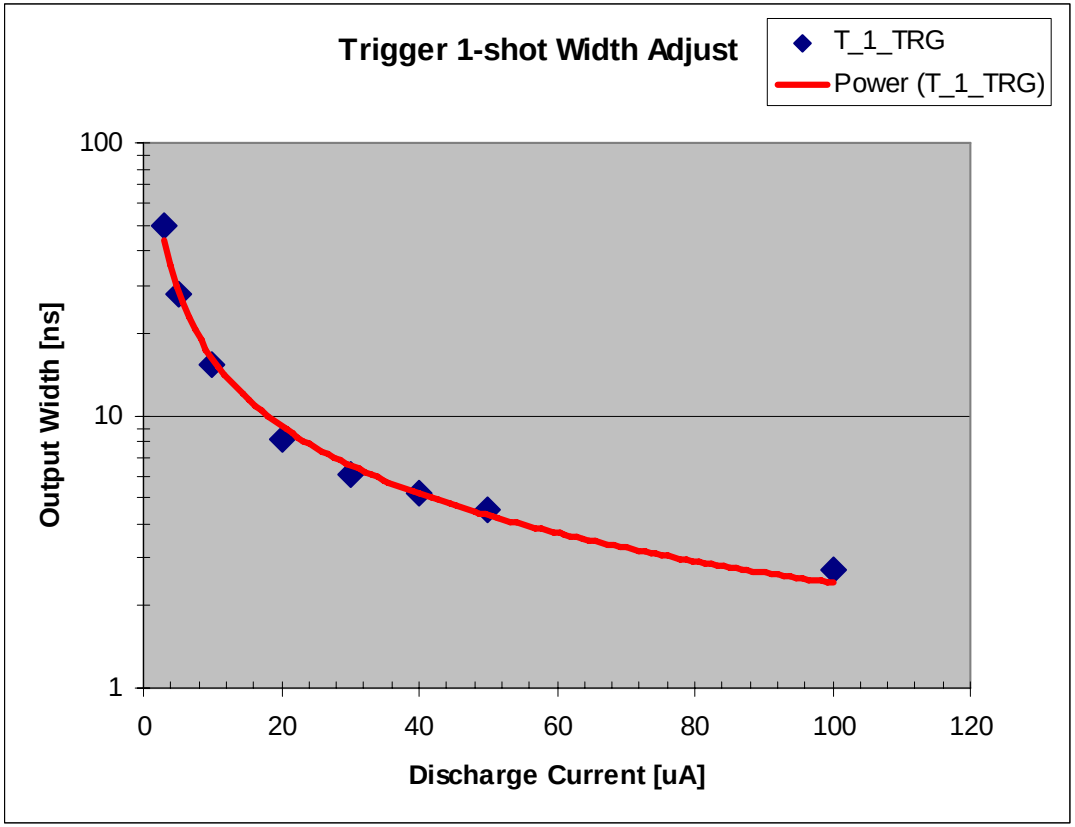


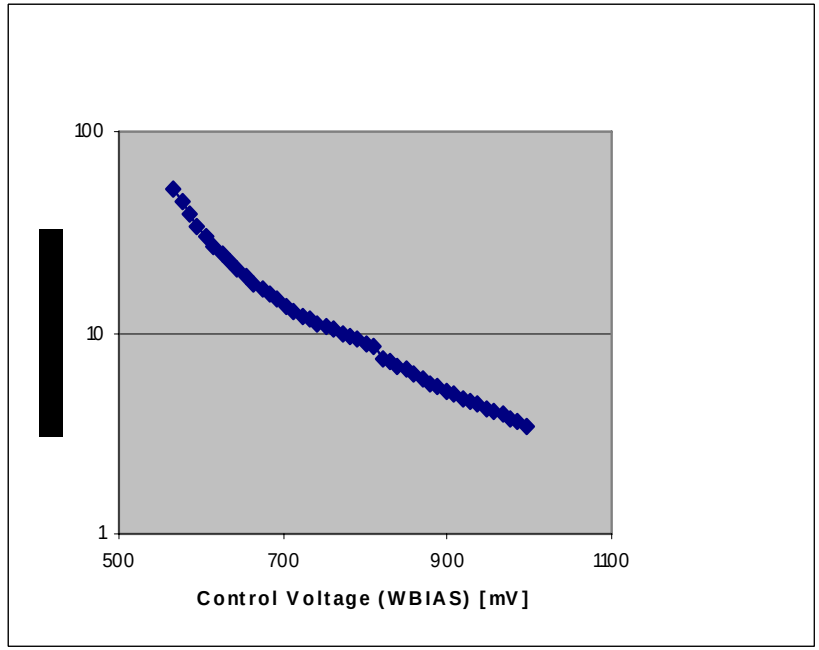
Trigger Logic



- Analog (Sum of # Ch. ON) & Digital OR output
- 1-Shot or Raw comparator output

Trigger Performance



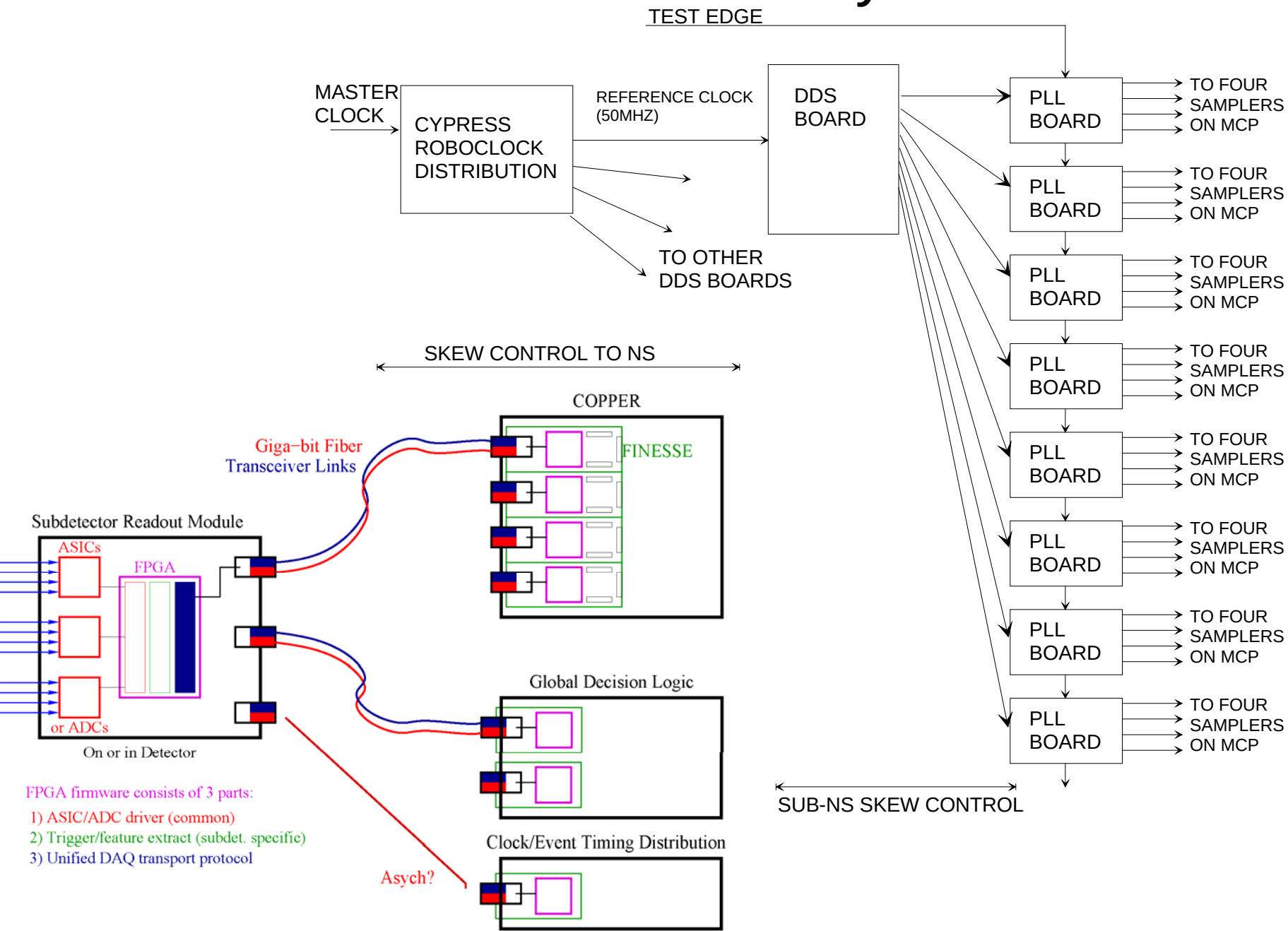


- Good Adjustment Range
  - Reasonable current values
  - Stable, good coincidence capability

Specific Issues

- Pixel: how to event match (track matching)
- SVD: APV25-type OK, but faster pipe drain desired
- CDC: matched amp/LVDS outputs
- KLM: 2-level FPGA readout OK? (FPGA-based TDC good enough)
- PID with Precision Timing: precision clock distribution

Clock Distribution System



CDCE62005 Pico BTS/Data Com Clock

3:5 Frequency Synthesizer/Jitter Cleaner

Features

- Input frequencies from 3MHz to 500MHz
- Crystal Inputs from 2MHz to 42MHz
- Output frequencies from 4.25MHz to 1.175GHz
- Output up to 5 LVPECL/5 LVDS/10 LVCMOS
- Individual phase adjust
- Optional high swing LVPECL mode
- Wide-range integer divide selectable by output
- **Low output skew (~ 20ps, typ)**
- Integrated/External PLL Loop Filter
- **Low jitter (< 1ps RMS)**
- On-chip EEPROM

Benefits

- Fully Integrated twin VCOs support wide output frequency range
- Wide input/output frequency range supports high and low end of frequency standards
- Selectable input/output standards reduces translation logic
- Integrated/external loop filter provides flexibility
- EEPROM saves default start-up settings
- SPI interface provides in-system programming
- QFN-48 package, Tem -40 to 85 C

Applications

- Wireless BTS
  (Pico, WiMax cells, Macro Base band)
- Data Communications
- Medical
- Test Equipment
- Jitter Cleaners

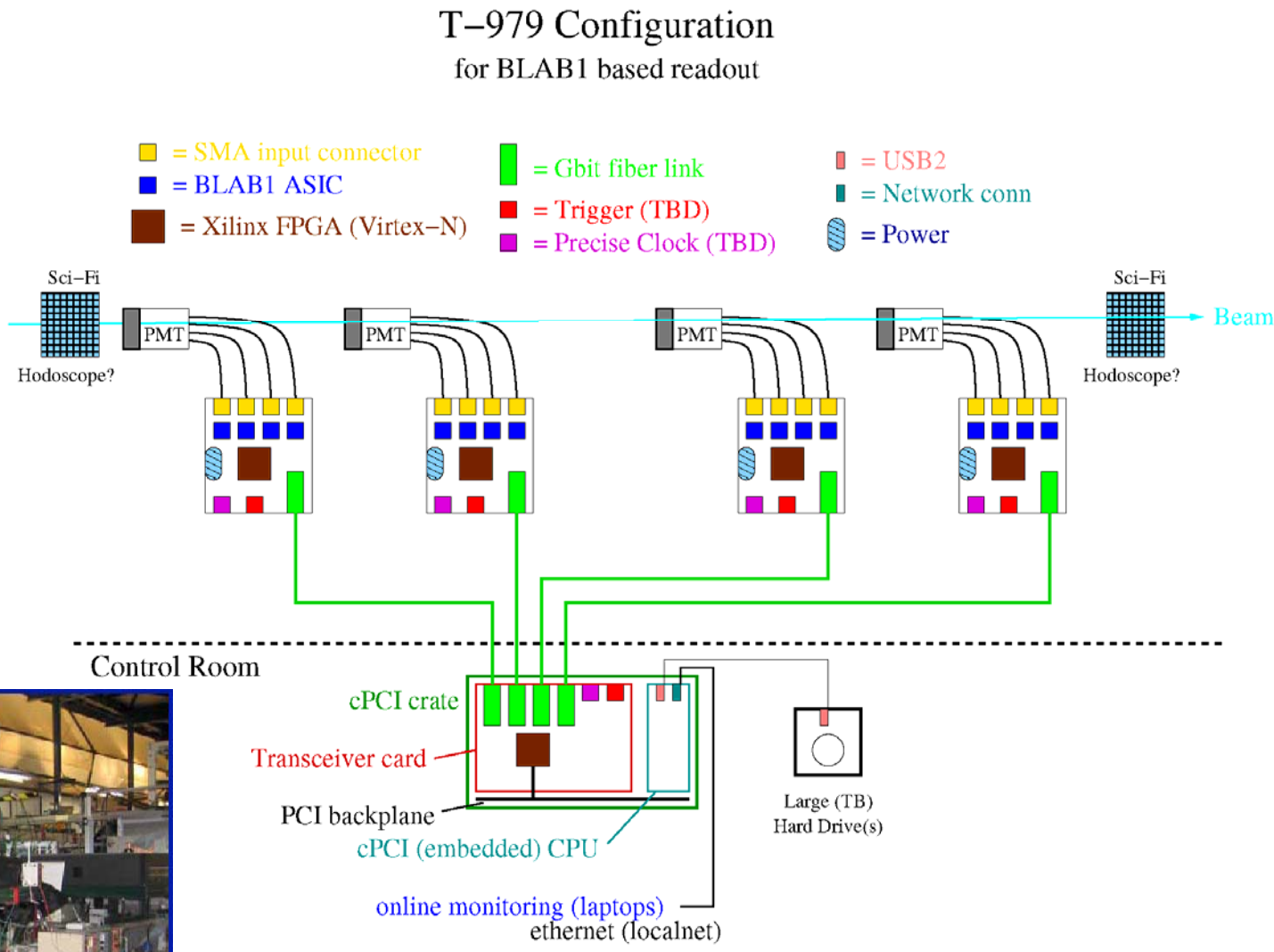
Oct/07 Sampling

May/08 In Production

John Anderson
HEP Electronics Group
Argonne National Laboratory

Presented by Gary Drake

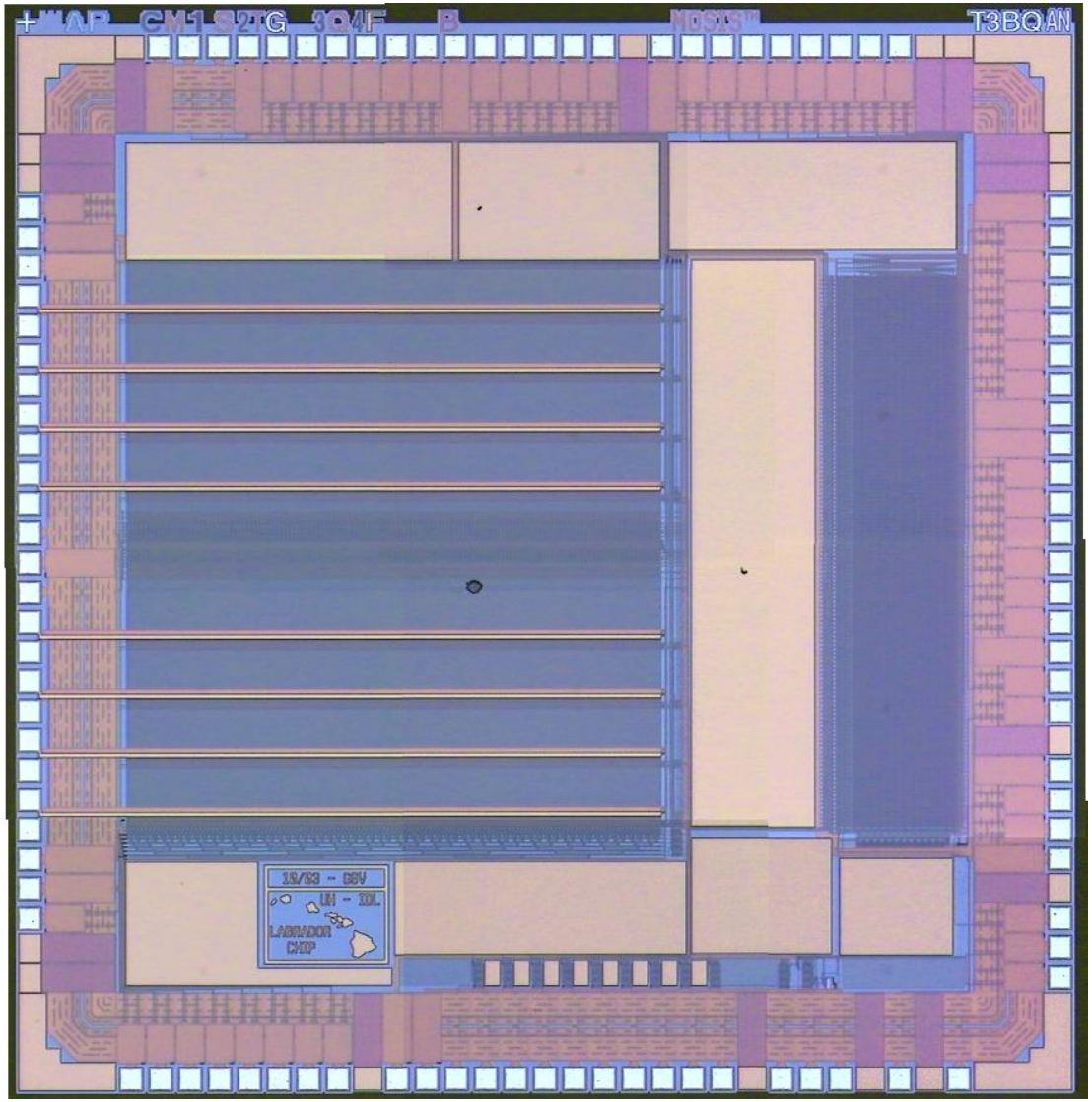
Testbed – FNAL T-979



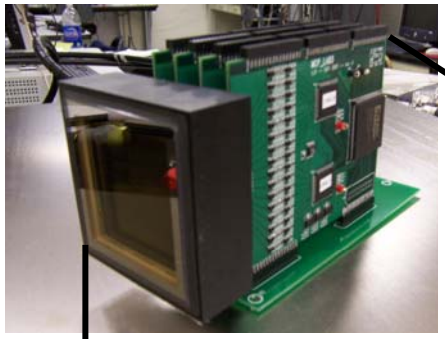
Summary

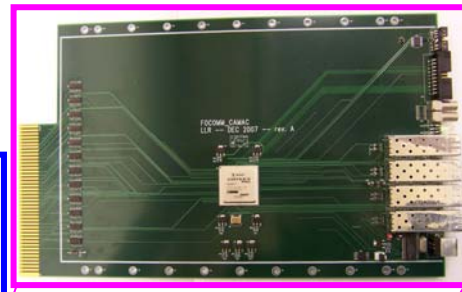
- New technologies options
  - Low cost, high performance recording
  - Internal gain/triggering (min. external noise)
  - Fiber-optic communications (back to future)
- Many details
  - Work with subdetector groups (offer, not forced)
  - Biggest issues: amplification and form factors
- Variants
  - While different in details, basics of buffer and trigger management common
  - Common protocols for subdetector readout developers to design to (common resources)

Back-up slides



Readout System Block Diagram





Giga-bit Fiber

CAMAC For beam-test only!

Photo-Sensor

BLAB2

BLAB2

BLAB2

BLAB2

MCP MAIN

x7

cPCI CARD

cPCI Crate (Linux)

x1

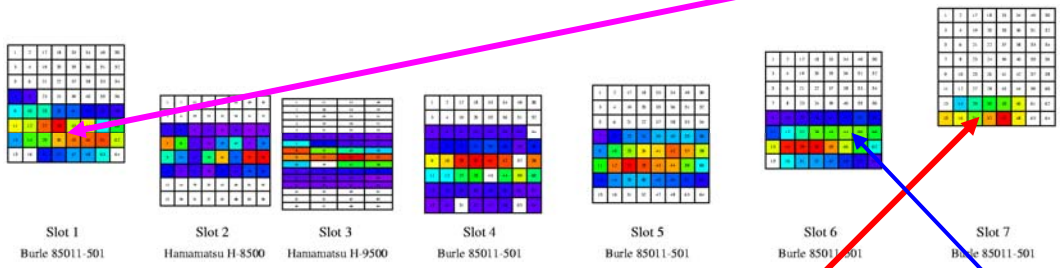
CAMAC CARD

CAMAC Backplane

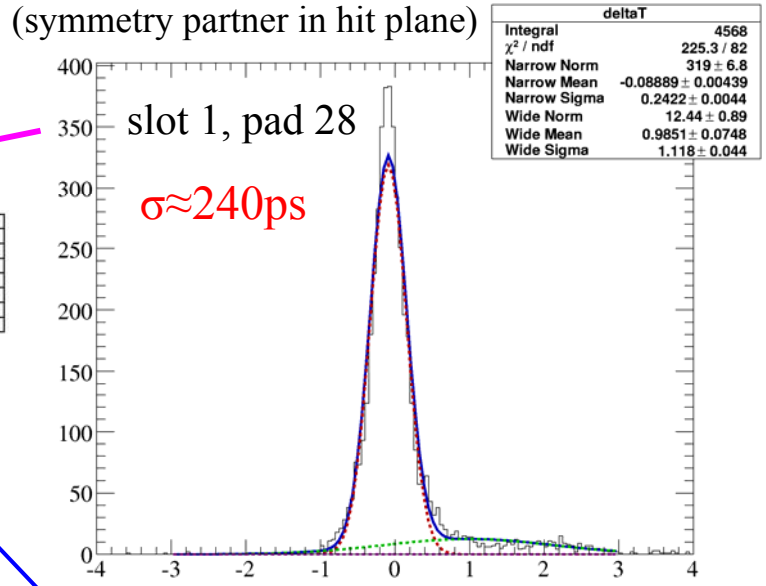
- Up to 7x64 channels per cPCI card
- CAMAC card for SLAC beam test
- Up to 32,256 channels/cPCI crate

Very cost effective, board hardware already exists

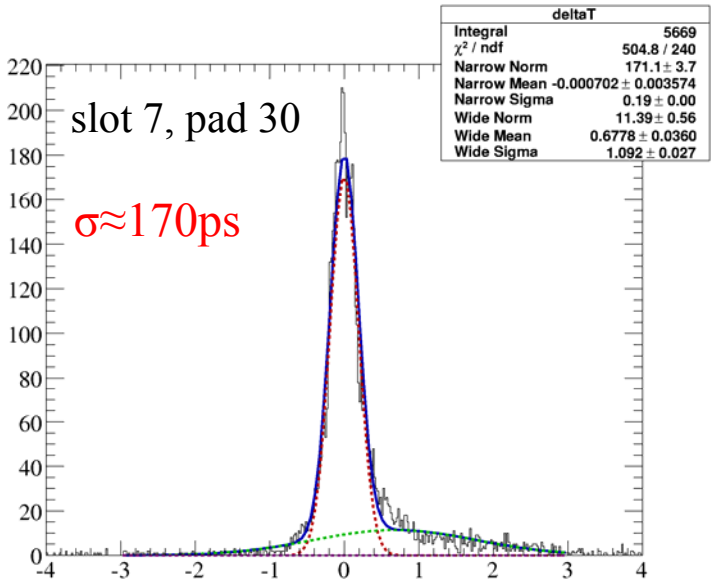
Comparison of UH timing slot 7, pad 15
to Philips slot 1&6
for run 27, pos 1, direct photons



(symmetry partner in hit plane)

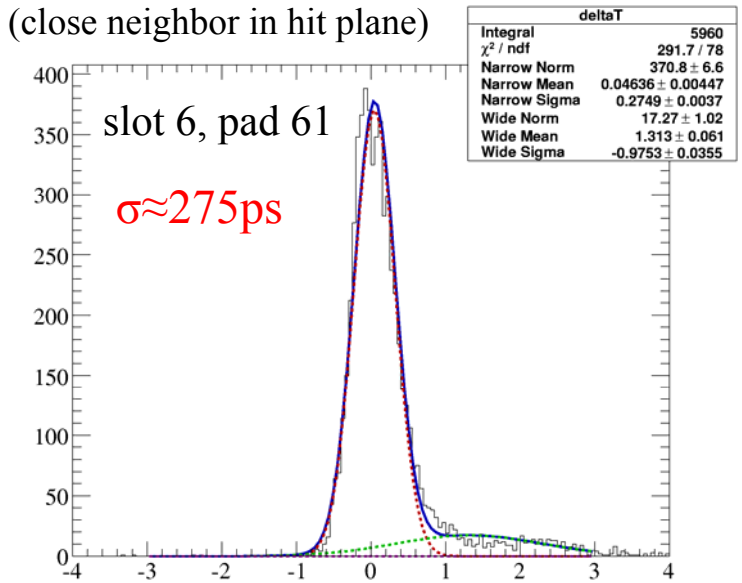


SLAC custom CFD + Philips ADC/TDC



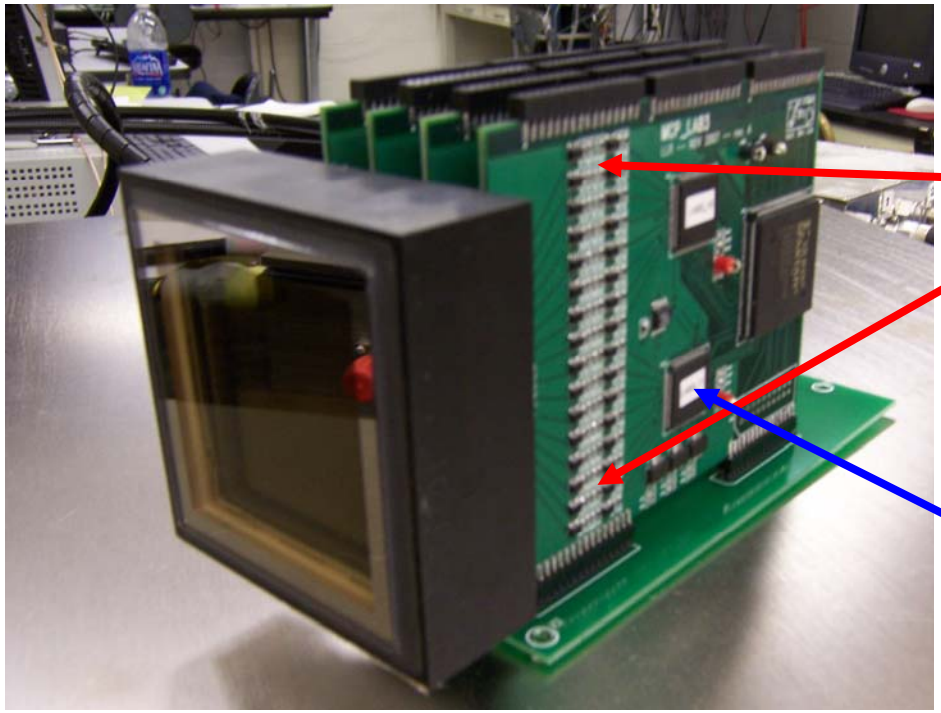
Jochen Schwiening analysis (preliminary)

(close neighbor in hit plane)



delta(time) (ns)

Gain Needed



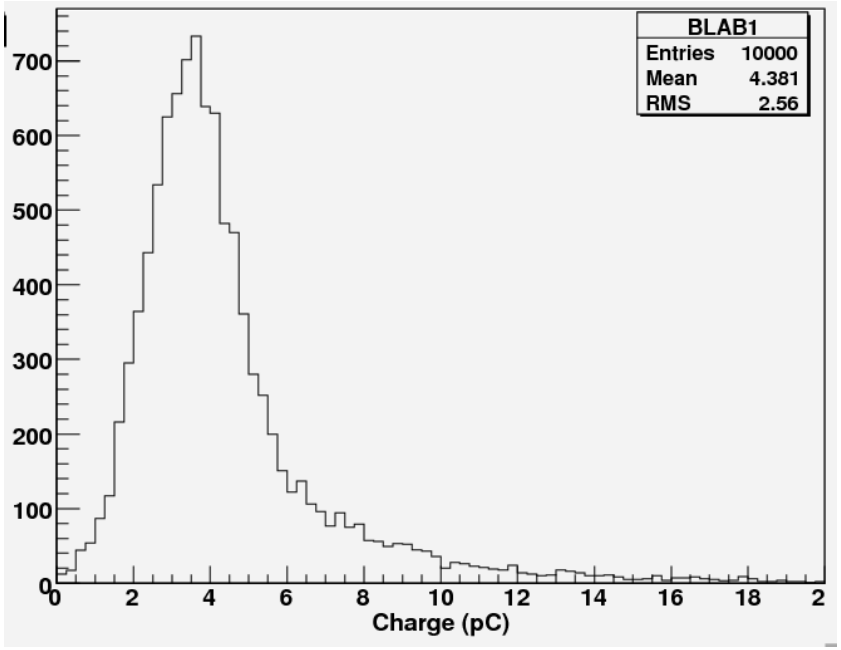
Amplifiers dominate board space

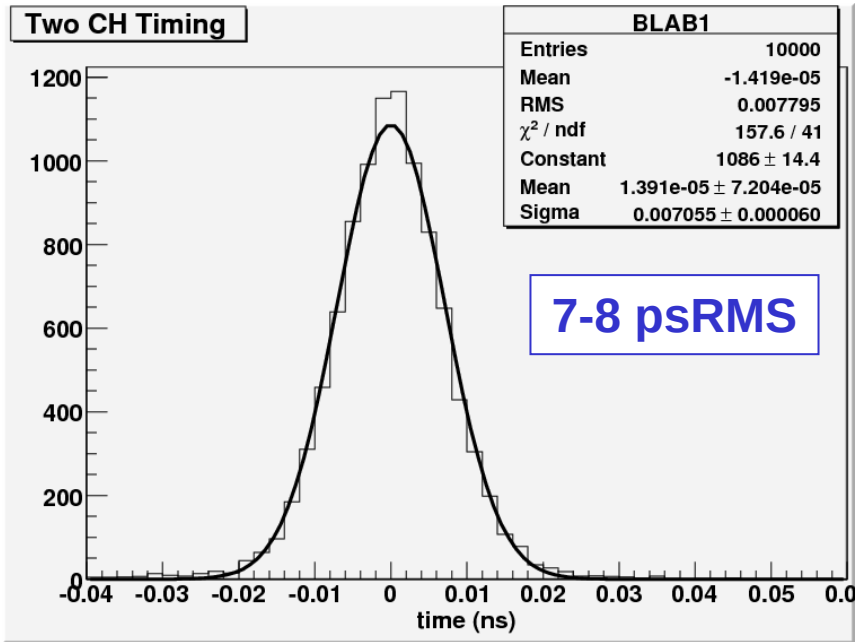
Readout ASIC tiny (14x14mm for 16 channels)

- What gain needed?
  - At 10^6 gain, each p.e. = 160 fC
  - At $2x10^5$ gain (better for aging), each p.e. = 32 fC
  - In typical ~5ns pulse, Vpeak = dQ/dt * R = 32uA * R = 32mV * R [kΩ] (6.4mV)

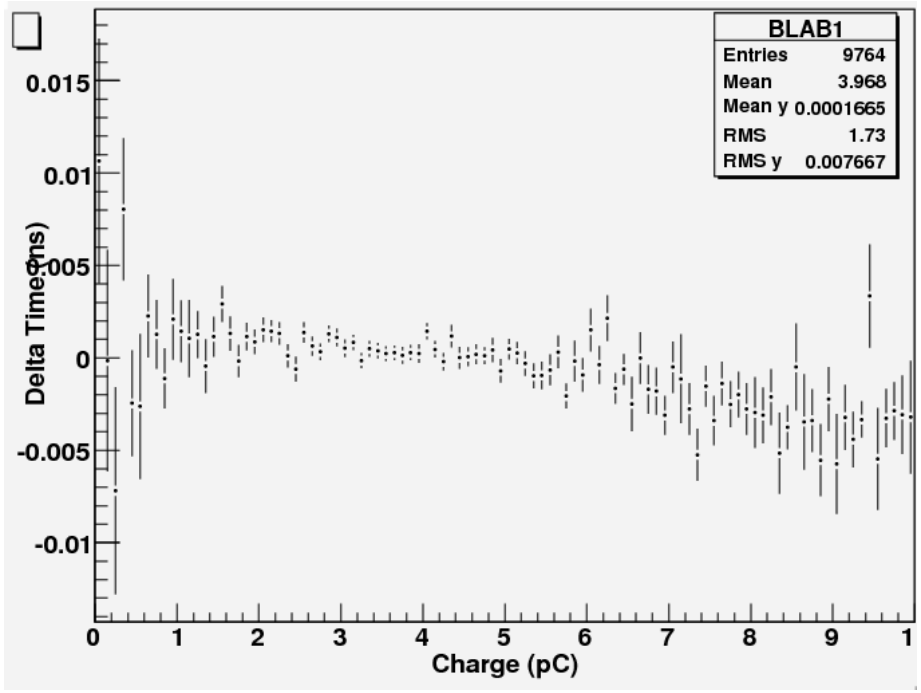
Gain Estimate	
Rterm	**1 p.e. peak**
50	1mV
1k	20mV
20k	400mV

Real MCP-PMT Signals (with BLAB2)





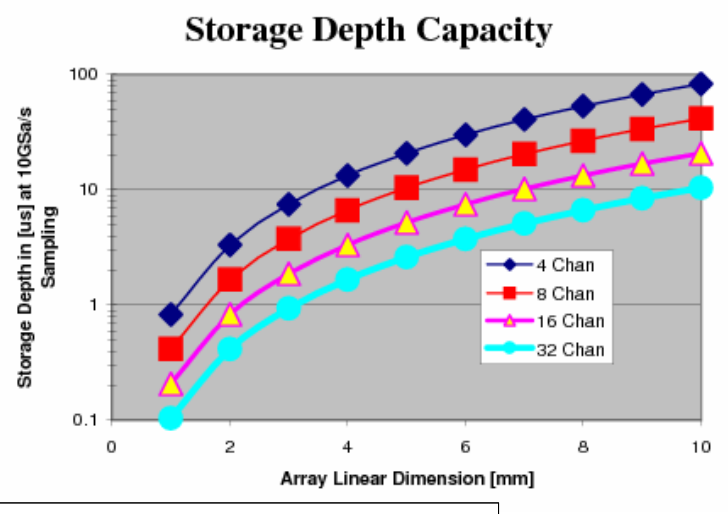
Residual Time Walk

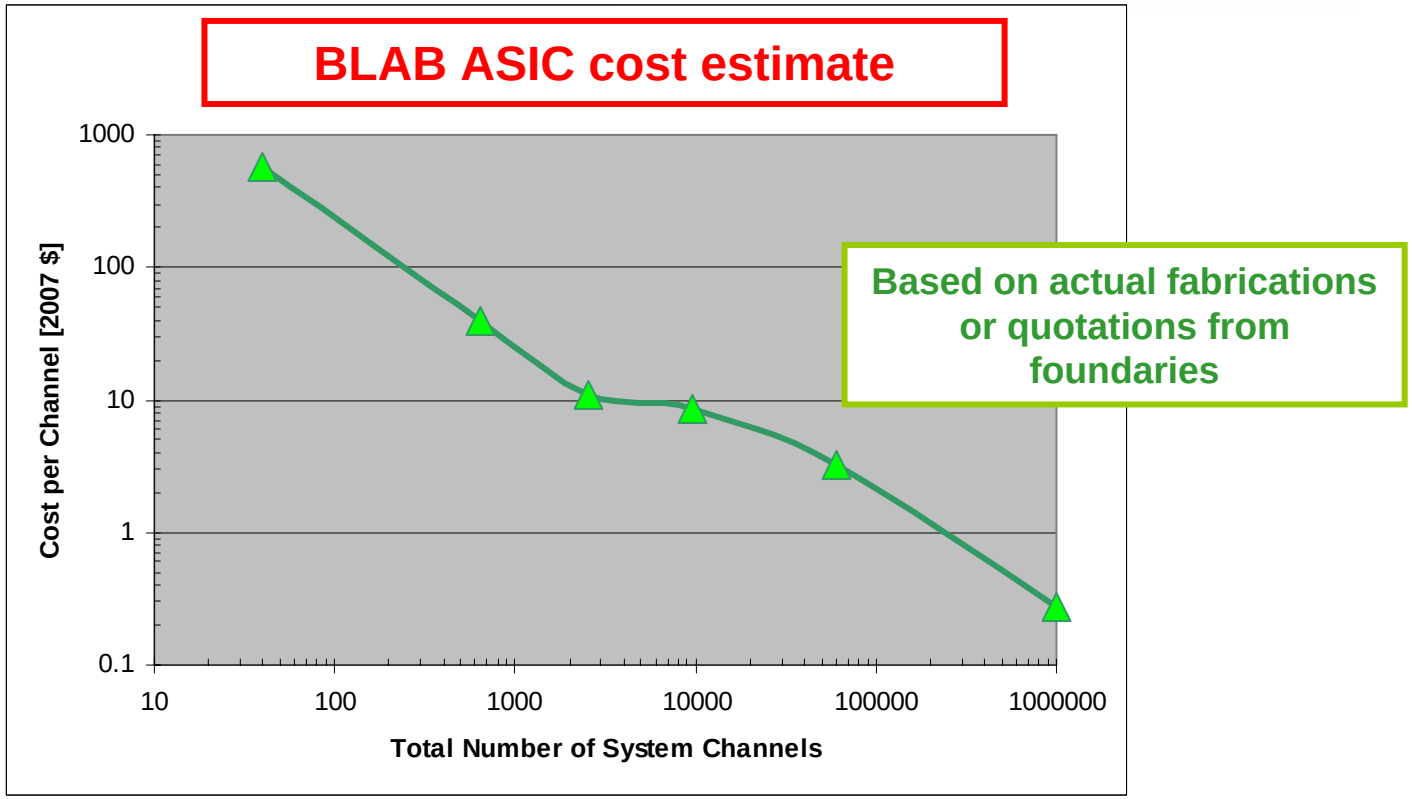


Rather robust for amplitude invariant signals,
TOF still hard, but can shape extract

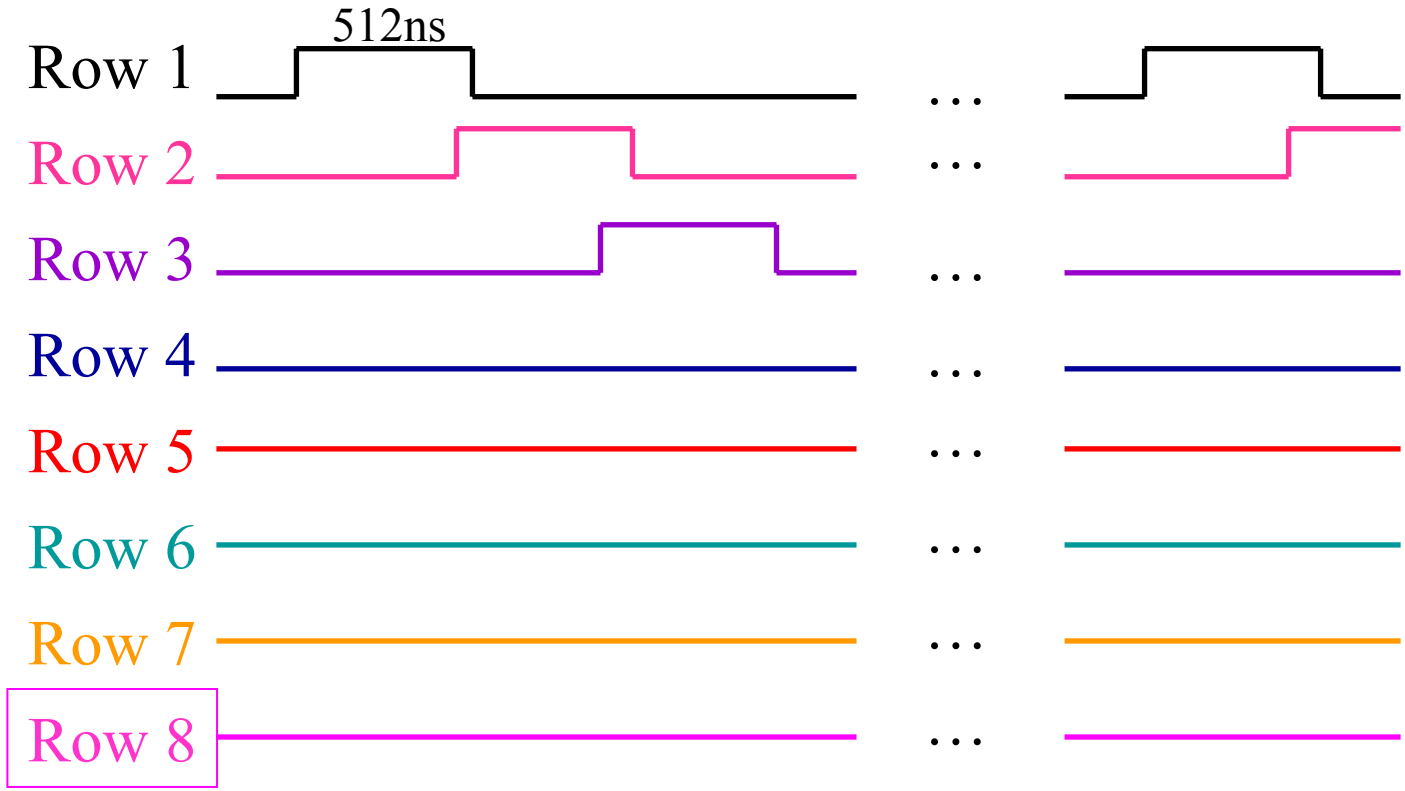
BLAB2 Density and Cost

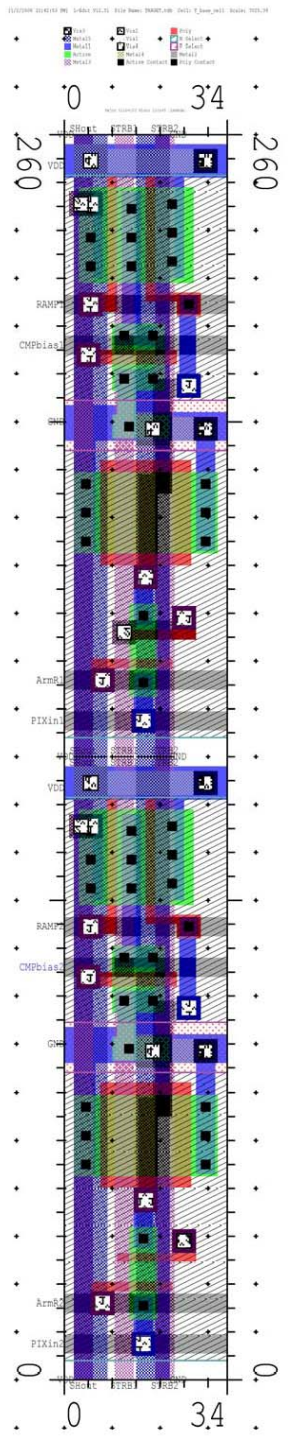
- 16 input channels
- For large-scale systems, cost very competetive





Storage Mode





- Storage configuration (4k samples [~4us])
  - 16 channels, each of 8 rows of 512 samples
  - Overlapped, continuous sampling (window select)
  - Readout: select 16ns tick and read with nearest 16ns
  - Multi-hit buffering (only block 1 row), continue sampling
    → 10% deadtime → 1% deadtime (30kHz, 30us)