3D Tracking in the Level 1 Trigger

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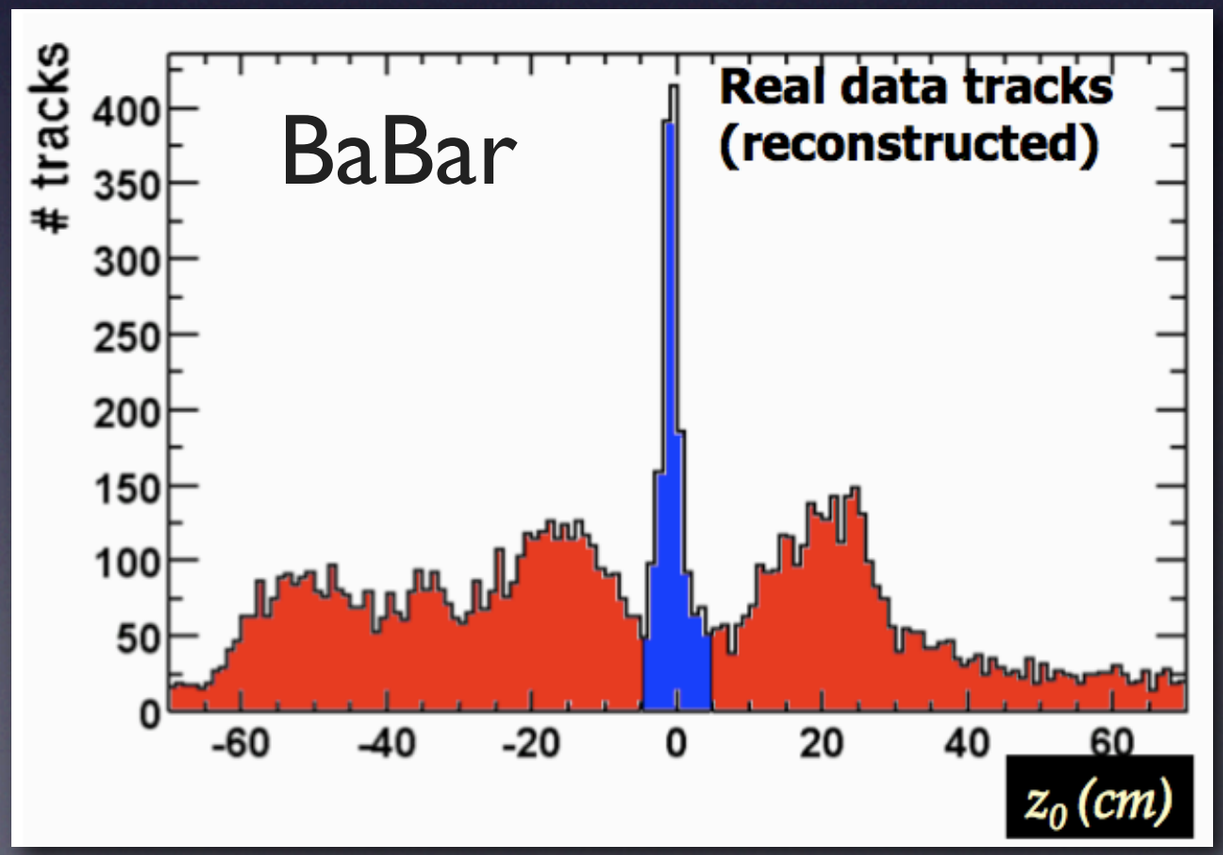
- ✓ Main Idea (from our friends)
- ✓ Implementation strategy to sbelle
- ✓ Resources

Level 1 3D Tracking in BaBar

- BaBar track trigger upgrade (2004) introduced a 3D track trigger in the L1 stage (IEEE NS 2, 1288 (2003))
- Calculation of tandip, pT, and z0 are done in FPGA
- Main idea: cutting on z0 will improve S/N significantly

You get all the public information from http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/upgrade/fdr/ and from http://www.hepl.harvard.edu/annual_reports/doe_site_visit_2004/BABAR/ZPD_Won.PDF and some of which I show today



Tracks originated from physics : z0~0

From background : |z0| >> 0

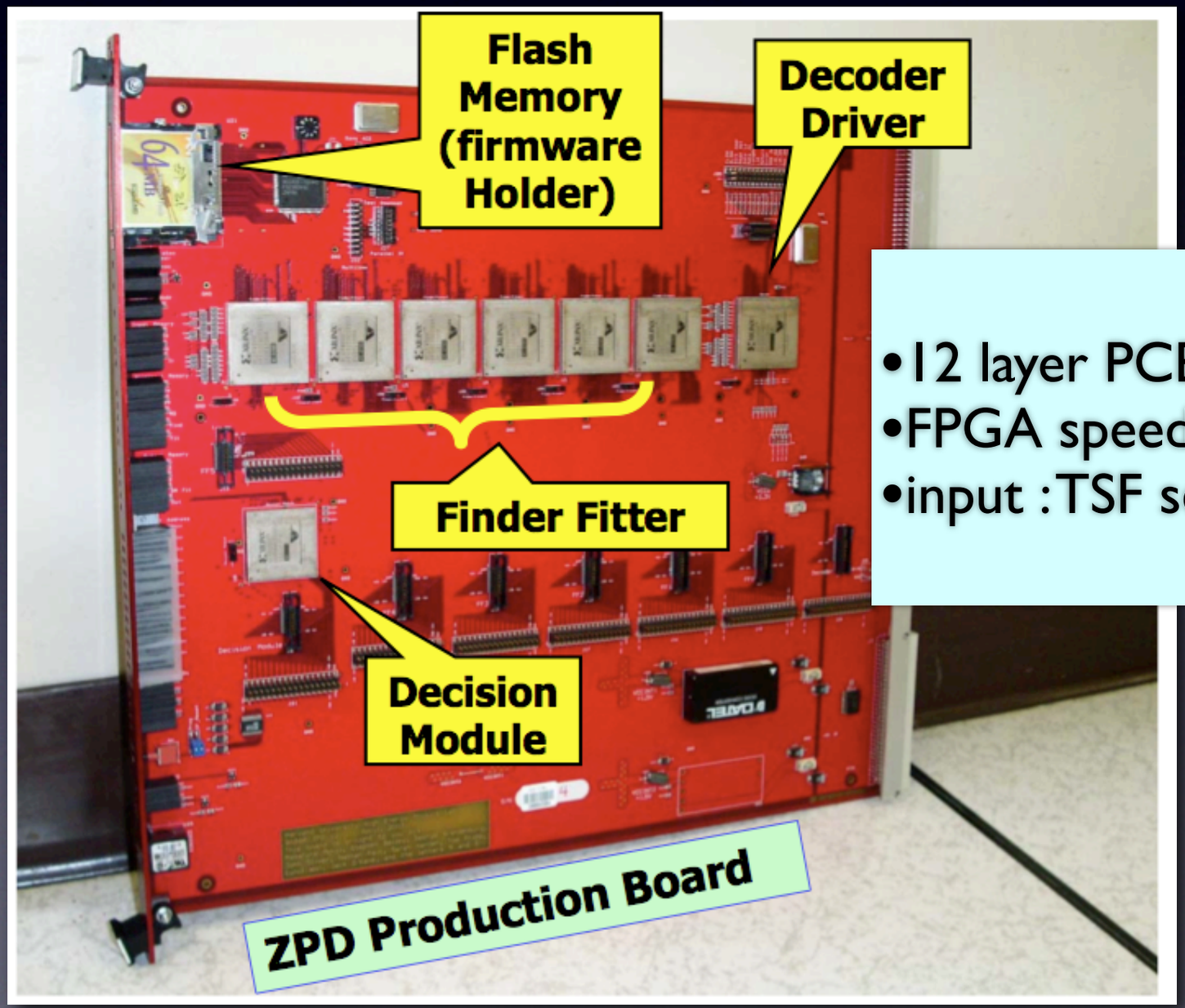
Calculation of z0 at the trigger level : tremendous help in rejecting background

Hardware Configuration

- VME 9U (EURO card) + J3/P3 for BaBar specific data/ control bus (fully pipelined)

Fastest as of 2001-2

- 8 FPGAs on board (6 Xilinx Vertex2 XC2V4000 + XC2V3000 + XC2V1000)

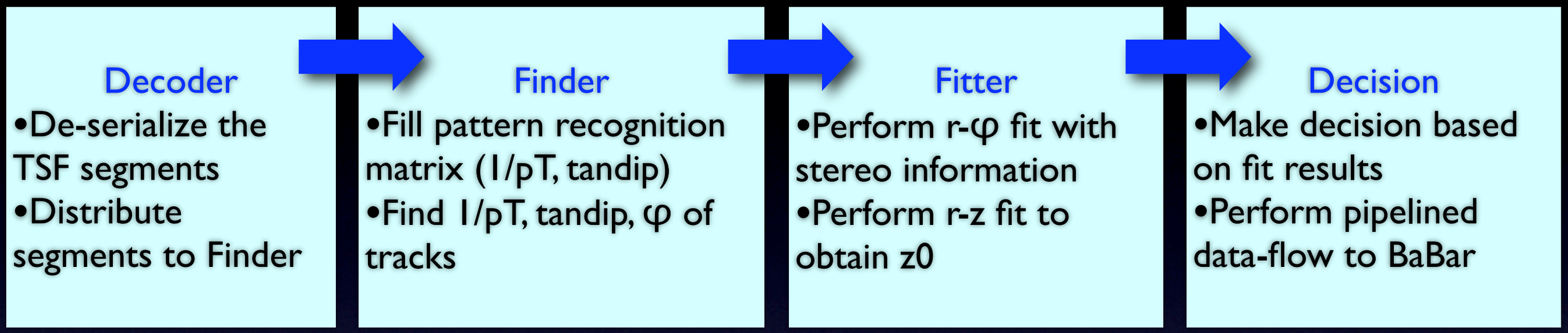


- 120 MHz (main algorithm)/60 MHz (decoding/decision) clocking

•12 layer PCB design
•FPGA speed grade: -4
•input : TSF segment from J1,2/P1,2

- Firmware loading via CF card (in total 8 different sets can be stored)
- One board covers 3/8 of 2π : total 8 boards with overlaps

Algorithm & Firmware

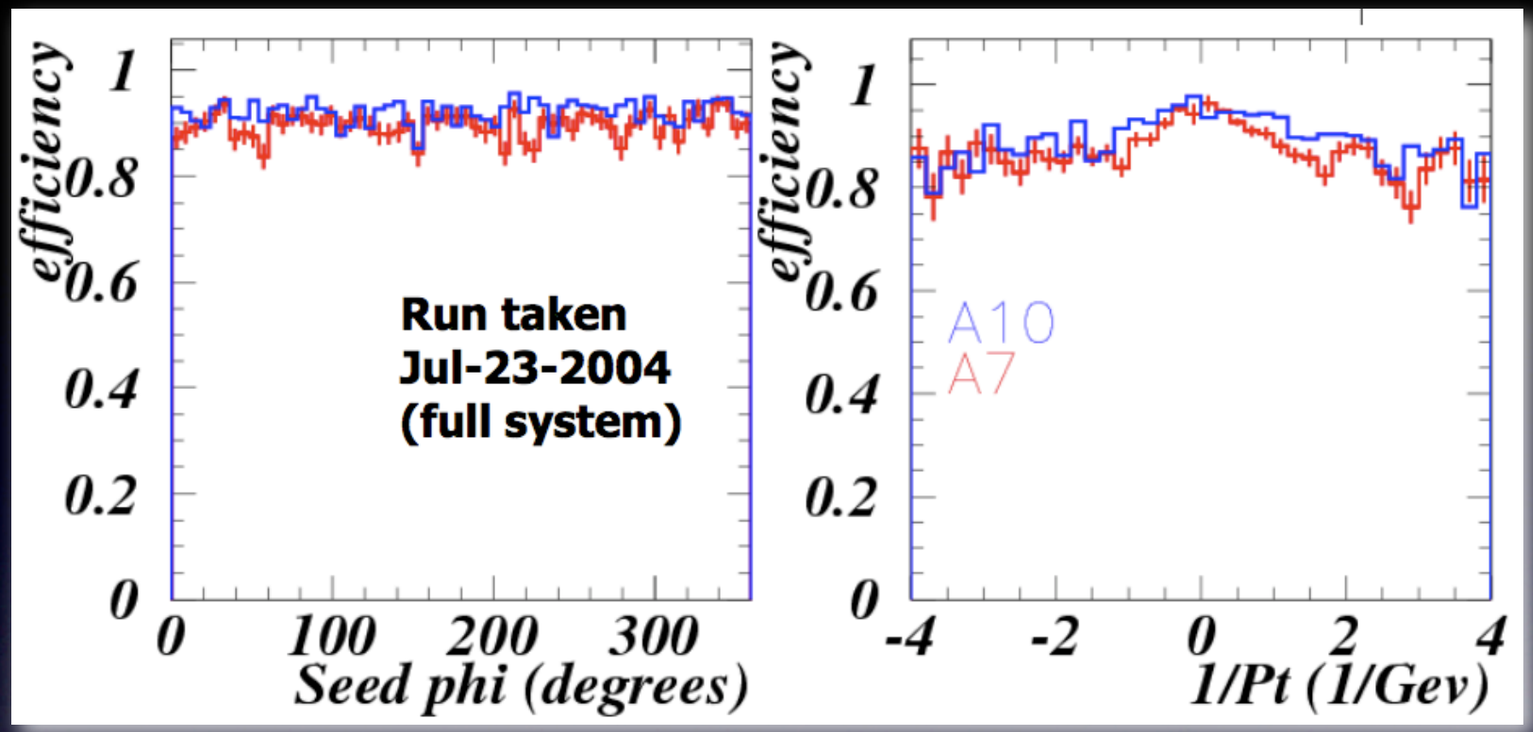


Latency distribution(*)	36 ticks 600 ns	60 ticks 500 ns	96 ticks 800 ns	6 ticks 100 ns

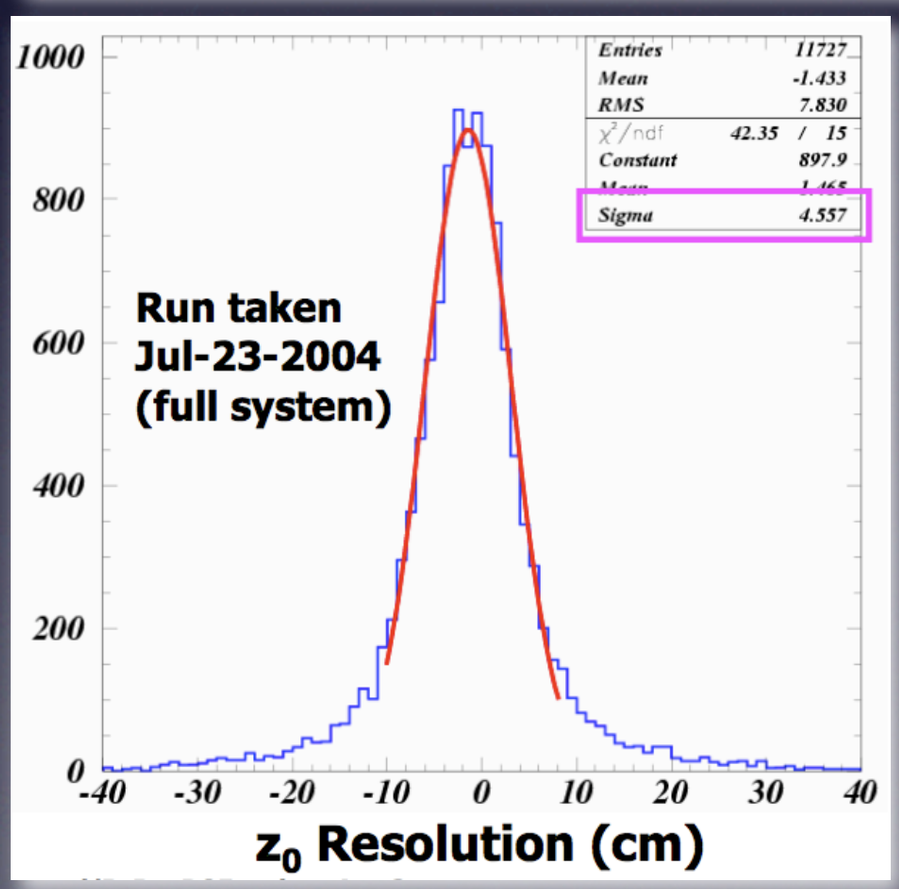
- Latency constraint: ~2.0 us (or in total ~200 clock ticks)
- VHDL codes: developed for 3 years with 2 full time good(?) physicists
- Entire algorithm verified with C++ and VHDL down to single bit level
- Each module has a memory block that "play&record" data for easier debugging of the firmware (For sBelle, we have to rely on CSR r/w through VME protocol)

(*) All numbers are approximate

Performance of BaBar 3D Track Trigger



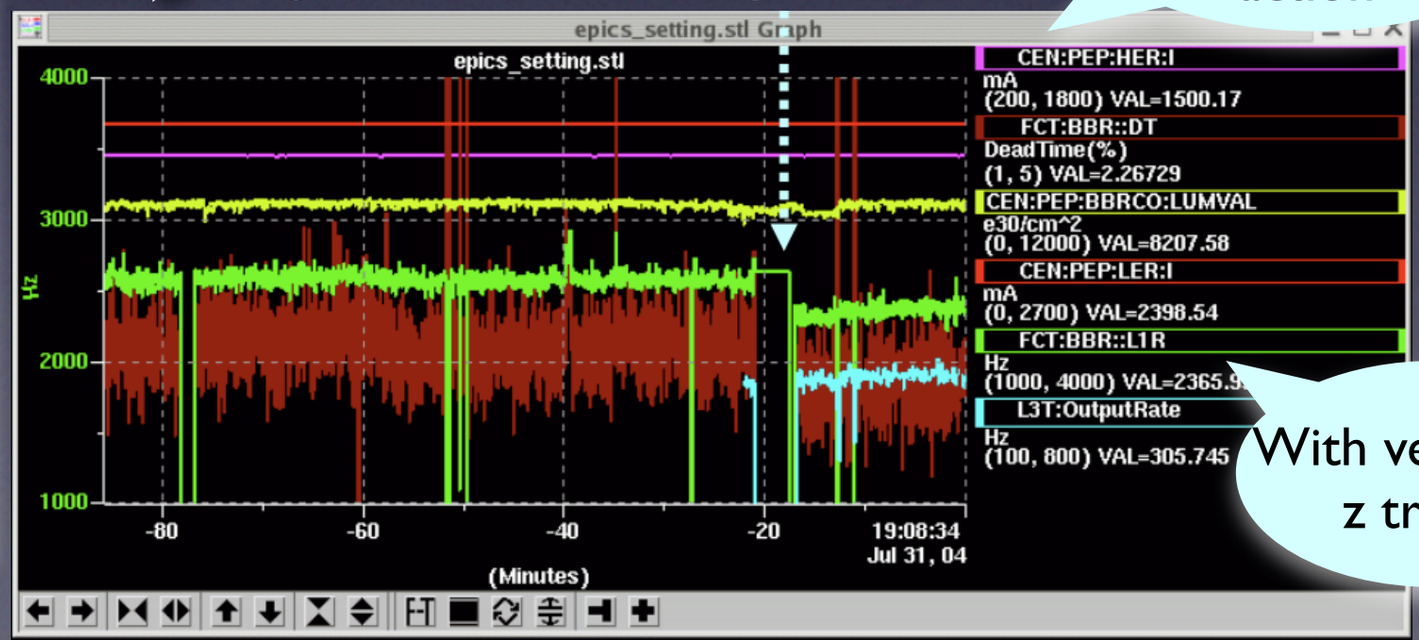
High efficiency (~90%) over full 360° and wide range of pT



The z0 resolution is ~ 4.6 cm and is in good agreement with their simulation

This is precise enough to select signal tracks exclusively

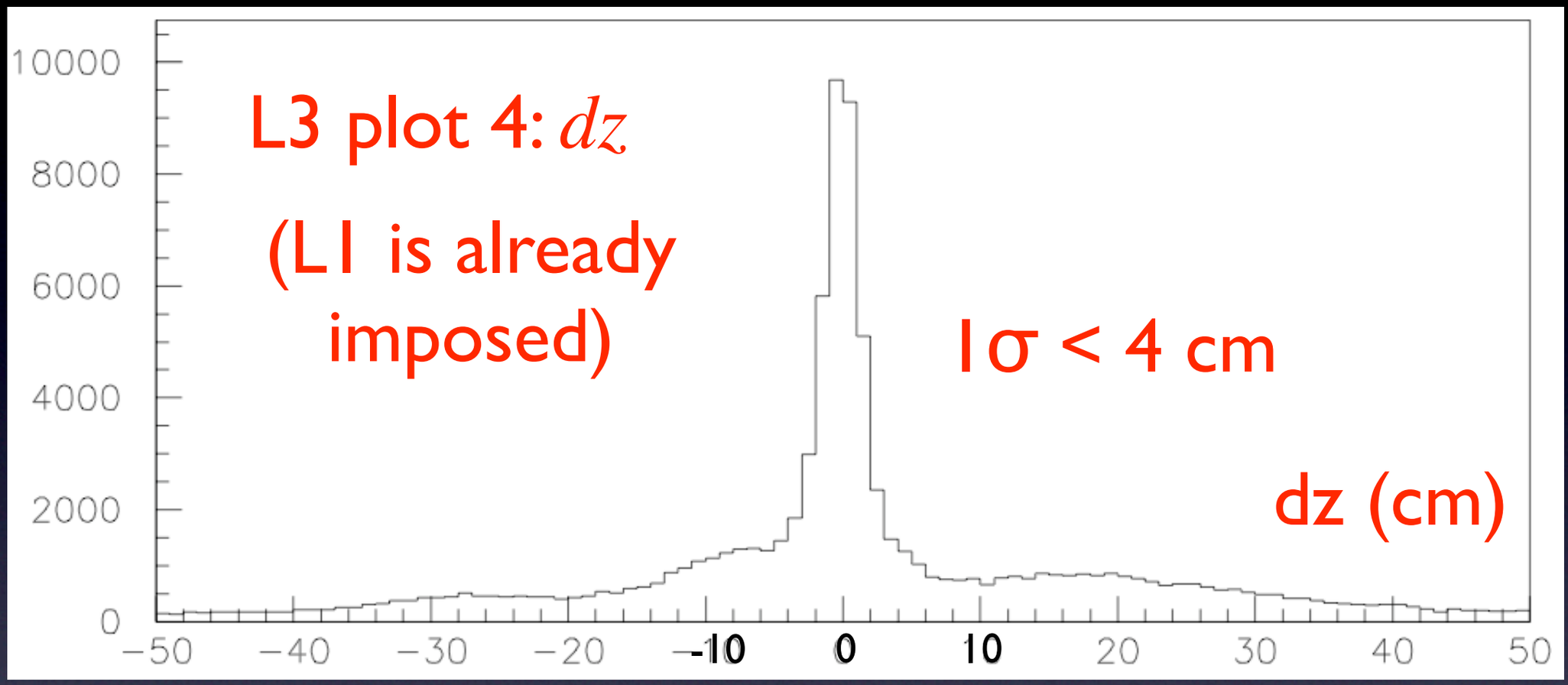
EPICS snapshot at the trigger in action



With very loose z trigger

Situation in (s)Belle

- "Current" Belle z distribution of tracks (from DQM manual)



- z distribution from random trigger will give us better understanding on the present situation

➡

- We gain L1 trigger rates from z-trigger : how much ? Depends really on the background situation at sBelle

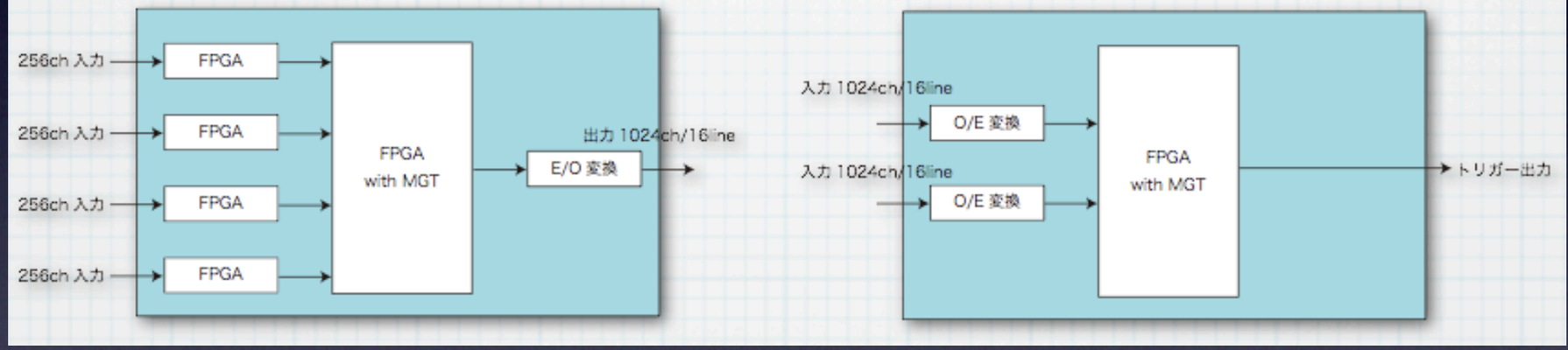
Situation in sBelle

- There is a hardware upgrade plan for track triggers/GDL in sBelle trigger scenario driven by Y. Iwasaki san

- Make TSF using axial and stereo wires
  - ~2000 TSFs
  - Hugh I/O board is preferable
- New I/O boards are under design
  - First stage multiplex TSF input
  - Second stage receives whole TSF information
    - Apply Hough and stereo finding logics

2007.3 TRG/DAQ meeting
Y. Iwasaki

This part is obsolete



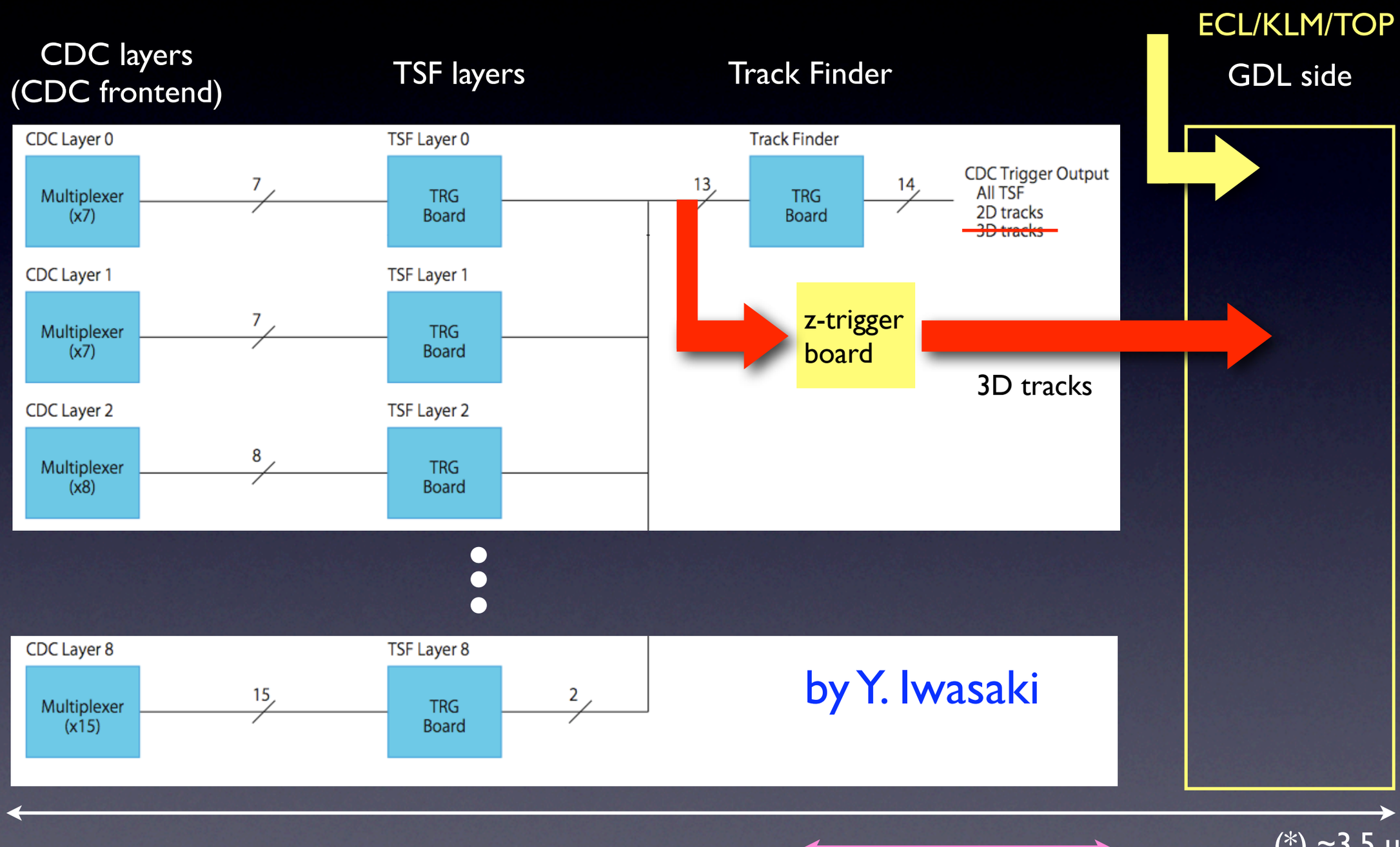
- Iwasaki san presented 3D tracking as

- Output
  - Track dz and momentum,
  - accurate track counting,
  - accurate momentum valance,
  - cosmic veto (by a line pattern search)

- I propose to develop algorithm to produce z0, similar to what BaBar did with their L1 track triggers

Situation in sBelle

- Current Idea for new CDC readout (From Y. Iwasaki, trigger part) + my initial thought (z-trigger part)



(*)~500 ns from z-trigger

* latency from discussion with Y.Iwasaki/T.Tsuboyama

Is this realistic?

Can we produce z0 in sBelle?

- The number of ticks we are going to have?

latency for the calculation of z0	number of ticks
0.5 us (entire trigger 3.5 us)*	20 @ 40 MHz
	40 @ 80 MHz
0.5 us	250 @ 500 MHz

* latency from discussion with Y.Iwasaki/T. Tsuboyama

80 MHz if we double clock with DCM

Modern FPGAs are advertised to run at as fast as 500 MHz at least (Xilinx Vertex5 series)

➡ I assume 250 ticks is long enough for producing z0 and the new board will host something similar to Vertex5

- We need stereo as well as axial TSF segments to begin with

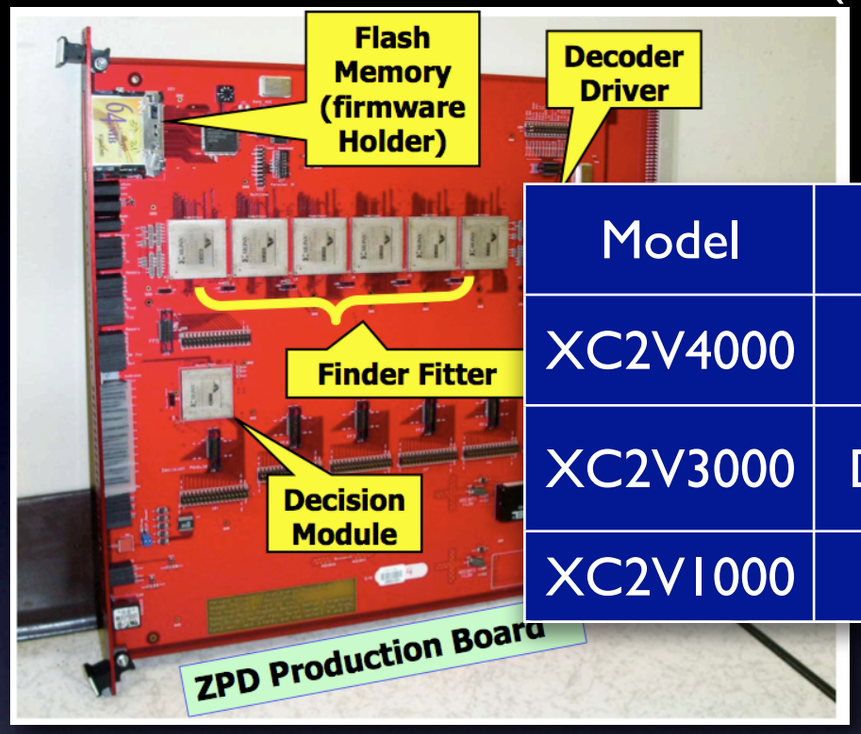
➡ I assume Iwasaki san's new TSF will deliver stereo segments as well to the board

- Do we have enough resources and experts?

➡ I am fairly familiar with VHDL but less with track fitting and almost nothing with pattern recognition for track finding

Can we produce z0 in sBelle?

- BaBar has one board (has 8 FPGAs) for 1/8 of 2π



Model	Function	CLB	Usage
XC2V4000	Finder and Fitter	23,040	44%
XC2V3000	Decoder and Driver	14,336	27%
XC2V1000	Decision Module	5,120	70%

Total 23040*6+14336+5120=160k (17.6k)

Grand total: 160k*8=1.2 M blocks (140k)

(weighted by usage: but place&route nontrivial if usage is high!)

- If we use Vertex5 (the lastest, largest, and fastest from Xilinx as far as I know. Does Altera have better ones?)

Model	CLB
XC5VLX330	51,840

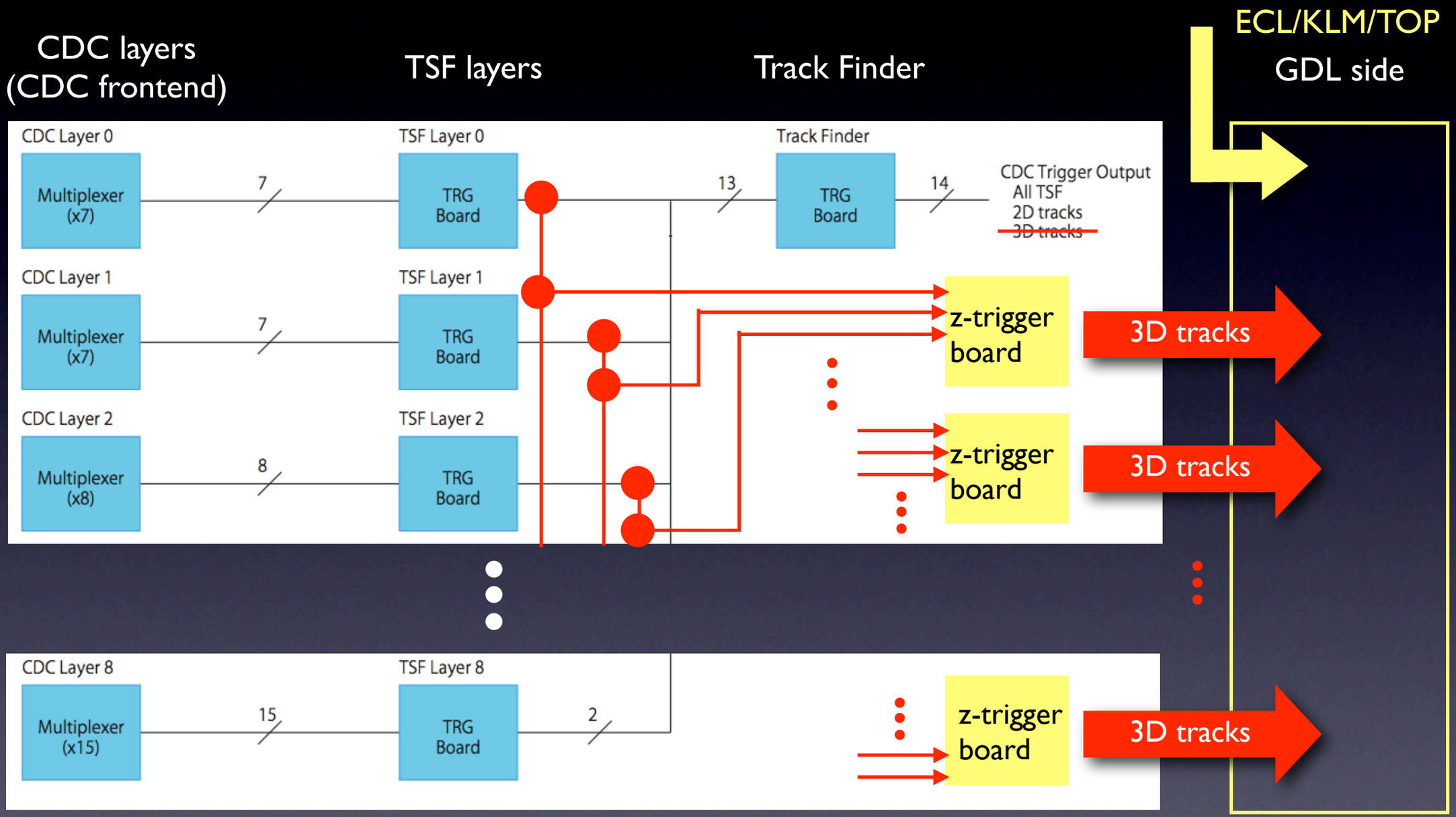
No way we can fit into a single board

One board covering 1/8 may be OK

(Note: TSFs are grouped in layers, not in phi)

Realistic Scenario ?

- We use TRG boards (no extra development in hardware)



- 8 z-trigger boards receiving 9 Rocket I/O via optical cables

Plans and Resources

- I believe it is worth trying: then we have two choices (usual 2D track triggers vs possible 3D fit)
- To do

  Full GEANT4 CDC trigger simulation to obtain TSF segments :
  tick by tick simulation is crucial

  Develop algorithms with C++ to extract z0, pT, tandip

  Translate them into VHDL (or verilog)

  Who will do all these?

  Eunil Won : VHDL coding

  Dr. Byeongrok Ko (0.3 FTE), Dr. Boyoung Han (0.5 FTE Korea University) : rest of the other work

  They have experience with offline tracking in CDF

- Let me know if you want to join this work