Summary of PXD Session

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1 Status of CAPS	H. Hoedlmoser (Video)
2 Status of SOI	Y. Arai
3 DEPFET Project	C. Kiesling
4 Status of DEPFET R&D	L. Andricek
5 DEPFET test beam	P. Kodys

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Vertexing at SuperBelle

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Increased background
⇒Radiation damage
⇒Occupancy

Shorter readout times (SVD with APV25)
Higher granularity: pixel detector
79mm => 75 μm: factor 1000
however: 10 μs integration time:
factor 100 improvement

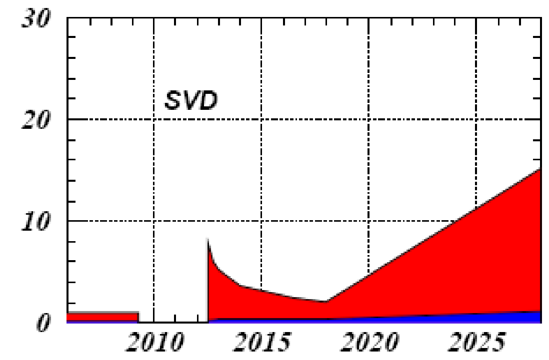
Improve performance?

$$\phi_{\text{MS}} = \frac{13.6\ \text{MeV}}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln \left(\frac{x}{X_0} \right) \right]$$

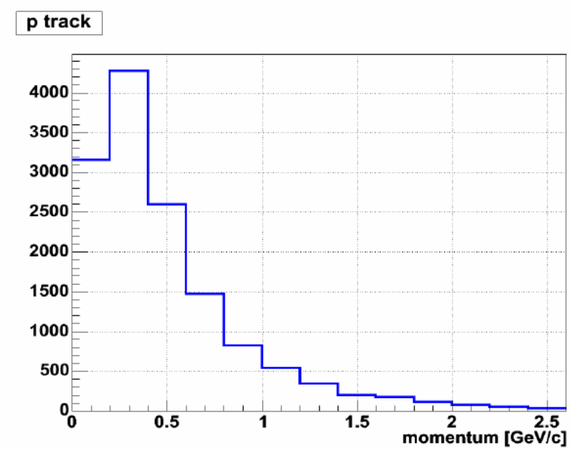
Beam pipe: 0.66% X_0 @ 1.5 cm:
σ_{ip}(MS) = 17 μm for 1 GeV/c (normal incidence)

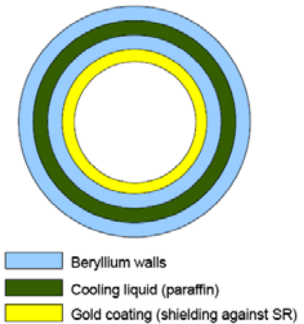
No need for very small pixels! 50 x75 μm^2 ok
It's the material! => thin silicon!

Keep beam pipe radius small !
Keep beam pipe thin!



Momentum spectrum of tracks in ee→BB sample





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CAPS

Binary CAPs

H. Hoedlmoser, Hawaii

CAP4 AMS 0.35 mm Opto
(E. Martin)
- Study of new analog and binary designs

Chattering pixels

CAP5 SOI prototype
(E. Martin)
- Study of 0.15 mm Fully Depleted OKI process

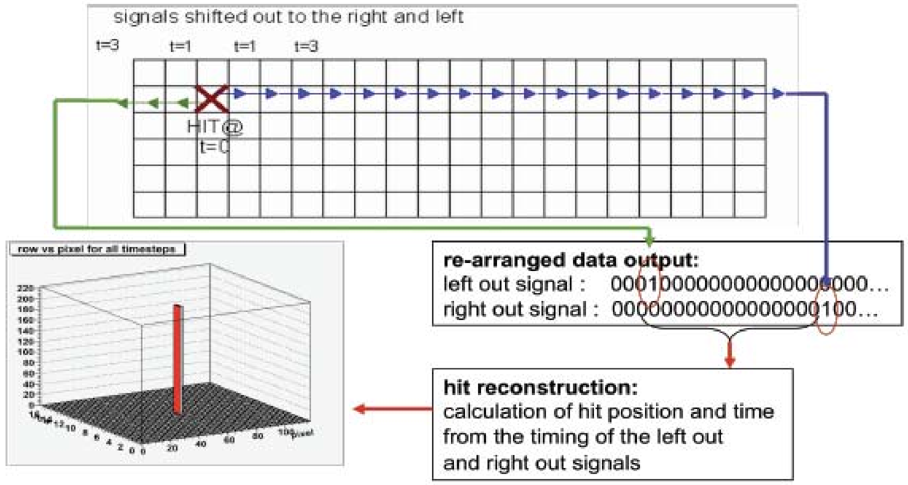
Problems due to SOI process

CAP7 SOI
(M. Cooney)
- 0.2 mm OKI SOI process submitted 01/2008
- improved binary design from CAP5

Latch instead of flip-flop
No chatter
Back 11/2008

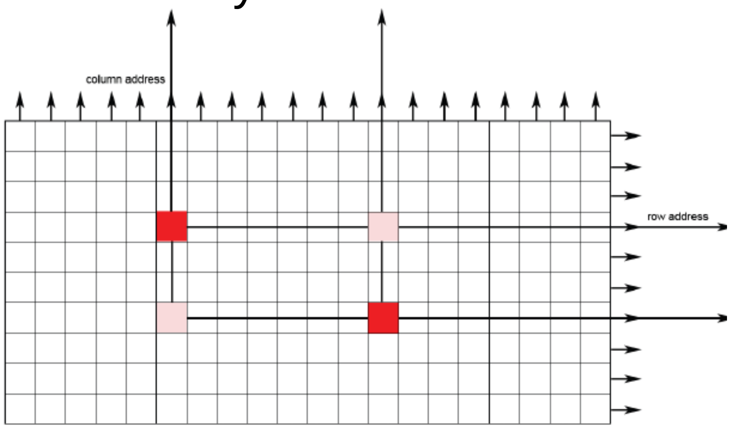
CAP6 hexagonal binary design in AMS 0.35 mm Opto
(M. Cooney)
- completely new readout concept
- submitted 10/2008

Binary readout

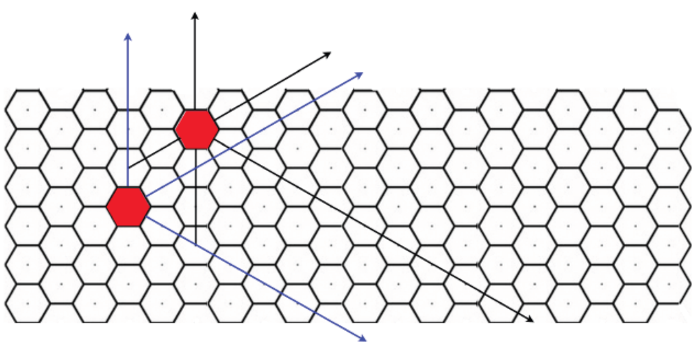


CAP4 design
Problem: ghost hits

Also for x-y readout



No ghosts for hexagonal readout



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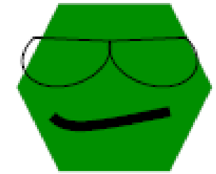
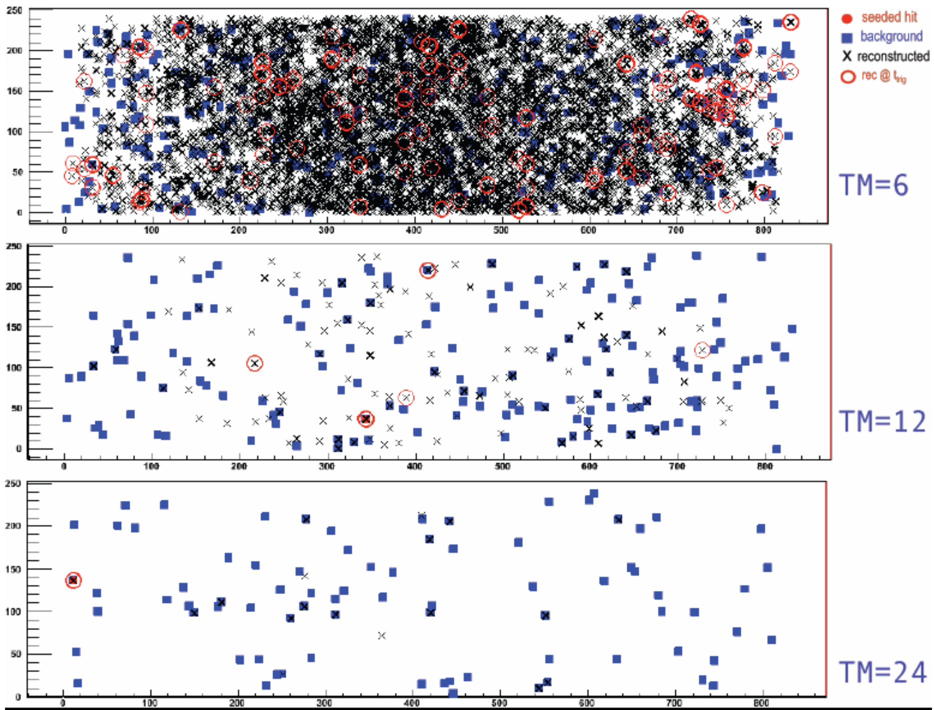
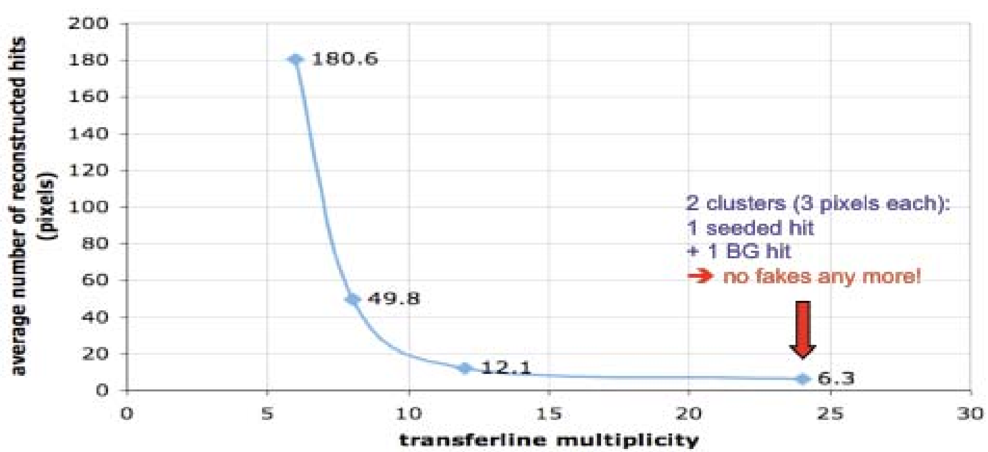
HIXEL DETECTOR





21x6 mm^2 array 25 μm square pixels
100 MHz transfer in periphery
12 transferelines
72 outputs
Occupancy: 5.2 x 10^{-5}
@ 30 times current background

(frame readout: ~ 10^{-2})



Prototyp (CAP6) in production

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SOI R&D

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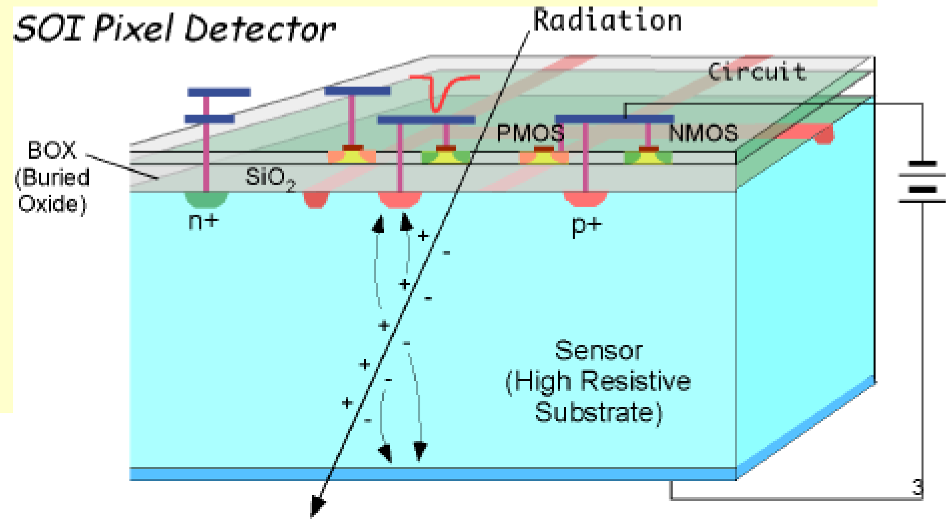
Features of SOI Pixel Detector

- Bonded wafer : High Resistivity (Sensor) + Low Resistivity (CMOS) .
- Truly Monolithic Detector (-> High Density, Low material, Thin Device).
- Standard CMOS can be used (-> Complex functions in a pixel).
- No mechanical bonding (-> High yield, Low cost).
- Fully depleted sensor with small capacitance of the sense node (~10fF, High conversion gain, Low noise)
- Based on Industrial standard technology (-> Cost benefit and Scalability)
- No Latch Up, Rad Hard.
- Low Power
- Low to High Temp (4K-300C) operation
- ...



Y. Arai

KEK SOIPIX History

'05. 7: Start Collaboration with OKI Elec. Co. Ltd.

'05.10: TEG submission to OKI SOI 0.15 μm process.

'06.12: 1st 0.15 um MPW run hosted by KEK.

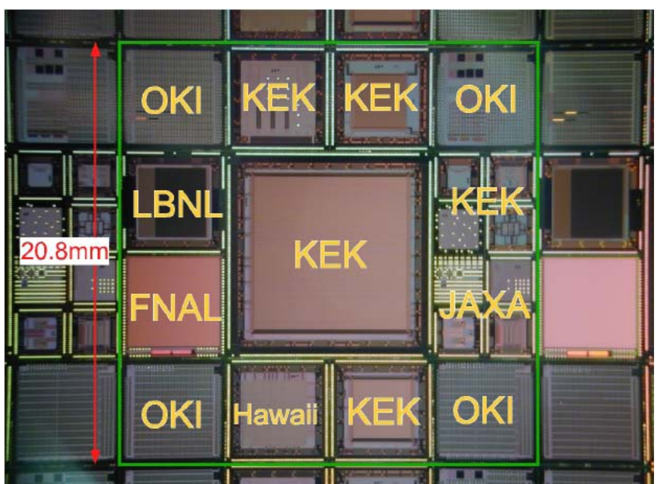
(17 designs; KEK, Japanese Universities, LBNL, FNAL, U of Hawaii)

'07.6: Process (and Fab.) is changed from 0.15 μm to 0.2 μm.

'08.1: 1st 0.2 um KEK MPW run is submitted.

'09.1: 2nd 0.2 um MPW run will be submitted.

'09.6: 3rd 0.2um MPW run is planned.



2008.1 MPW run with KEK, LBNL, FNAL, Hawaii

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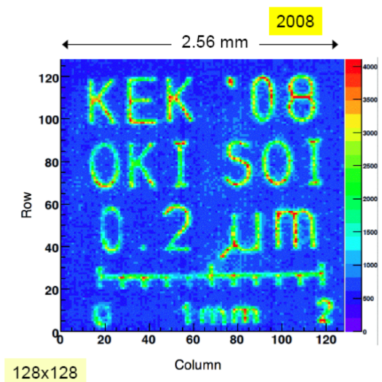
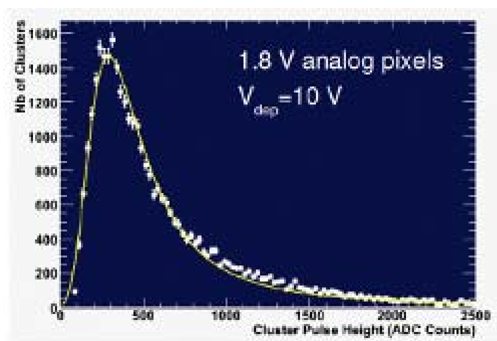
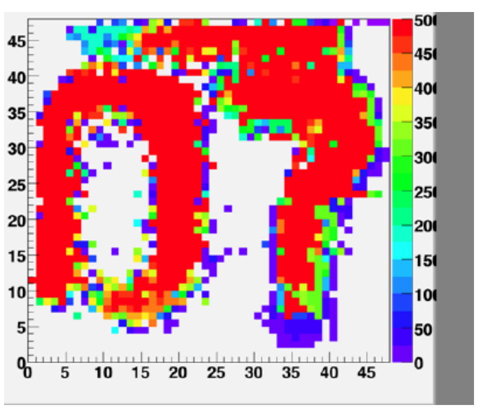
Results

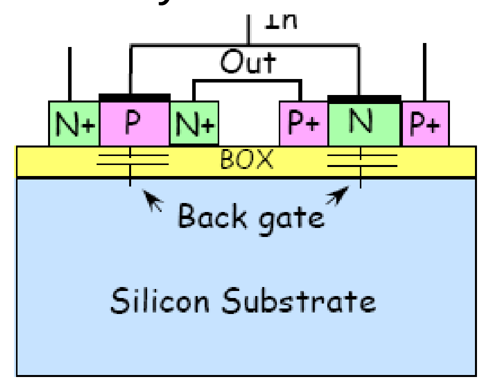


Counting pixels (x-ray imaging)
sBelle pixels: 48x48 pixels (100 x 100 μm^2)

Works, but problems due to back-gate-effect
Successful with x-rays







LBNL beam tests: best S/N (15) at U=10V
Gets worse at higher U (no full depletion)

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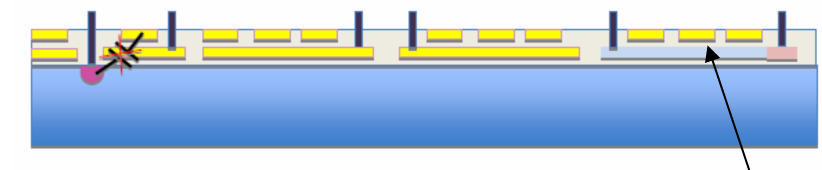
Plans

Double the number of submissions at OKI

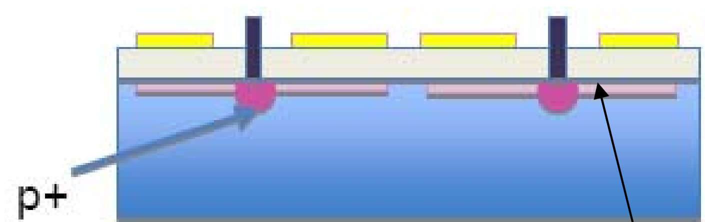
Reduce back-gate-effect:



Second layer to shield substrate

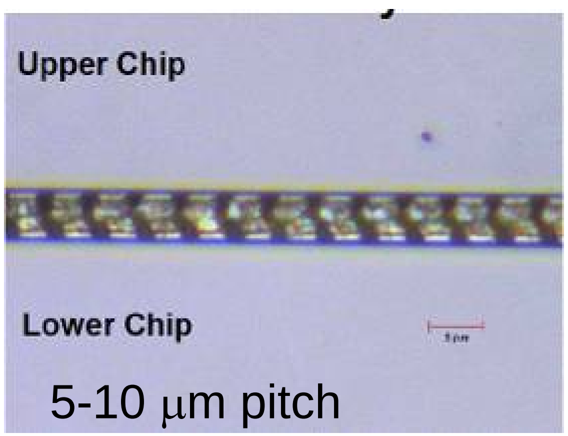
Double SOI

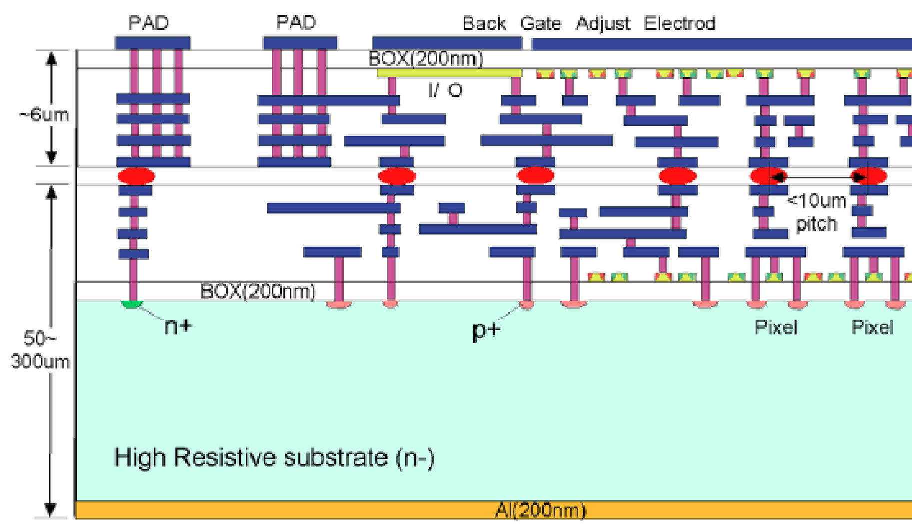
Implant through BOX



Reduce field under oxide

3D/SOI Project (with ZyCu
To be bonded in April 09





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DEPFET Status

Each pixel is a p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate
Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

Accumulated charge removed by a clear contact (“reset”)

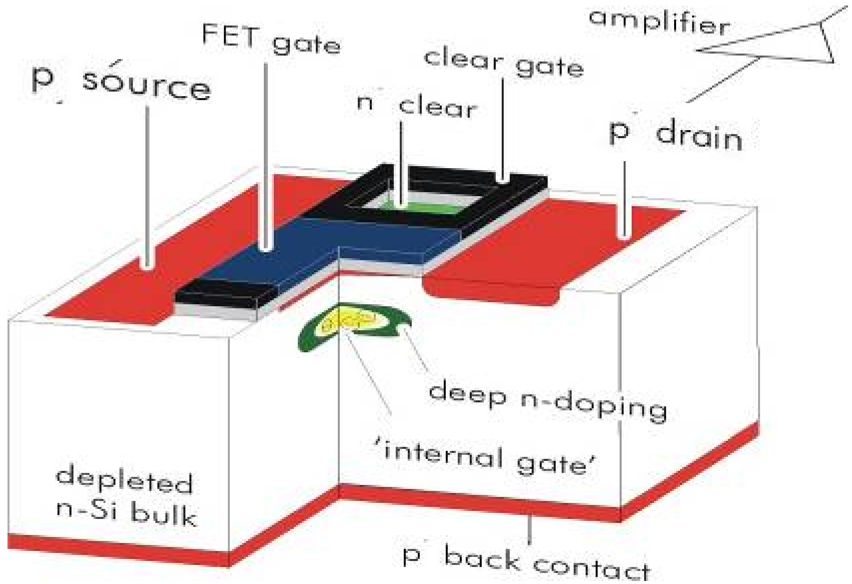
Fully depleted:
⇒large signal, fast signal collection

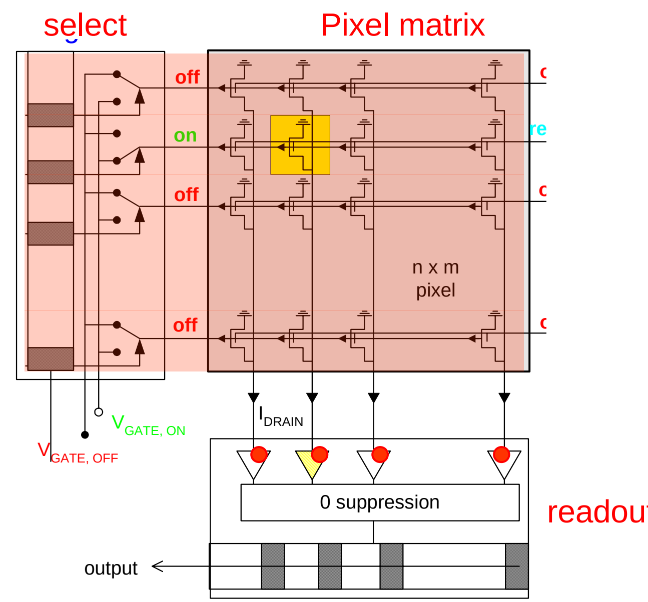
Low capacitance,
internal amplification: => low noise

Frame readout
- => sequential readout of pixels or rows
- => rolling shutter mode
- => integration over many readout steps

frame readout time: <10 μs

- => only few pixels active: low power
- => ASICs at periphery





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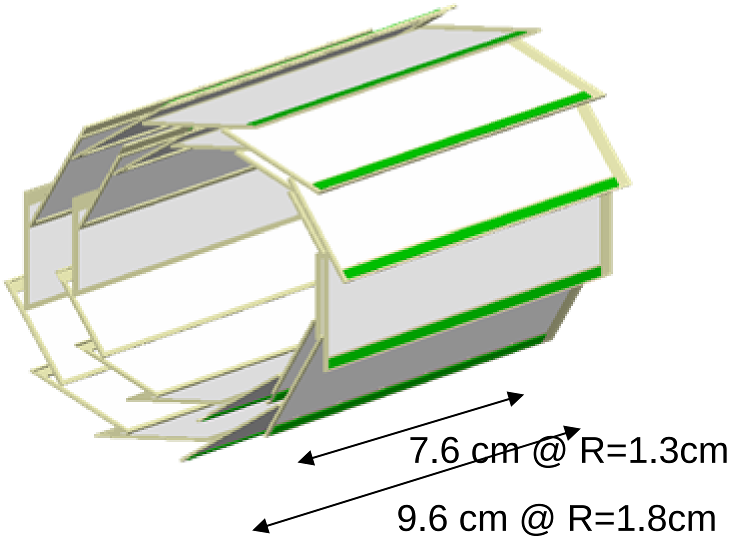
Detector Layout

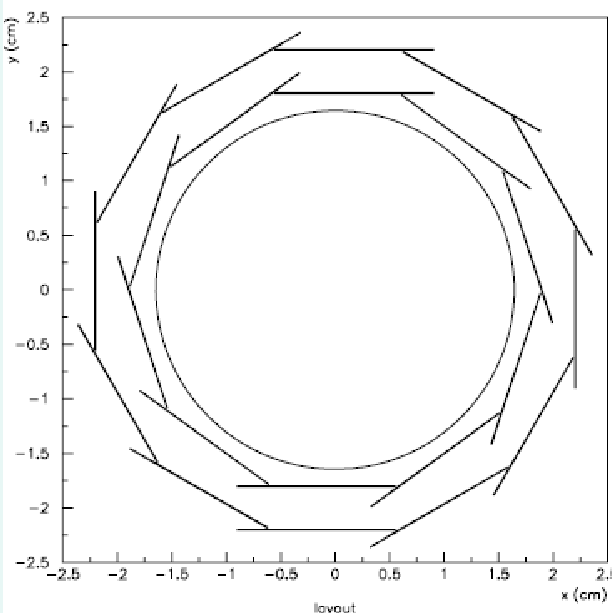


Small Detector:
20 – 24 Modules (one sensor each)

Radii still subject to optimisation:

Beam pipe radius: 1 cm or 1.5 cm?
Probably: 1.5 cm initially with upgrade to 1.0 cm later

Total detector: 6 Mpixel (2 layer)

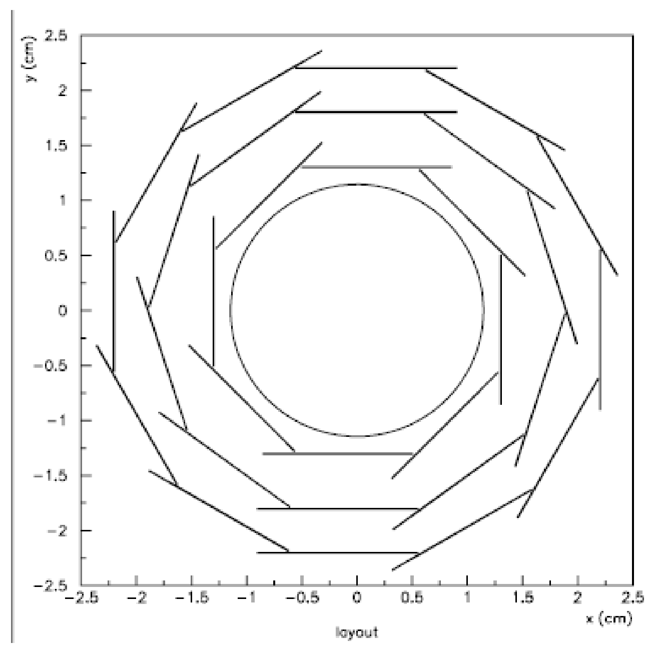


Most likely scenario

Layer 1 at 1.8 cm
Layer 2 at 2.2 cm

Later upgrade:
Layer 0 at 1.3 cm
2 or 3 layers

Depends on machine design



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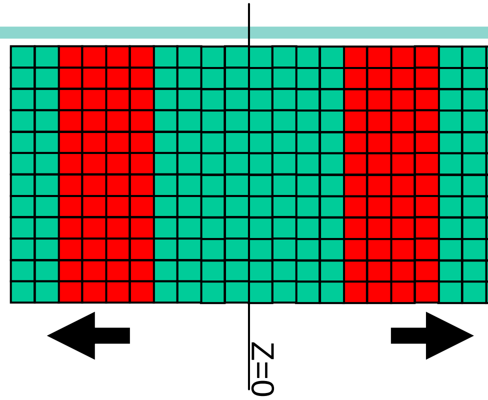
Radius <-> Pitch

Frame readout time < 10 μs
Line readout time: 80 ns
2 x 4 lines per readout step
-> 1000 lines along z

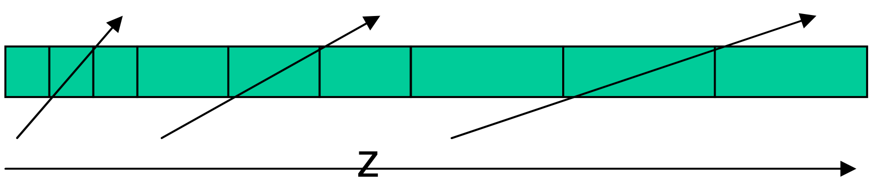


R	L	pitch
1.3cm	7.6 cm	76 μm
1.8cm	9.6 cm	96 μm
2.2cm	11.5 cm	115 μm

Impact parameter resolution in z scales with R^2 !
Extrapolation error ~ R
Intrinsic resolution (pitch) ~ R

Improvement: variable pitch
At large z: larger pitch possible
optimal charge sharing
small cluster size
Central part: small pitch
better resolution

R	Pitch (min)	Pitch (max)
1.3cm	56μm	175μm
1.8cm	87μm	175μm
2.2cm	110μm	175μm



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SuperBelle PXD Module

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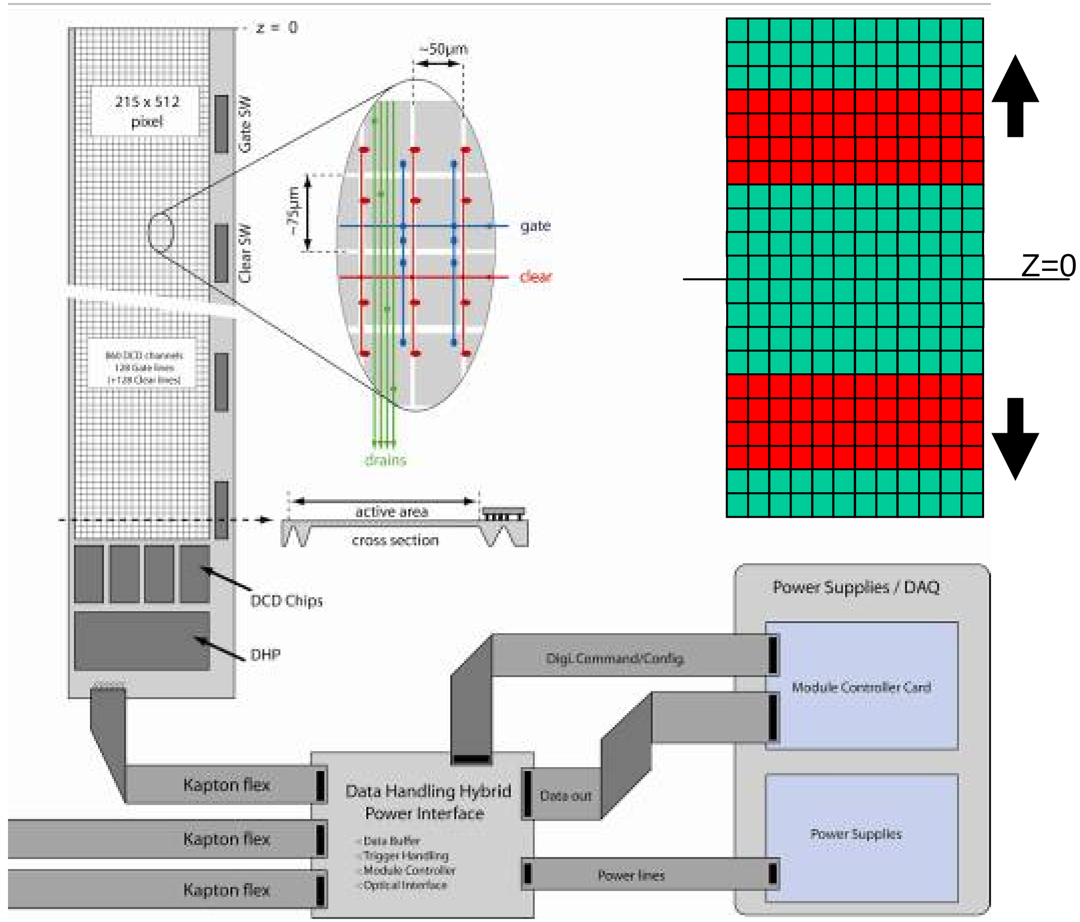
50 x (75-115) μm^2
(or variable in z)

Read out four rows in parallel

256 x 1000 pixels
80 ns readout time
10 μs a frame
(100 kHz)

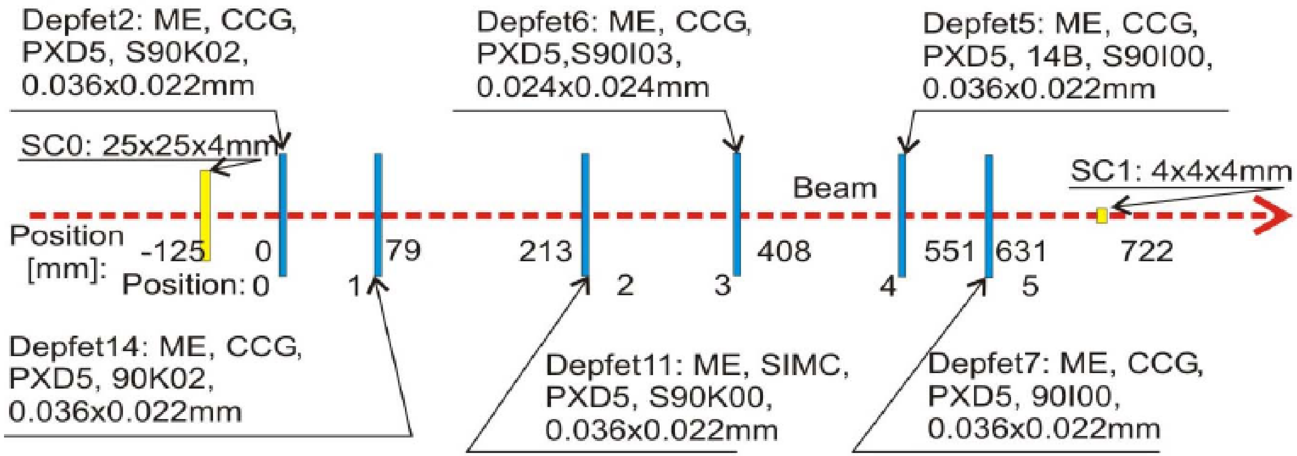
All silicon module
50 μm active area
Thick frame
X_0 ~ 0.15%
(average, including chips)

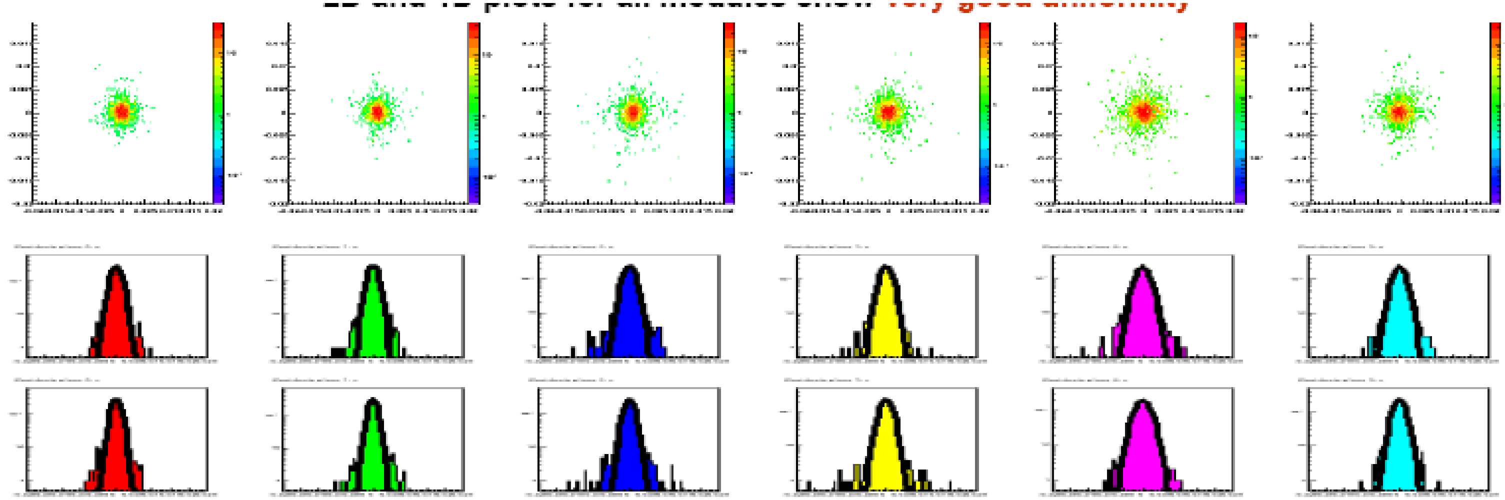


Test Beam

Peter Kodys

2006 – 2008: 7 beam tests at DESY (<6 GeV) and CERN (180 GeV)
Latest setup: 6 DEPFET array acting as telescope & DUT
20 M events taken => analysis in progress





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Radiation Hardness

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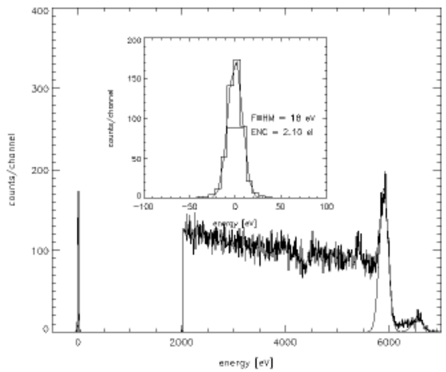
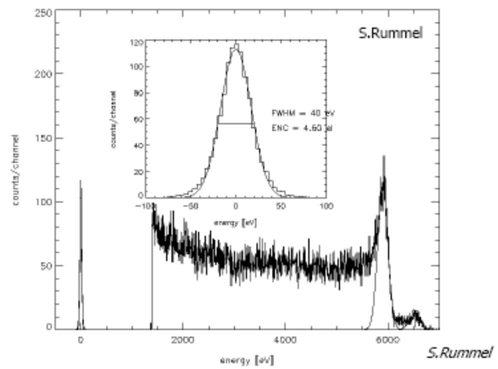
The good news:
DEPFET works after 8MRad with low noise

The bad news:
Large (operation mode dependent) threshold voltage shift & dispersion



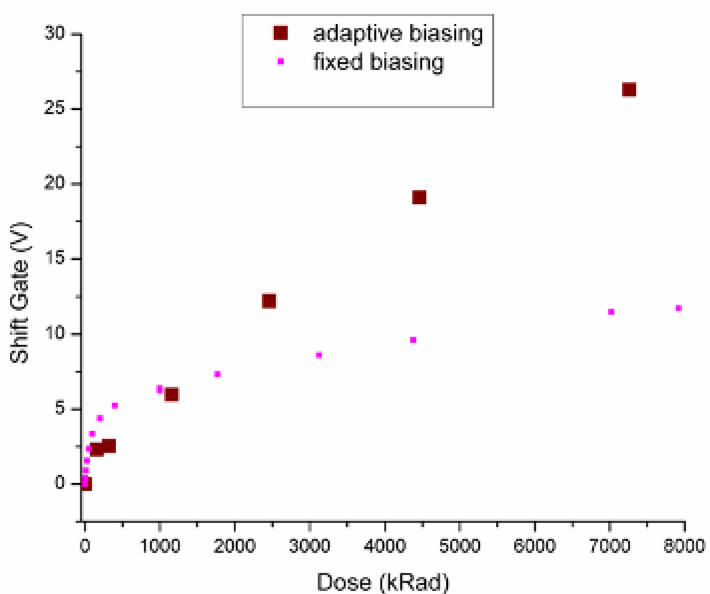


non-irradiated
$V_{thresh} \approx -0.2V$
time cont. shaping $\tau = 10\ \mu s$

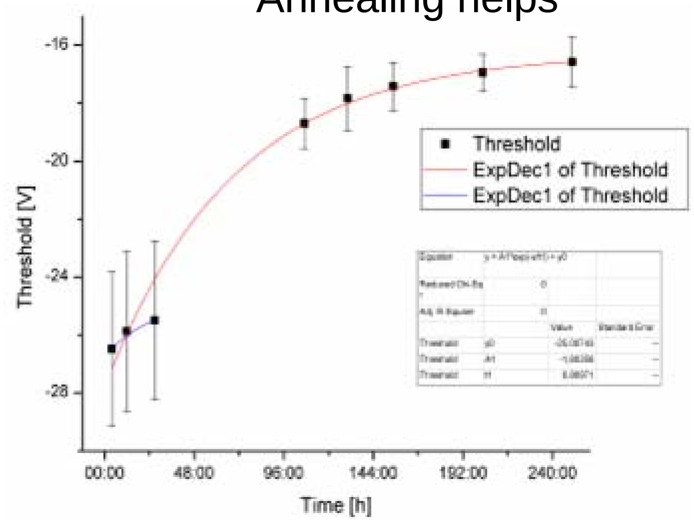
Noise ENC=2.1 e^- (rms)
at T>23 degC

7.9 Mrad, 10keV X-rays
$V_{thresh} \approx -13.0V$,
time cont. shaping $\tau = 10\ \mu s$

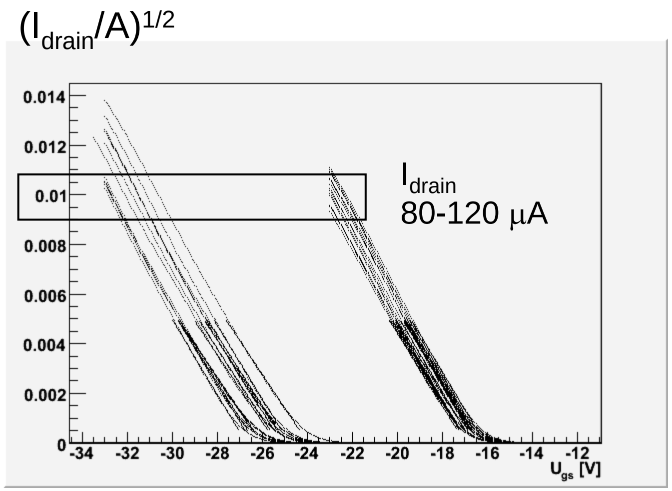
Noise ENC=4.6 e^- (rms)
at T>23 degC

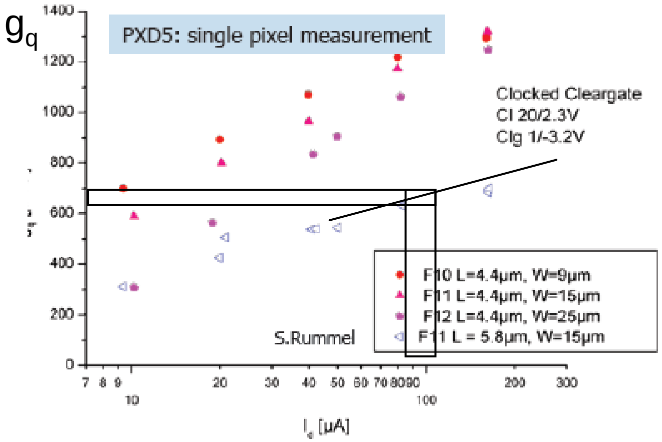


Annealing helps



Consequences

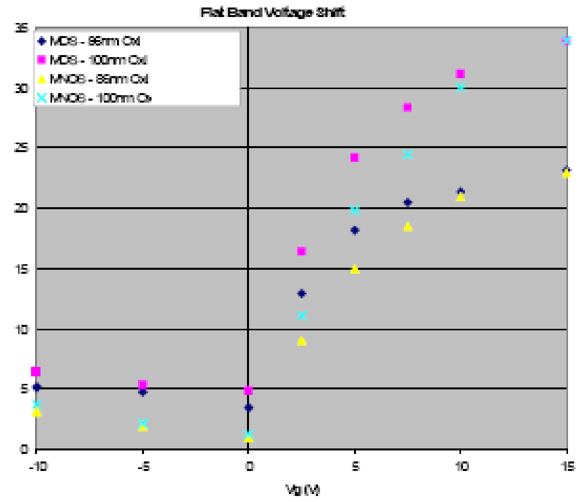




rough estimate: ΔU_{th} -> 10% Δq_g (min-max, rms should be smaller)
Clear performance more critical!

Program:
ASICs deliver large voltage range
Operate (whenever possible) at 0V
Thinner oxides, optimal nitride/oxide

⇒R&D program for optimized gate dielectric parallel to prototype production



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Simulations

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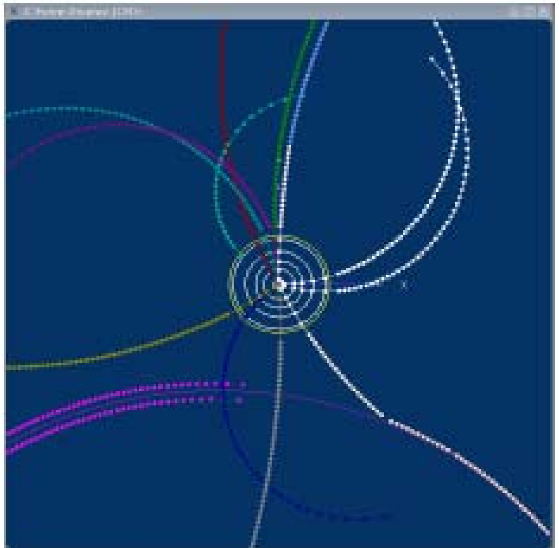
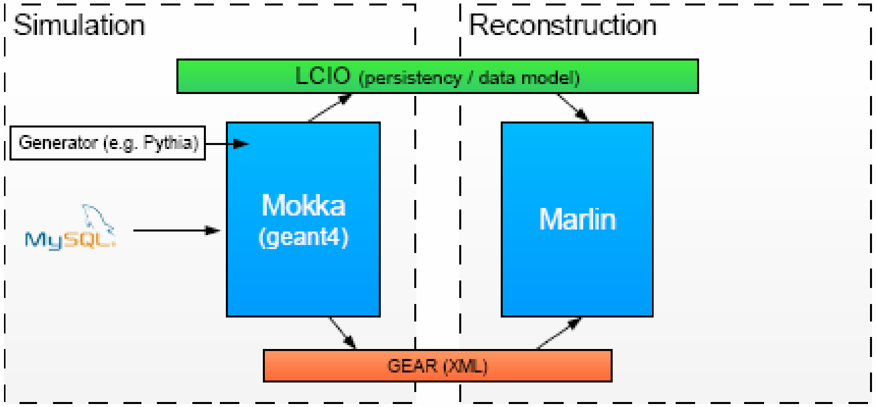
Alexei Raspereza:
Use LDC/LDC software

Implement:
Beam pipe
DEPFET PXS
SVD (no ghosts yet)
CDC
background

PXD: 2 and 3 layer layout
(R_{inner}=1.2cm and 1.7cm)



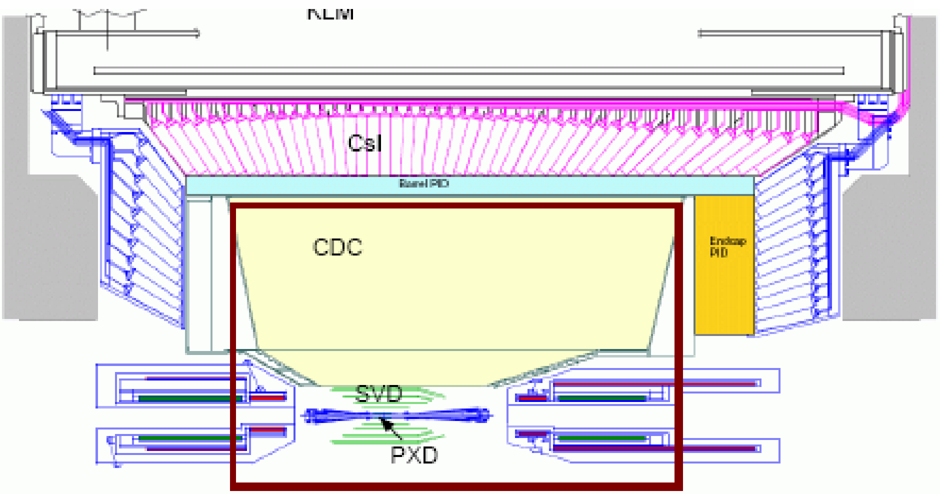


Mokka is geant4 based framework for full detector simulation

LCIO is a persistency framework that defines a common data model

Marlin is modular C++ application framework based on LCIO

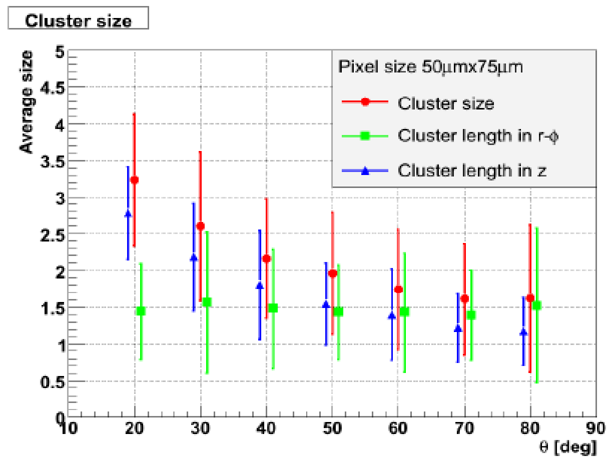
GEAR: one source of geometry. Mokka creates geometry xml files used in Marlin

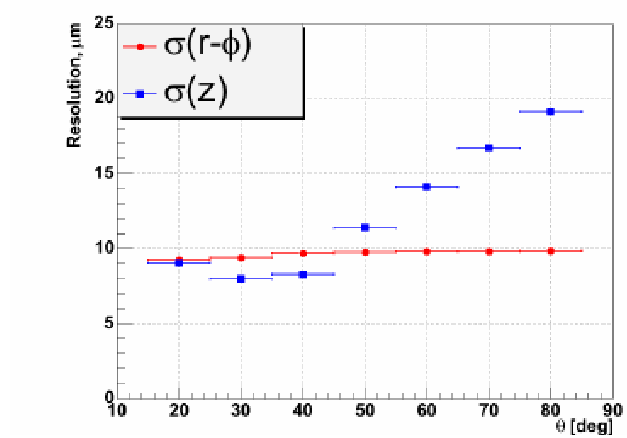


Components implemented in detector simulation
beampipe, PXD, SVD, CDC

DEPFET performance

DEPFET simulation verified/tuned to test beam data





Cluster size in z at low θ can be reduce by variable pitch
Z-resolution at large θ can be improved by variable pitch

two options simulated
2 layer, R_{inner}=1.7cm

3 layer R_{inner}=1.2 cm

Still not final!

	#	r (cm)	sensor (cmxcm)	# sensor in z	#ladders (around phi)	thickness (μm)
1st option	1	1.7	7.1x0.94	2	12	50
	2	2.0	8.4x1.10	2	12	50
2nd option	1	1.2	5.1x0.66	2	12	50
	2	1.7	7.1x0.94	2	12	50
	3	2.0	8.4x1.10	2	12	50

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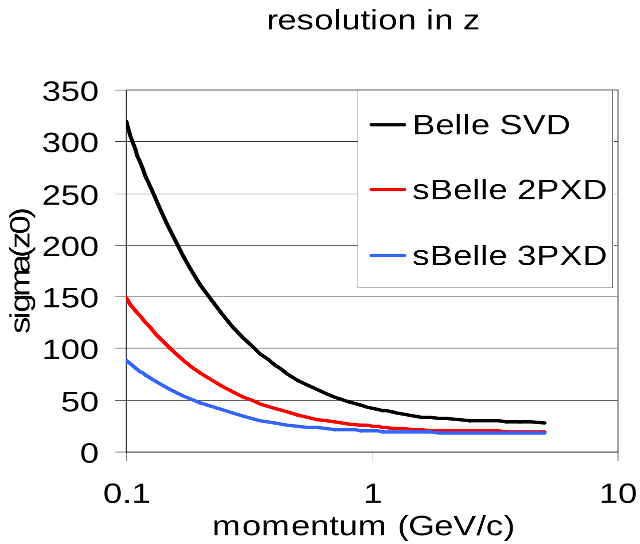
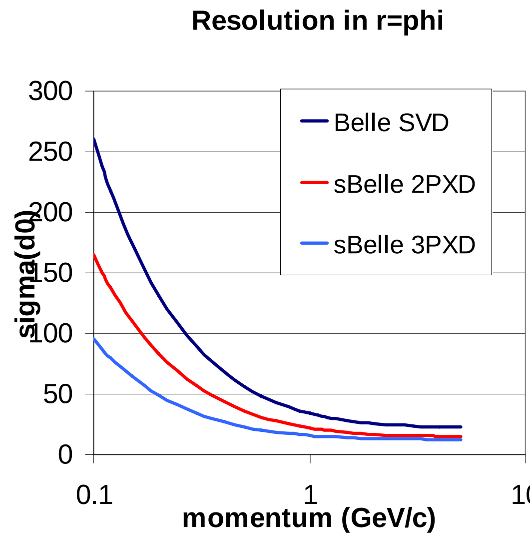
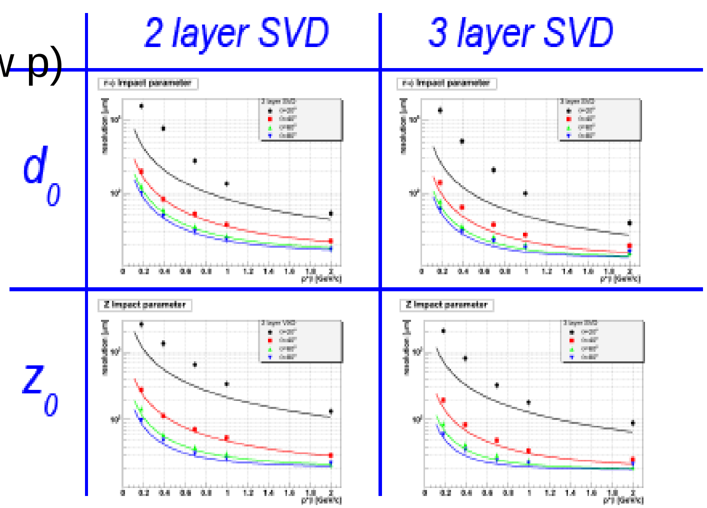
Impact Parameter Resolution





Adding Background:
Resolution at low θ degrades
(however: software not yet tuned to low p)

Impact Parameter Resolution in Presence of Backgrounds



Occupancies: (initial lumi)

R	Occup.
1.2	1.6%
1.7	0.8%
2.0	0.6%

DEPFET Collaboration

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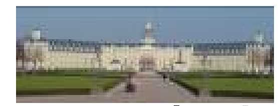
List of Institutions contributing to DEPFET @ SuperBelle

			Contact
Germany			
	MPI	Max-Planck-Institute for Physics, Munich	C. Kiesling, H.-G. Moser
	BON	University of Bonn	N. Wermes
	GIE	University of Giessen	S. Lange
	GOE	University of Göttingen	A. Frey
	HEI	University of Heidelberg	P. Fischer
	KAR	University of Karlsruhe	T. Müller
Austria			
	VIE	Institute for High Energy Physics (HEPHY), Vienna	M. Friedl
Czech Rep.			
	PRA	Charles-University Prague	P. Kodys
Poland			
	KRA	Institute of Nuclear Physics, Krakow	H. Palka
Spain			
	IFV	Instituto de Fisica Corpuscular (IFIC), Valencia	C. Lacasta
	URL	University Ramon Llull, Barcelona	J. Riera Babures
	UBA	University of Barcelona	L. Garrido
	CNM	Centro Nacional de Microelectronica, Barcelona	E. Cabruja
	IFB	Instituto de Fisica d'Altes Energies (IFAE), Barcelona	M. Chmeissani
	USC	University of Santiago de Compostela	P. Vazquez Regueiro
	IFC	Instituto de Fiisica de Cantabria (IFCA), Santander	I. Vila
USA			
	HAW	University of Hawaii	G. Varner
Japan	KEK	KEK	T. Tsuboyama

C. Kiesling, 1st Open Meeting of the SuperKEKB Collaboration, KEK, Dec. 10-12, 2008

HEPHY



IEKP Karlsruhe

Workpackages/Organization

1.1	**Parameter Definition**	MPP/HLL	KRA, PRA
1.2	**DEPFET Sensor**	MPP/HLL	
1.3	**ASIC**		
1.3.1	Switcher	HD	
1.3.2	DCD	HD	
1.3.3	DHP	BN	MPP/HLL, UBA, USC, URL
1.3.4	Data Link	BN	MPP/HLL, UBA, USC, URL
1.4	**Module Design**		
1.4.1	Sensor Ladder (& Interconnection)	MPP/HLL	HD, BN, IFV, CNM, IFB
1.4.2	Kapton Flex	KEK	VIE, BN
1.4.3	DHH (Data Handling Hybrid)		
1.5	**Mechanical Design**	MPI	KA, VIE, KRA, IFV, IFB
1.6	**Thermal Simulation**	KA	MPP, VIE, KRA, IVF, IFB
1.7	**System**		
1.7.1	DAQ	GOE	KRA, GIE, MPP, KEK, URL, HAW
1.7.2	Power & Slow Control	KRA	KEK, USC
1.7.3	Cooling plant	KEK	

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Schedule

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- Two DEPFET runs for SuperBelle

<u>First run PXD6: 2009</u>

-: first DEPFET run on SOI wafers!!

-: 6 SOI and 2 std. Hi-Res Wafer

-: top wafer (front side) technology like PXD5

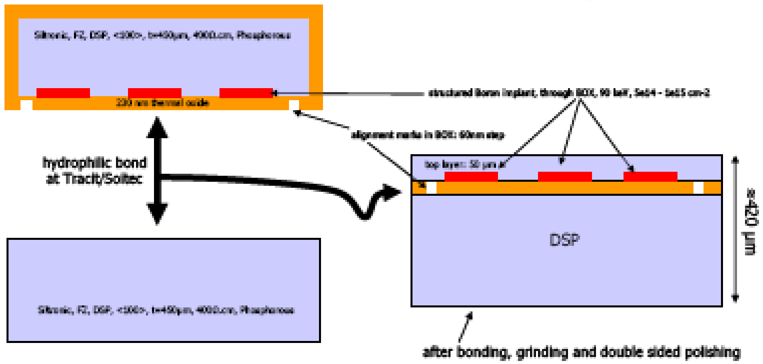
-: new technology: thinning and BS process

-: Aim: - find optimal design

- test yield and optimize technology

- provide devices for all-silicon module

End Spring 2010

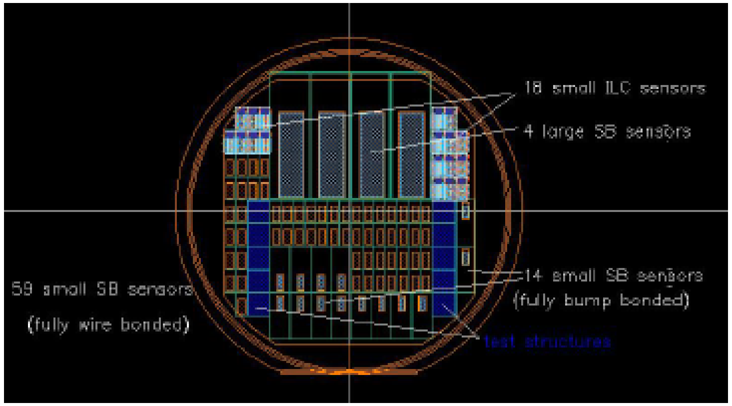


<u>SuperBelle Production PXD7: Start 2011</u>

-: With improved technology

-: 20 Wafer? (depends on yield of PXD6)

End Spring 2012



preliminary wafer floor plan for PXD6

Schedule

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Prototype Sensor

Final Sensor

ASICs

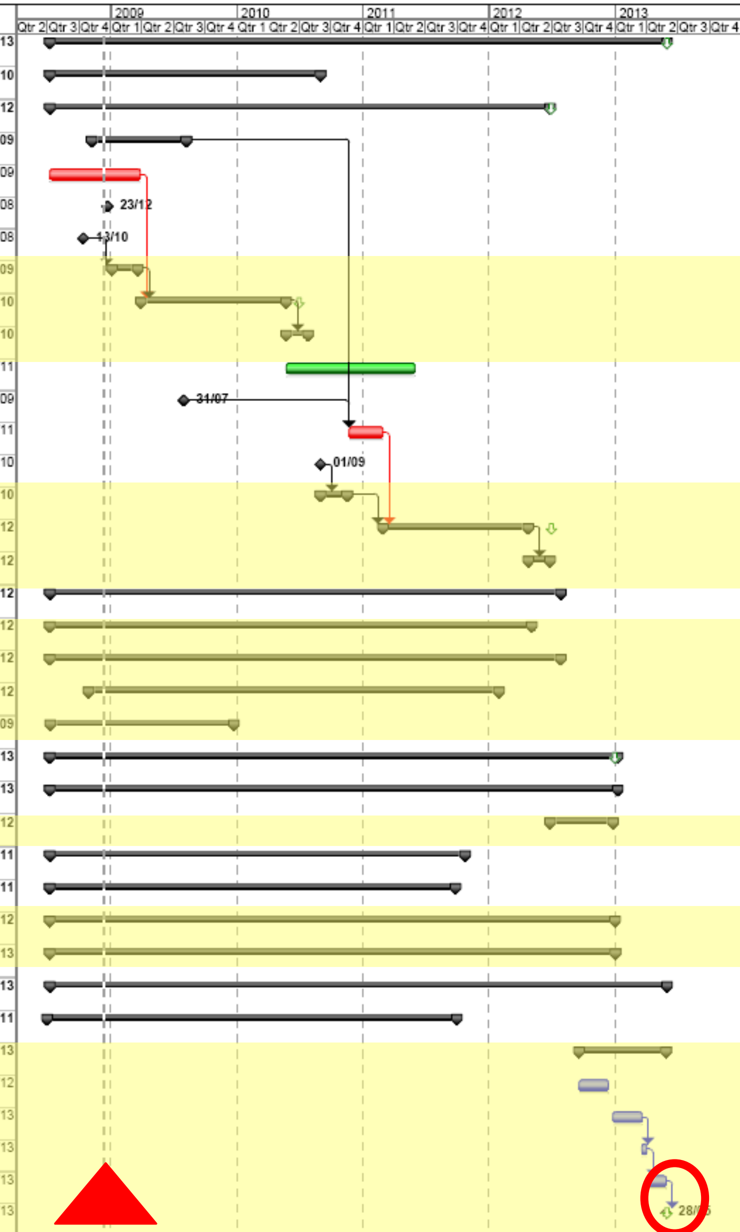
Module Production

Mechanics, Cooling

Installation at KEK

Ready: May 2013

ID	Task Name	Duration	Start	Finish
1	1.0 DEPFET Detector	1278 days?	Wed 09/07/08	Fri 31/05/13
2	1.1 Parameter Definitions	560 days?	Wed 09/07/08	Tue 31/08/10
4	1.2 Pixel Sensor	1035 days?	Wed 09/07/08	Tue 26/06/12
5	R&D on thin oxides	196 days?	Fri 07/11/08	Fri 07/08/09
12	PXD6 Design	188 days?	Wed 09/07/08	Fri 27/03/09
13	Layout Deadline (Chip	0 days	Tue 23/12/08	Tue 23/12/08
14	Wafer Delivery	0 days	Mon 13/10/08	Mon 13/10/08
15	SOI preparation	55 days	Mon 05/01/09	Fri 20/03/09
20	PXD6 production	301 days?	Mon 30/03/09	Mon 24/05/10
24	thinning	45 days	Tue 25/05/10	Mon 26/07/10
30	PXD6 evaluation	266 days?	Tue 25/05/10	Tue 31/05/11
31	fix final module dimens	0 days	Fri 31/07/09	Fri 31/07/09
32	PXD7 Design	70 days?	Tue 23/11/10	Tue 01/03/11
33	wafer delivery	0 days	Wed 01/09/10	Wed 01/09/10
34	SOI preparation	55 days	Wed 01/09/10	Tue 16/11/10
39	PXD7 production	301 days?	Tue 01/03/11	Tue 24/04/12
43	thinning	45 days	Wed 25/04/12	Tue 26/06/12
49	1.3 ASIC	1058 days?	Wed 09/07/08	Fri 27/07/12
50	1.3.1 DCD	998 days?	Wed 09/07/08	Fri 04/05/12
60	1.3.2 Switcher	1058 days?	Wed 09/07/08	Fri 27/07/12
72	1.3.3 DHP	849 days?	Wed 29/10/08	Mon 30/01/12
92	1.3.4 Data Link	380 days?	Thu 10/07/08	Wed 23/12/09
94	1.4 Module	1175 days?	Wed 09/07/08	Tue 08/01/13
95	1.4.1 Sensor ladder	1175 days?	Wed 09/07/08	Tue 08/01/13
105	Module Production	130 days	Wed 27/06/12	Tue 25/12/12
132	1.4.2 Kapton link	859 days?	Wed 09/07/08	Mon 24/10/11
137	1.4.3.DHH	839 days?	Wed 09/07/08	Mon 26/09/11
141	1.5 Mechanical Design	1169 days?	Wed 09/07/08	Mon 31/12/12
145	1.6 Thermal Issues	1170 days?	Wed 09/07/08	Tue 01/01/13
149	1.7 System	1278 days?	Wed 09/07/08	Fri 31/05/13
158	2.0 Test Systems	849 days?	Tue 01/07/08	Fri 30/09/11
167	Intergration/Installation	180 days	Wed 19/09/12	Tue 28/05/13
168	Installation of 1st layer	3 mons	Wed 19/09/12	Tue 11/12/12
169	Installation of 2nd layer	3 mons	Wed 26/12/12	Tue 19/03/13
170	service connection	2 wks	Wed 20/03/13	Tue 02/04/13
171	tests & debug	2 mons	Wed 03/04/13	Tue 28/05/13
172	System ready at KEK	0 days	Tue 28/05/13	Tue 28/05/13



Open Questions

Radiation
- => improve on threshold voltage shift
- => dose, spectra, uniformity
- => optimal shielding
- => NIEL damage (particle type, spectra)

Need to know beam pipe radius (outer!)
- => the smaller the better (for resolution)!
- => fix at latest mid 2010 (final sensor geometry)

Need to know clearances and envelops at and around IP
- => mechanics, cooling, routing
- => temperature of the beam pipe

Engineering of mechanics/interface to SVD
- => PXD should be mounted parallel to beam pipe
- => same mechanical structure as SVD?
- => common services (cooling)?

DAQ interface (PXD may deliver up to 70 Gbit/s)

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Conclusions

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CAPs, SOI:

very promising concepts
status: basic R&D
important upgrade path for highest luminosity!

DEPFET:

evolving from basic R&D towards production
Sensors: one more prototype production in 2009
(convert from ILC to SuperBelle layout)
final production in 2011
radiation hardness should be improved

Electronics: prototypes under test (control, readout)
digital readout chip in work
System: work started
Schedule: install in 2013
upgrade after ~5 years
(radiation damage, occupancy,
smaller beam pipe?)

We propose DEPFET as baseline PXD for superBelle
to be discussed in closed session