Front-end readout study for SuperKEKB

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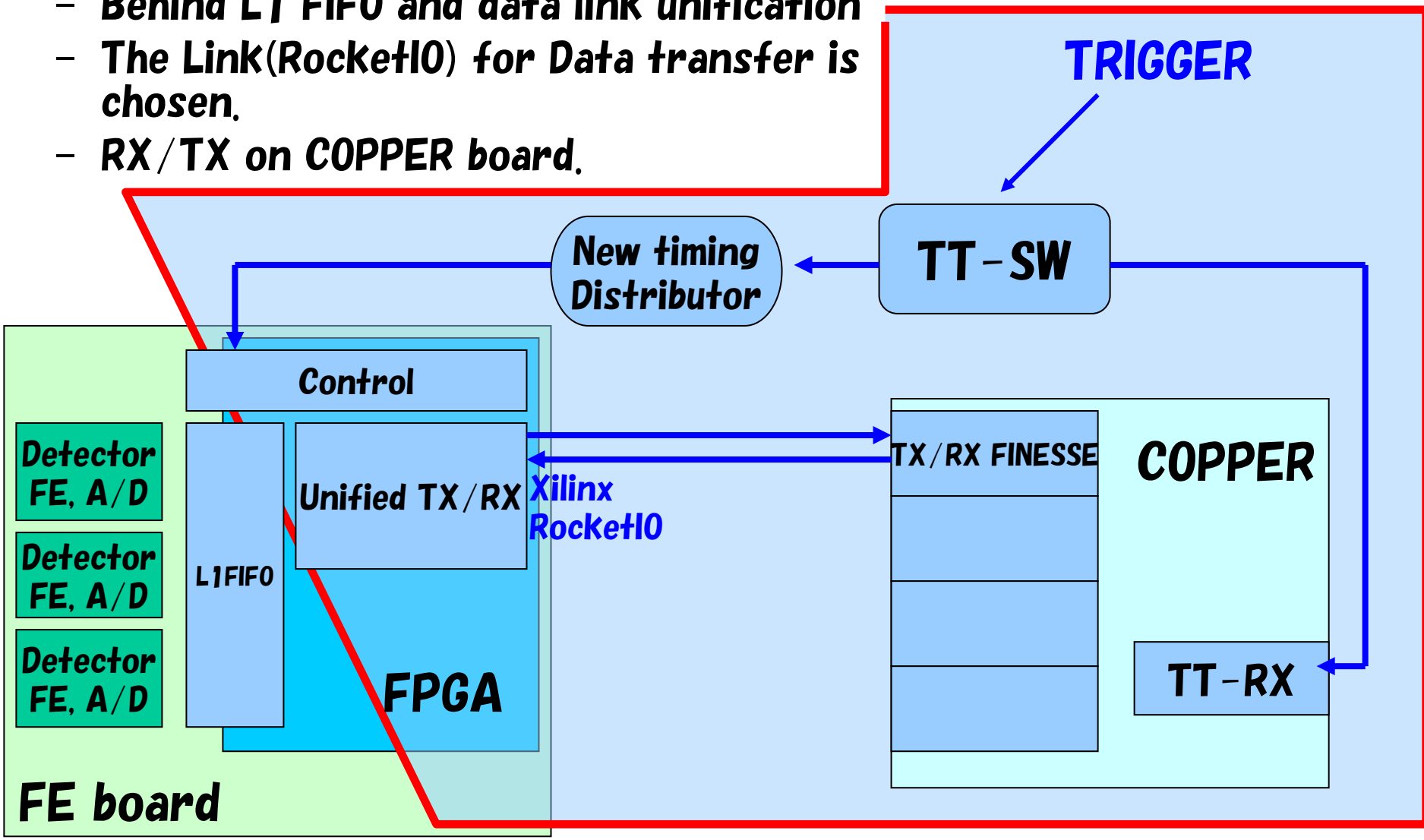
Requirements of Front-end from DAQ

- Trigger decision time (3μsec ~ 6μsec)
  - Buffer size of L1 Trigger : 6 μsec
- Rapid trigger communication
  - Trigger/Busy handshake
  - Event Tag.(ID?) receiving
- Dead-time must be less than a few μsec
- Data transport to DAQ system
- (Trigger pattern information transport to GDL)

Unification idea by DAQ group

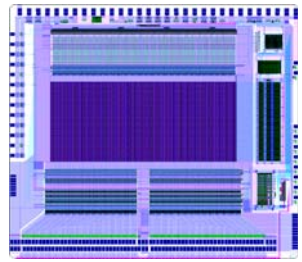
- **Unification point**
  - Behind L1 FIFO and data link unification
  - The Link(RocketIO) for Data transfer is chosen.
  - RX/TX on COPPER board.



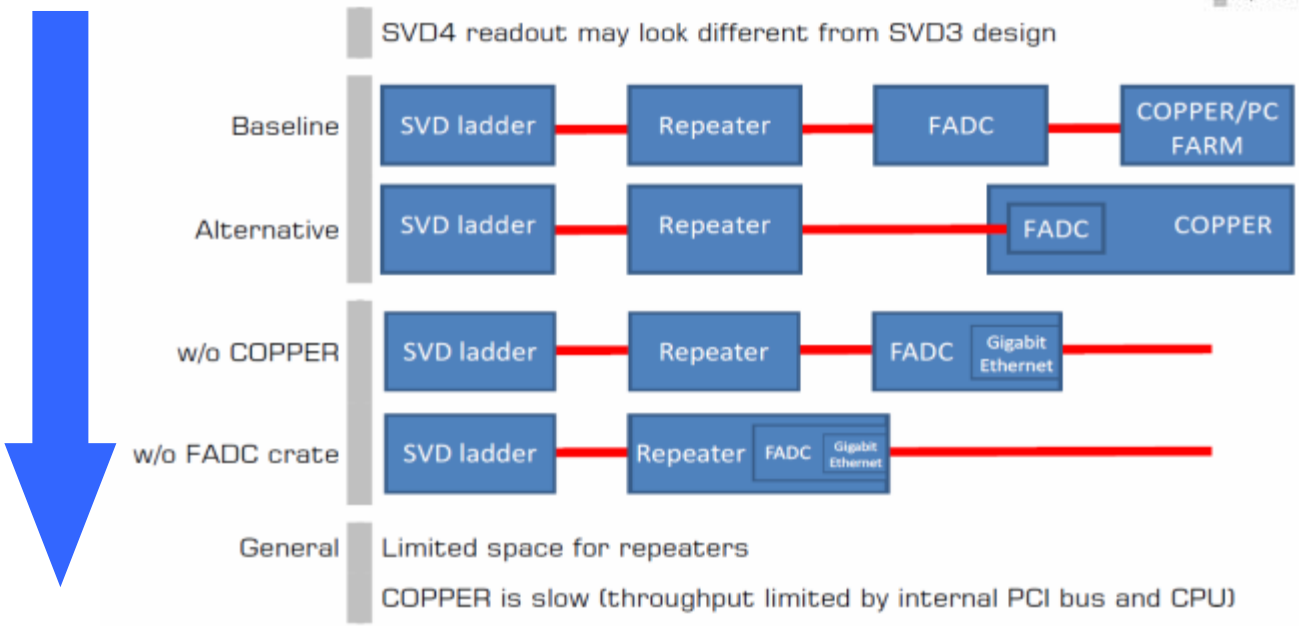
Detectors and readout methods

	Read-out device plan	location
SVD	APV-25 + Repeater + VME FADC	Near detector + electronics hut
CDC	ASB/TDC/FADC or High speed FADC	Near detector
PID ARICH	ASIC (SA,...)	Near detector
PID TOP	(high precision time measurement : σ~10ps)	-
ECL	Waveform Digitizer	Side of detector + ?
KLM	Disc.+FPGA	Near detector
PXL	Application of PANDA readout board	

SVD front-end

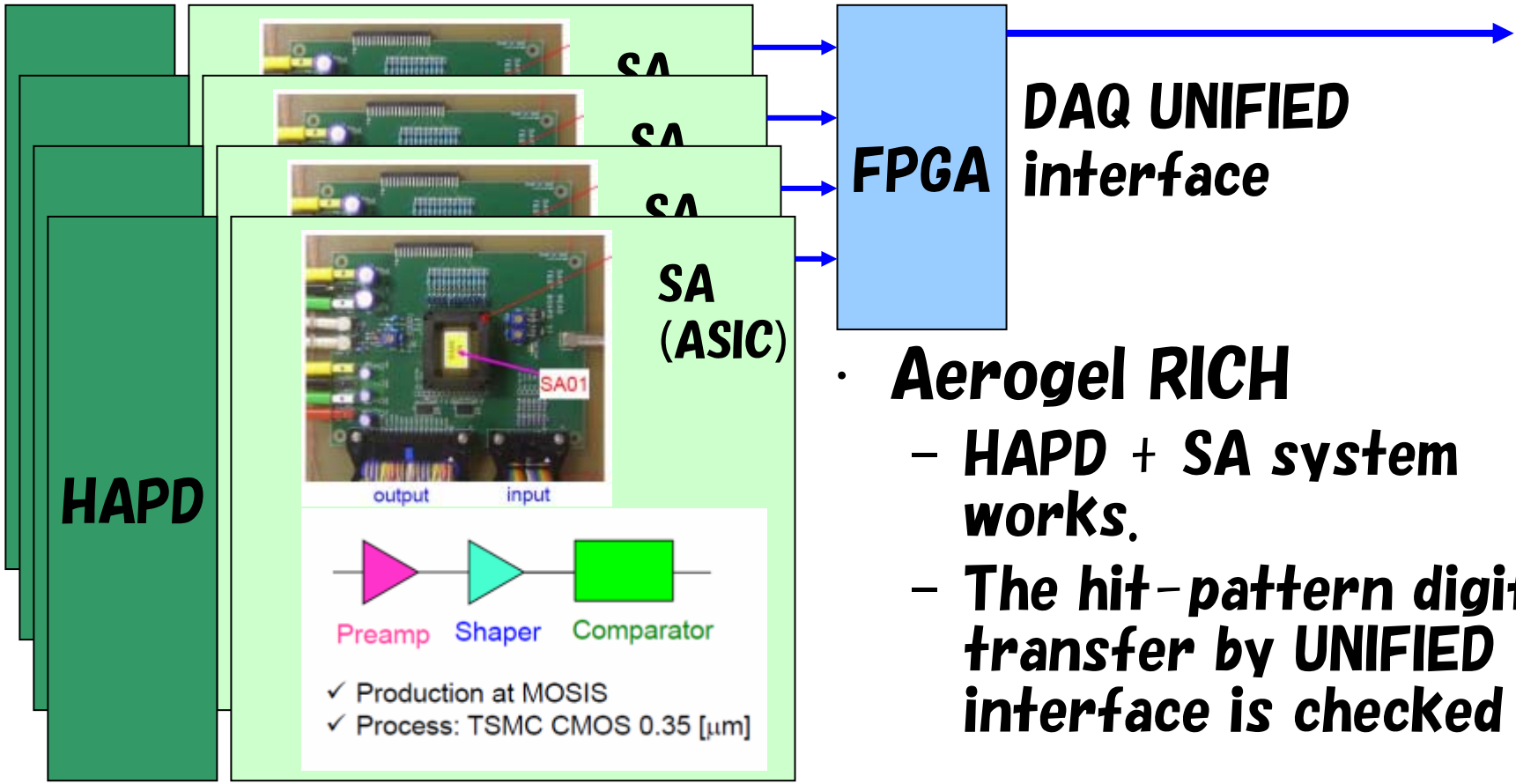


- APV-25 readout baseline design works already.
- SVD group will progress to w/o FADC crate design to reduce module space and power consumption.



← Now

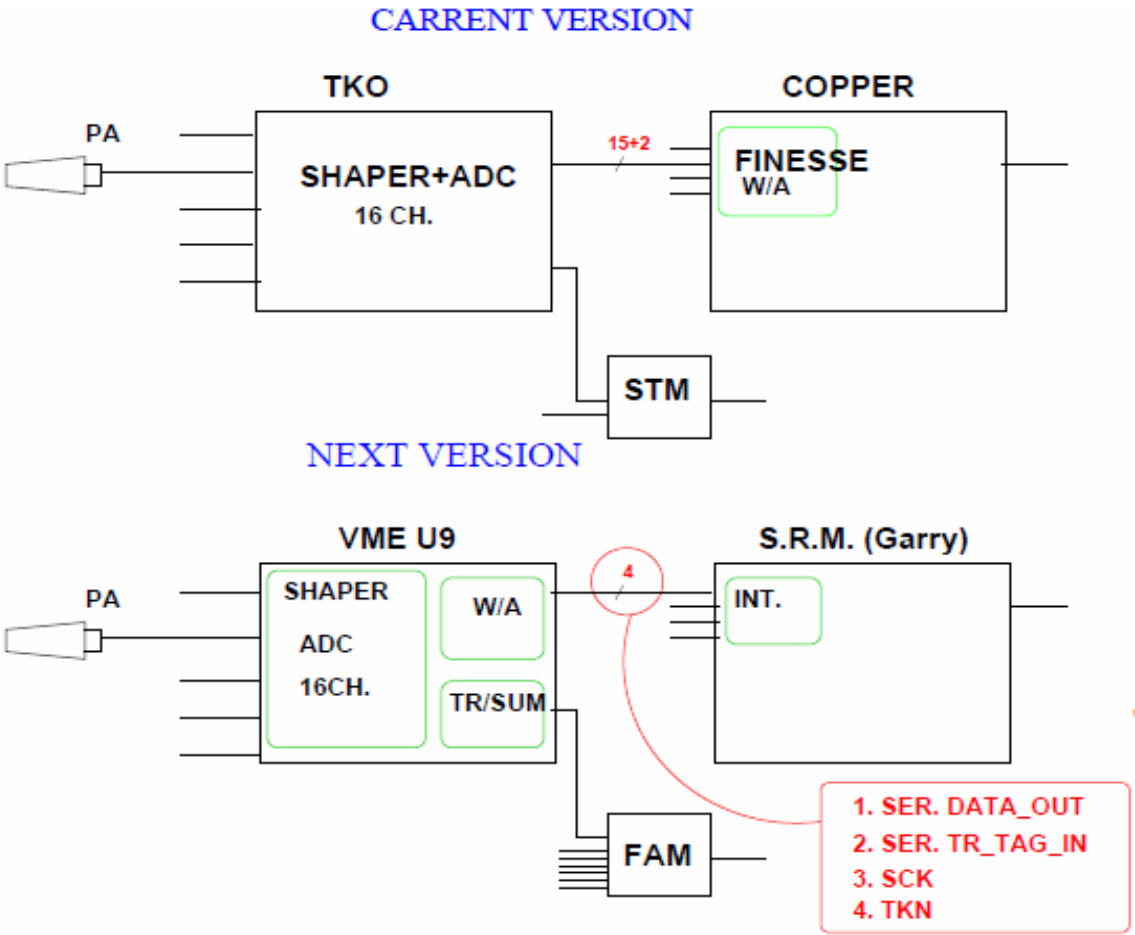
PID front-end



- Aerogel RICH
  - HAPD + SA system works.
  - The hit-pattern digital transfer by UNIFIED interface is checked up.
- TOP ?

ECL front-end

- COPPER based Waveform digitizer was tested.
- VME U9 Shaper ADC Waveform Analyzer is planed.



KLM front-end

- RPC :
  - time-multiplex→ COPPER TDC system works.
  - The hit-pattern digital transfer by UNIFIED interface is checked up.
- New Scintillator :
  - The hit-pattern digital transfer by UNIFIED interface ?

G.S.Varner's Proposal

- **Waveform sampling for all detectors**
- **TARGET :**
  - **1GHz, 9bit digitizer**
- **BLAB2 :**
  - **10GHz digitizer which can be used high-resolution time measurements**

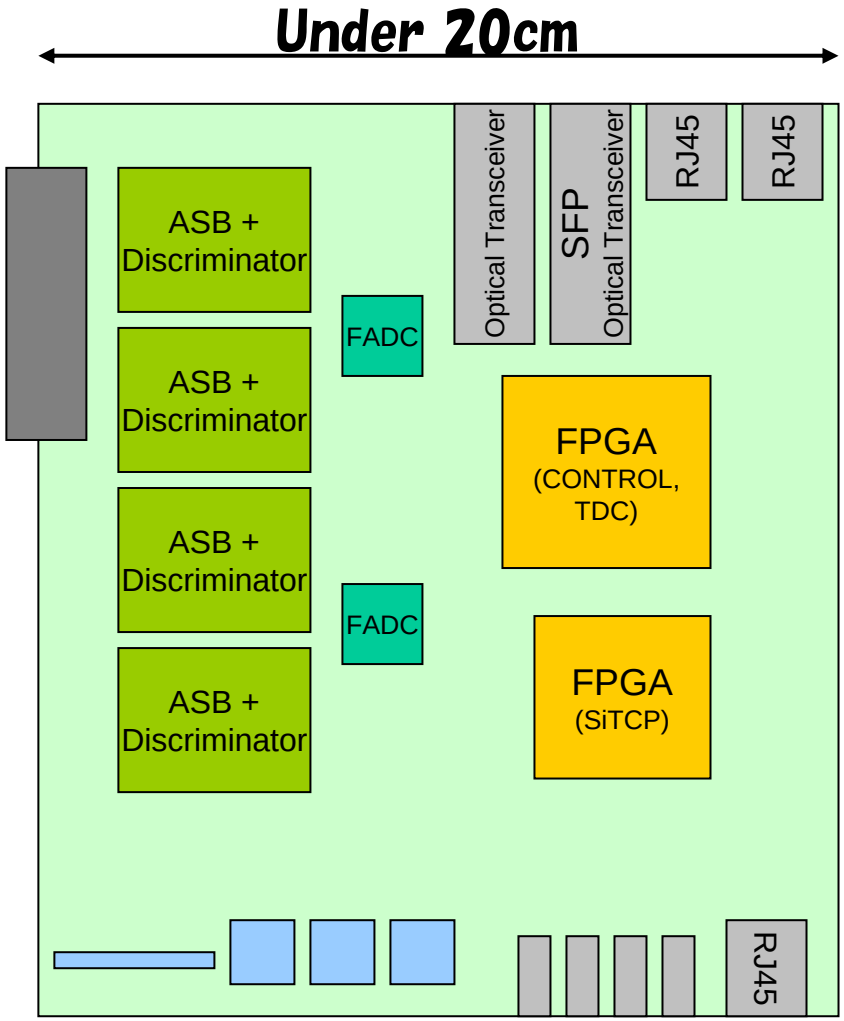
Subdetector	ASIC	ref. ASIC	Location	FPGA link
SVD3	APV25		E-hut	no
new SVD	BSR/KUPID	APV25	hybrid/dock	yes
CDC	BCA	TARGET	in detector	yes
PID SiPMT	BCA	TARGET	in detector	yes
PID HP-PMT	HPBA	BLAB2	in detector	yes
ECL	N/A		on detector	yes
Scint. KLM	BCA	TARGET	in detector	yes
VFV	BCA	TARGET	in detector	yes

CDC Readout study with DAQ UNIFIED interface

- CDC FE prototype card
  - A study about CDAQ/Front-end data transport.
  - A study about GDL/Front-end data transport
  - A study of the CDC readout scheme
    - Charge measurements by (slow) FADC
    - Drift time measurements by FPGA based TDC
  - A study of common mode noise from the front-end readout board to CDC
  - A confirmation of front-end specification

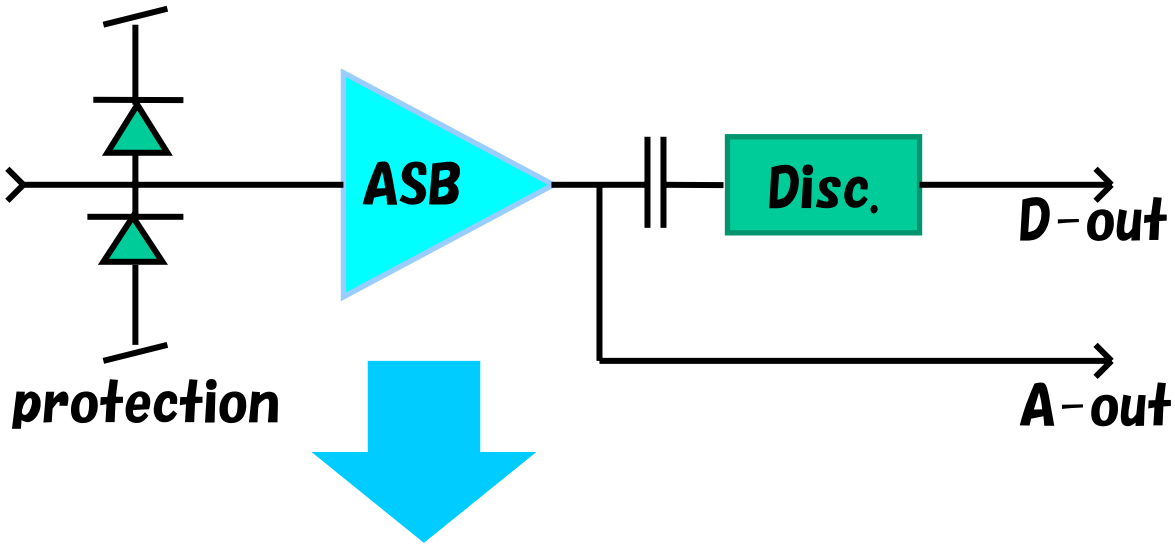
- G.V.'s proposal FE will be tested in parallel.

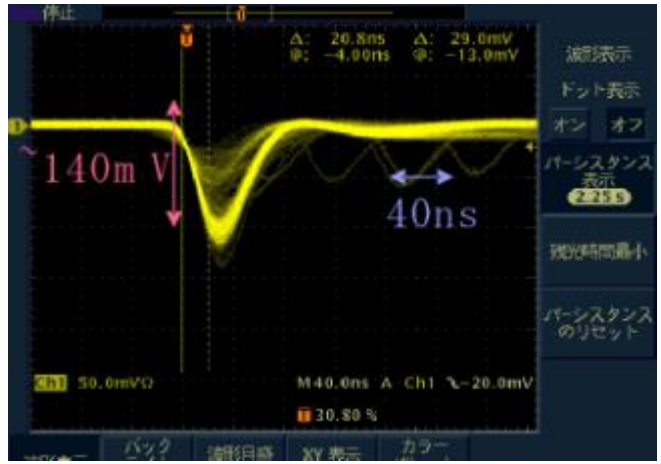
CDC FE Prototype card



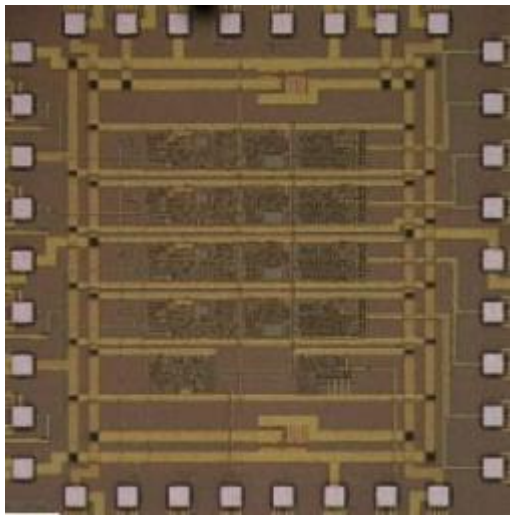
- 16ch/board
- BJT-ASB/Discriminator
- FADC: over 20MHz / 10bit
- FPGA : Vertex-5 LXT
  - TDC: 1 nsec counting
  - FADC reading
  - Control
- FPGA: Spertan3A
  - SiTCP for CDC study
- Connectors
  - RJ-45 for SiTCP
  - RJ-45 for DAQ timing signals
  - RJ-45 for DAQ data line
  - SFP for DAQ data line
  - Optical TX/RX for GDL
  - LEMO input x 3, output x1
- Shielded substrate

Front-end (for system test)





Fe source

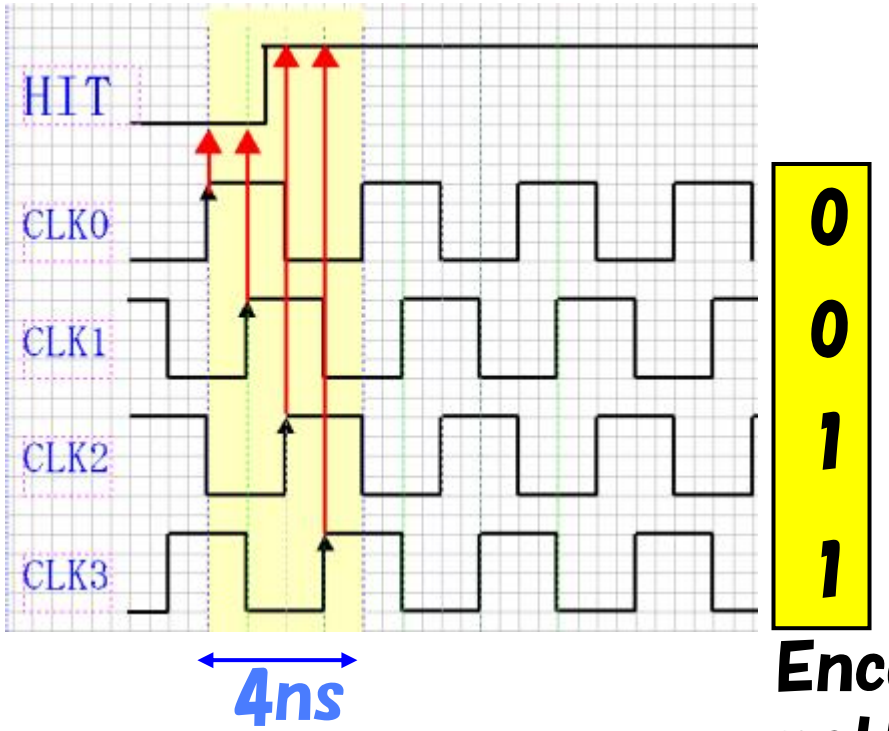


- ASB
  - Amp. Shaper Buffer
  - 4ch/chip
  - Peaking time ~40nsec
  - Gain :
    - -360mV/pC ~ -1400mV/pC
    - (4 step variable)

TDC in FPGA

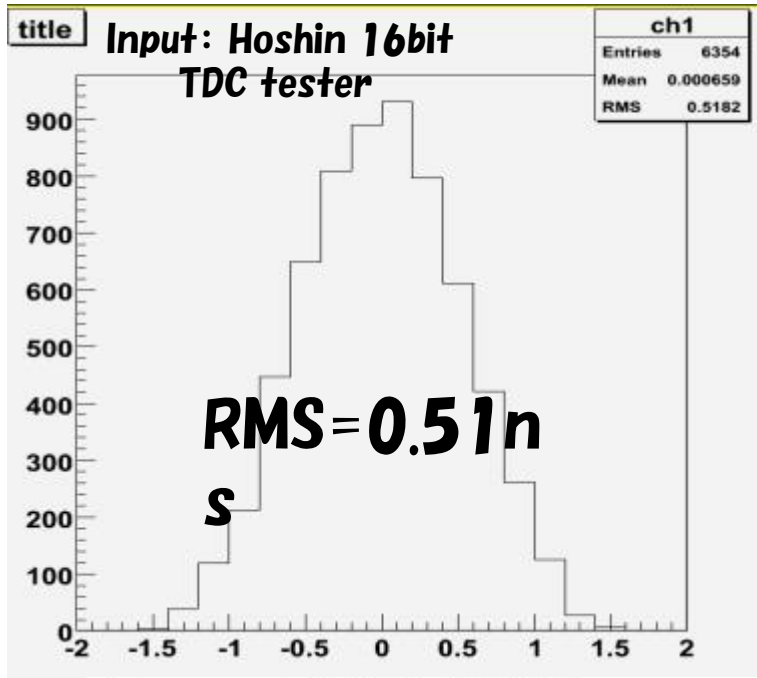
- To use 4 different phase 250MHz Clock in the aim of 1 nsec counting

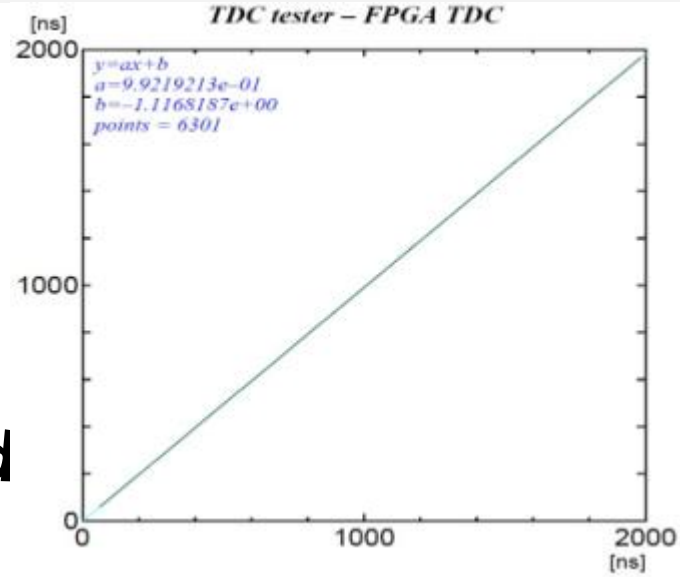
Latch each clock timings



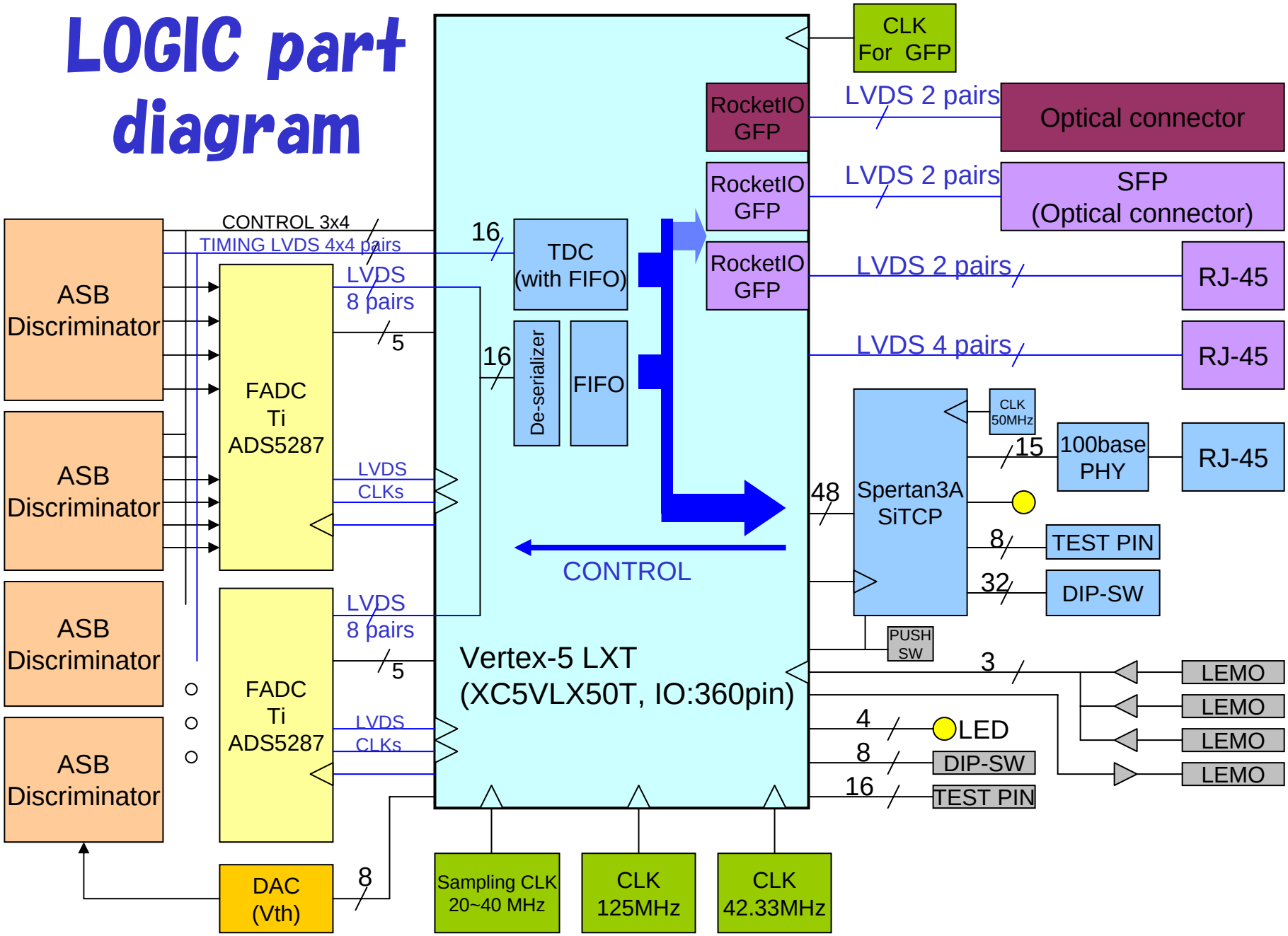
0
0
1
1

Encode latched pattern





LOGIC part diagram



Scheduled plan

2008/11	Study preliminary specification
2008/11,12	design circuit schematics -ASD part (T.Taniguchi-san) -Digital part (M.Saito-san)
2008/12 end	order printed circuit board design
2009/2	Final check of the PC board design and start production -M.Ikeno-san etc…
2009/3	Start the practical study

Summary

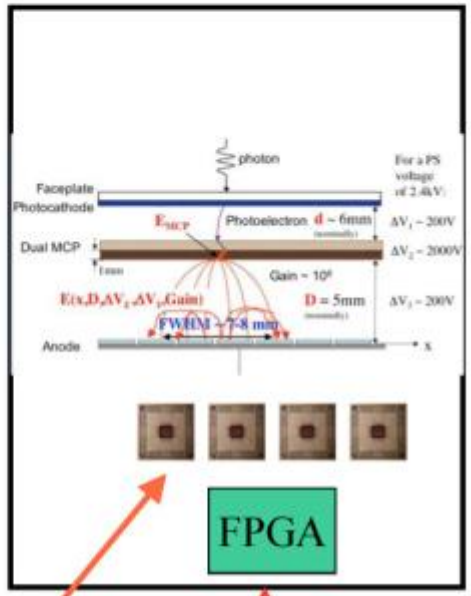
- Each detector groups are progressing to design the detector Front-end.
- G.V. offer good two high speed waveform samplers to unified FE.
  - The unification by the waveform sampler should be discussed.
  - Those prototype is available.
- UNIFIED interface R&D has been started in collaboration with CDC group.

- Issues
  - Treatments about over 20 MB/sec/link speed data flow
    - COPPER can treat up to 40MB/sec data flow w/o network.
    - Will detector groups request more faster single link data flow ?
  - Discussion with the groups which thinking COPPER-less option.

Backups

TARGET (TeV gamma) Proto System Specifications

4096	samples/channel (2us trig latency)
16	channels/TARGET ASIC
4	TARGET ASIC
~9	bits resolution
32	samples in window (~32ns)
~1	GSa/s (up to 2.5GSa/s)
2k	word (9 bits) Event size
16	us to read all samples
50	kHz sustained readout



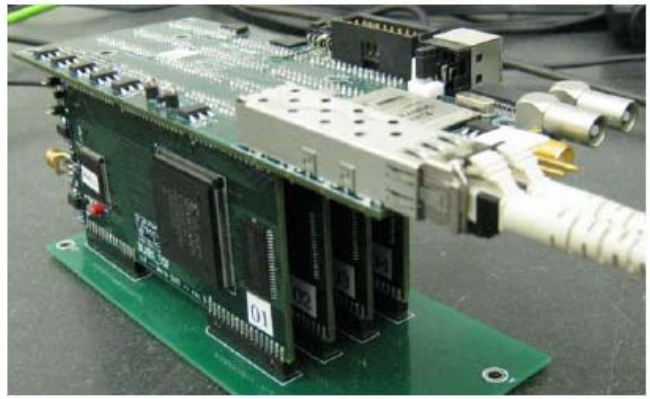
- Any group of 16 packing possible
- Readout link
  - Initially USB2 [>50kHz Event sustained (20Mbit/s)?]
  - Fiber links to cPCI as upgrade [make TARGET RO limit] and use to collect trigger information

Highly Integrated Readout

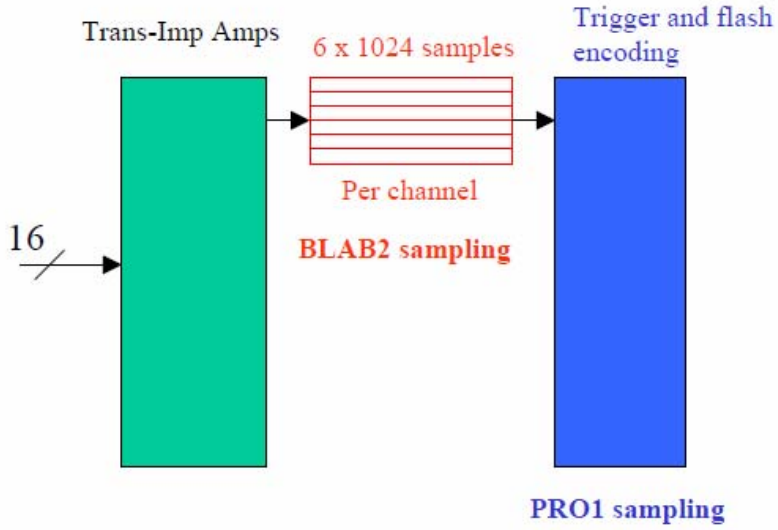
- **Buffered LABRADOR**

TABLE II: *BLAB2 ASIC Specifications.*

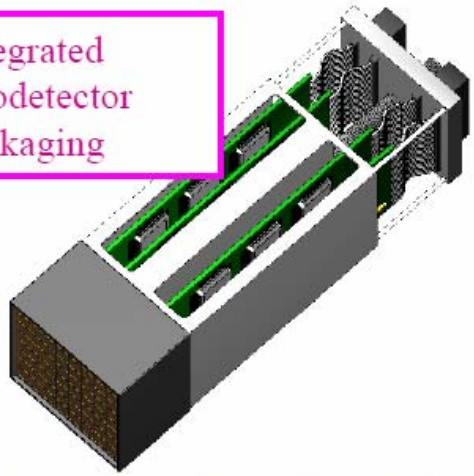
Item	*Value*
Photodetector Input Channels	16
Linear sampling arrays/channel	~~2~~ 6
Storage cells/linear array	~~512~~ 1024
Sampling speed (Giga-samples/s)	2.0 - 10.0
Outputs (Wilkinson)	32



BLAB2 ASIC



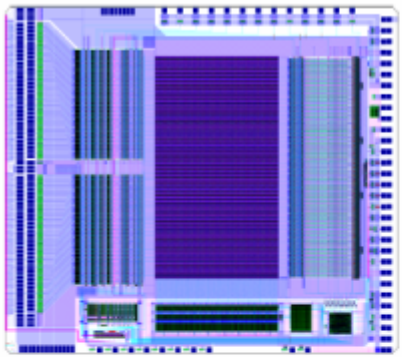
Integrated Photodetector packaging

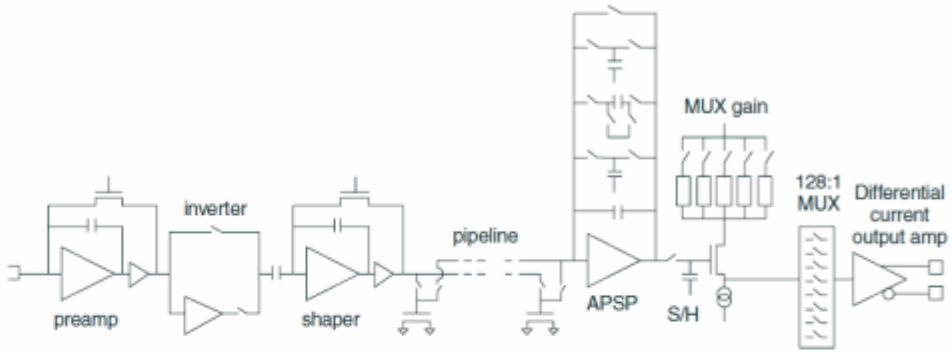


BLAB2 submit 6/23, ASICs received last Monday

SVD front-end

APV25 Front-End Chip



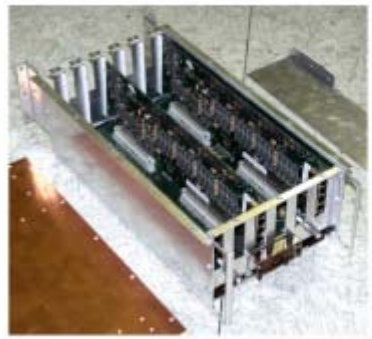


APV25 — Developed for CMS Tracker

Features

- 50ns (default) peaking time (cf. 800ns of current VA1TA) → significant occupancy reduction
- 40MHz (default) clock, 192-cell pipeline → no dead-time
- Noise: 250 e + 36 e/pF (peak mode) – drawback of fast shaping
- Multi-peak mode allows to several samples along shaping cur
  additional occupancy reduction possible through peak time de

SVD3 Readout – Repeater and Back-End



Repeater Box ("DOCK")

9U VME readout crate