SuperKEKB Meeting
December 11, 2008

Electronics for endcaps KLM

D. Liventsev (ITEP, Moscow)

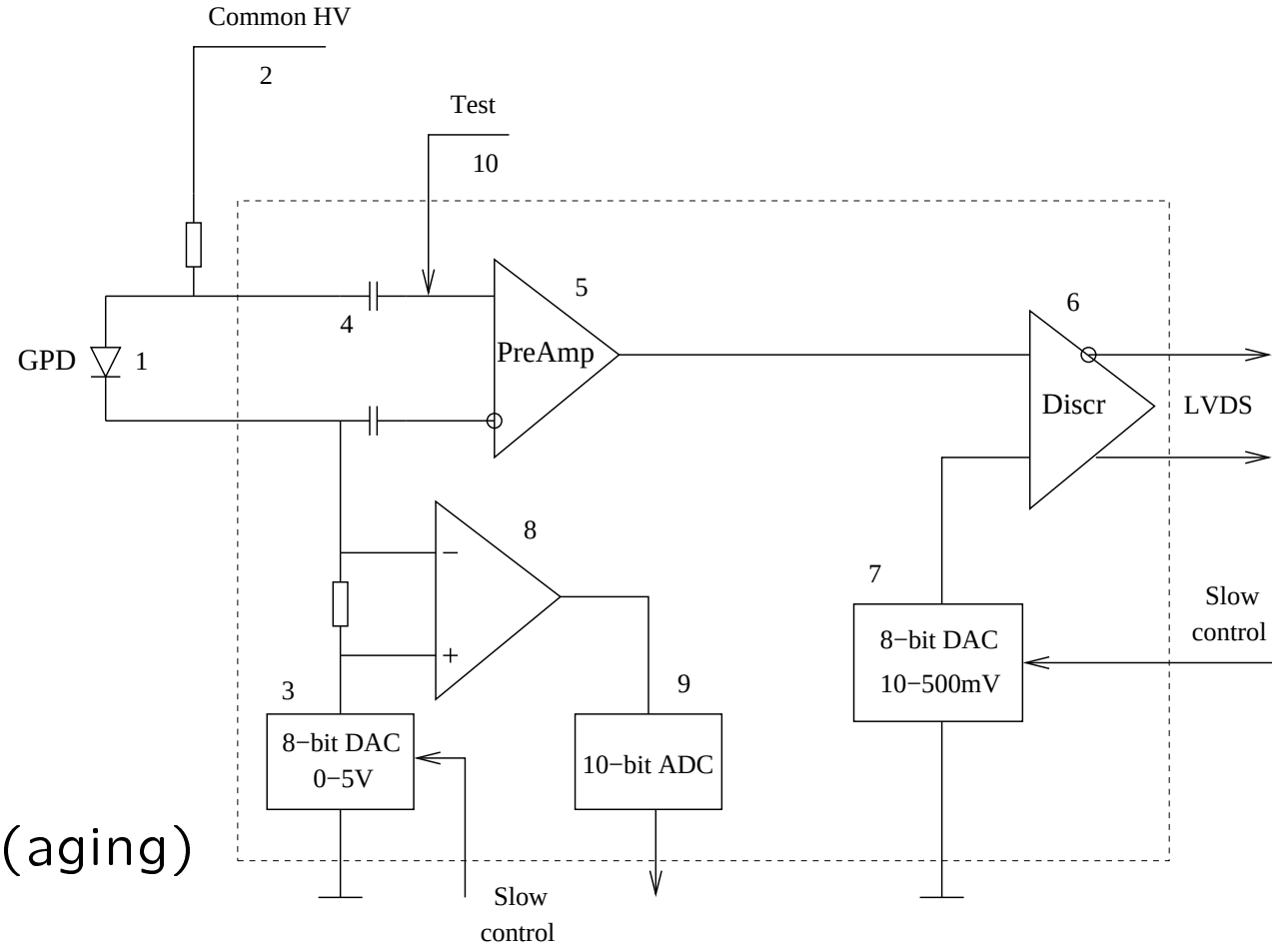
Rough scheme

1: Light detection

5 – 6: Signal measurement

3: HV adjustment

8 – 9: Current measurement (aging)



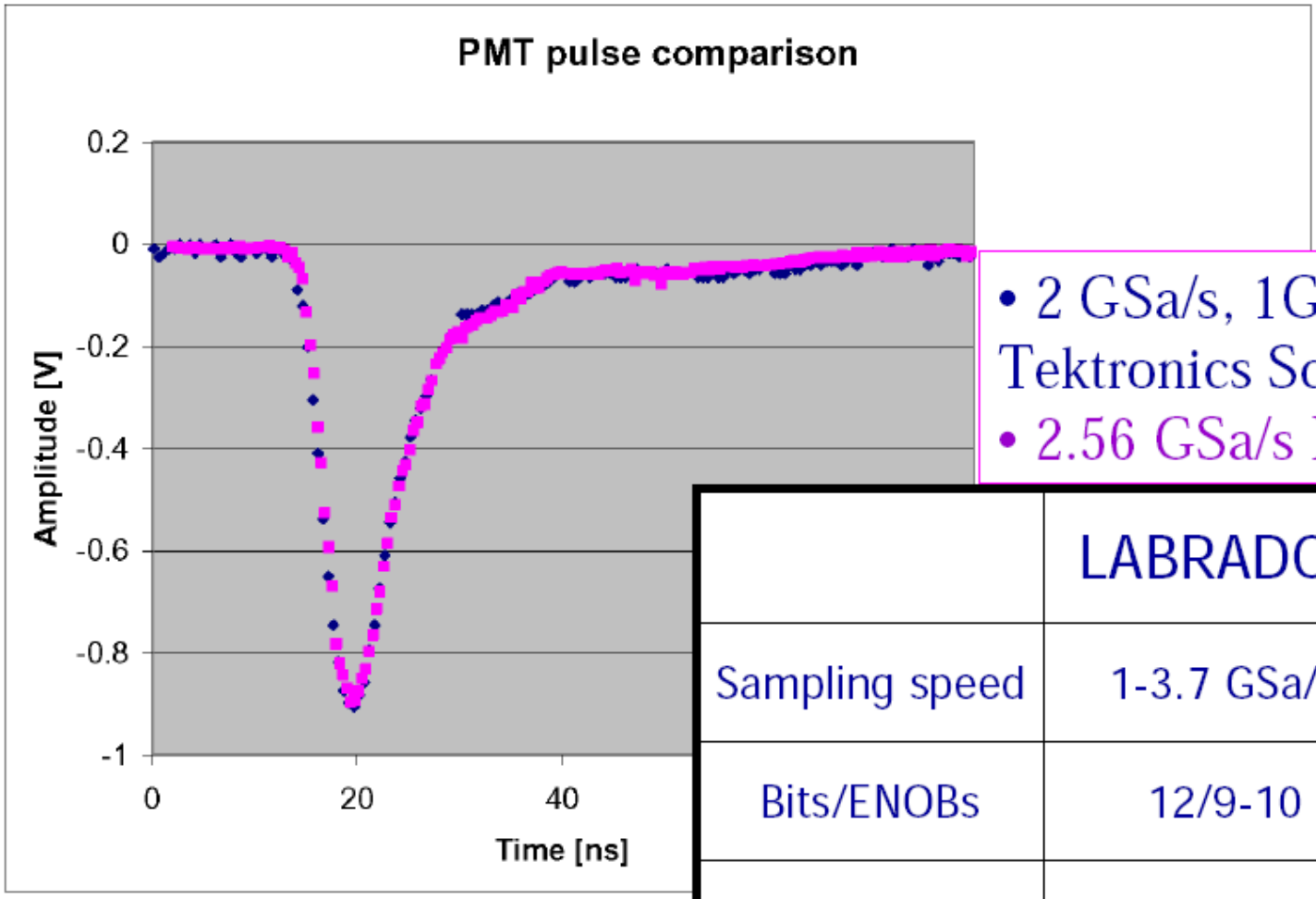
Good time resolution is crucial.

Possible ASIC Options

Subdetector	ASIC	ref. ASIC	Location	FPGA link
SVD3	APV25		E-hut	no
new SVD	BSR/KUPID	APV25	hybrid/dock	yes
CDC	BCA	TARGET	in detector	yes
PID SiPMT	BCA	TARGET	in detector	yes
PID HP-PMT	HPBA	BLAB2	in detector	yes
ECL	N/A		on detector	yes
Scint. KLM	BCA	TARGET	in detector	yes
VFV	BCA	TARGET	in detector	yes

- Basis of all chips = waveform sampling ("oscilloscope on a chip")
  - Amplifier design (BSR/KUPID) hard – won't report today
  - TARGET prototype ASIC (TeV gamma) results
  - BLAB2 prototype (precision timing) preliminary results

Motivation – waveform sampling



- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

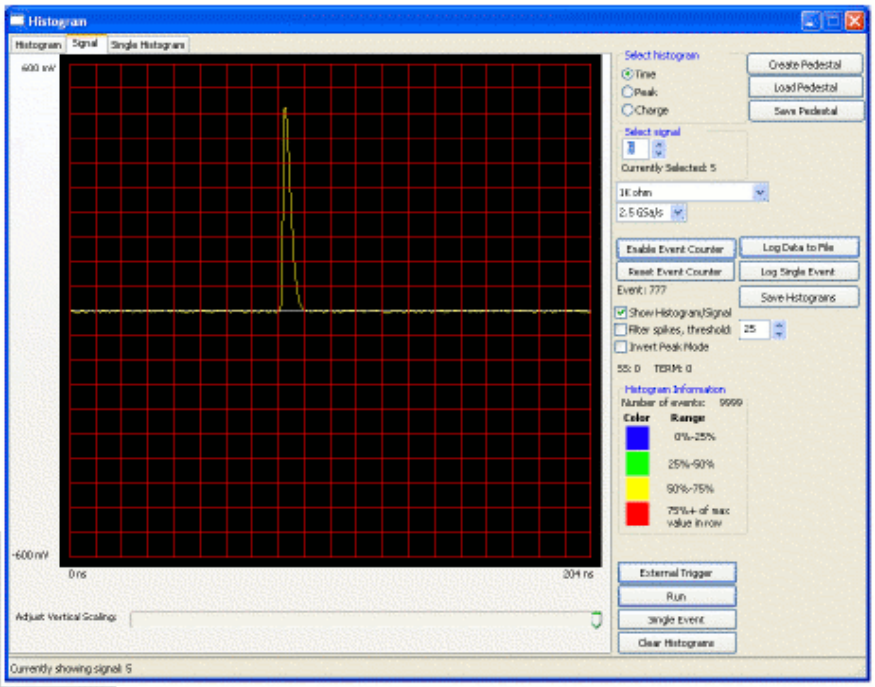
	LABRADOR	Commercial
Sampling speed	1-3.7 GSa/s	2 GSa/s
Bits/ENOBs	12/9-10	8/7.4
Power/Chan.	<= 0.05W	5-10W
Cost/Ch.	< $10	> 1k$

Signals shaping/ feature extraction in firmware

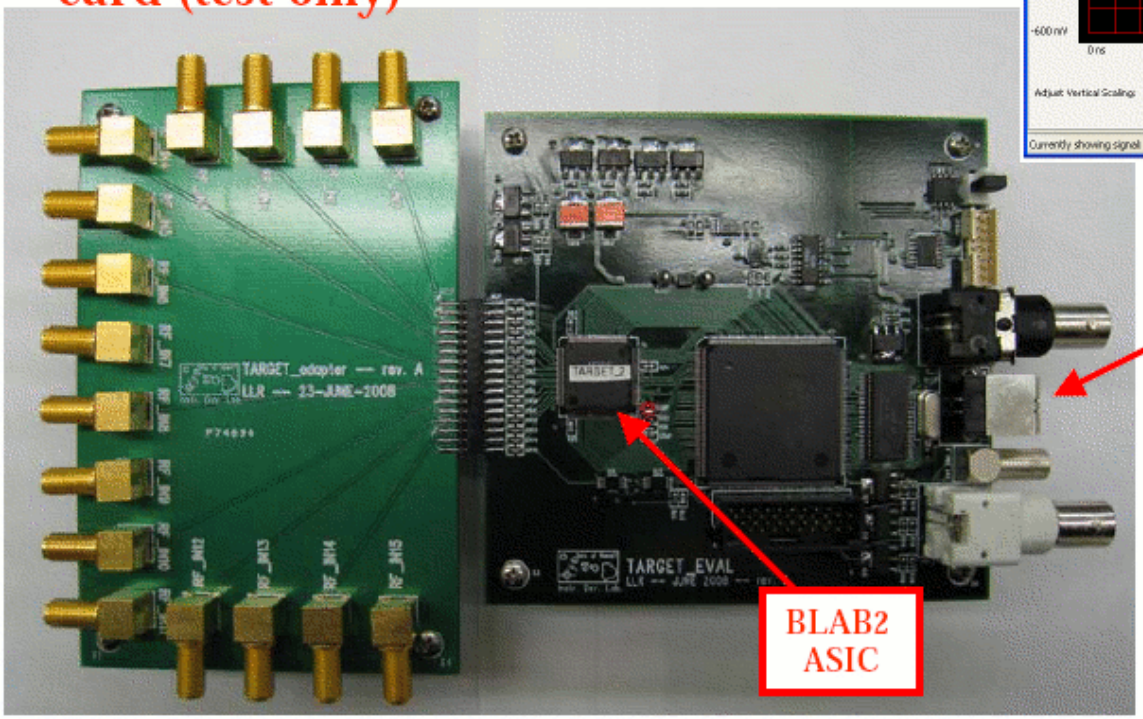
Gary Varner (Hawaii Univ.)

TARGET Eval Board

Can use laptop as DAQ system



Signal fan-in card (test only)

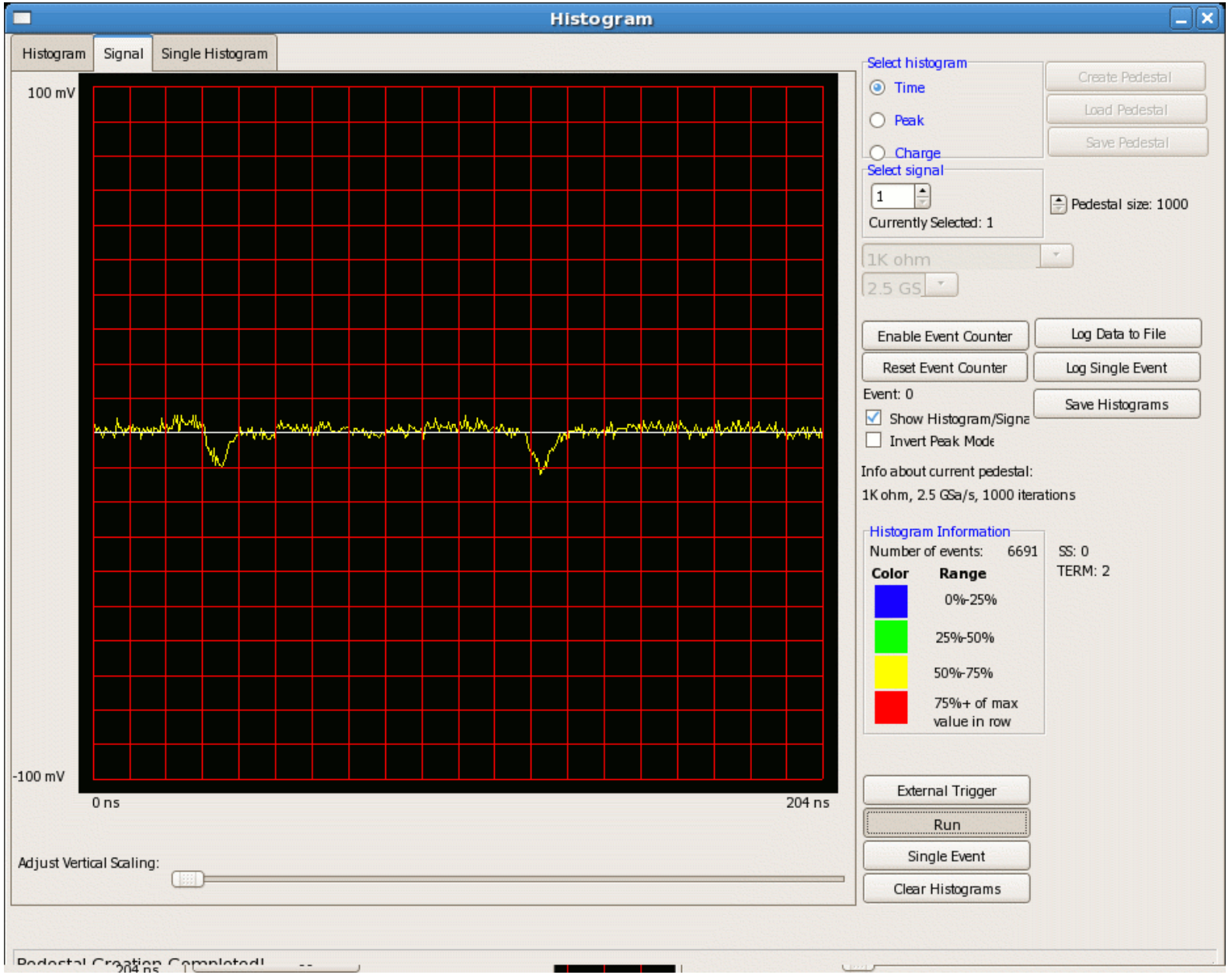


Eval board USB2 RO

- Win XP
- Linux
- Mac OS-X

10 mV ~ 20 p.e.

10 ns



Summary

- Hawaii's BLAB ASIC is regarded as very good option for endcaps KLM front-end electronics;
- First test is OK, but more elaborated study is planned (sensitivity, stability, cross-talks etc);
- ASIC development is ongoing.

"Common infrastructure ASICs for detector readout", Gary Varner (Detector Upgrade Meeting, 18 September 2008)

arxiv.org