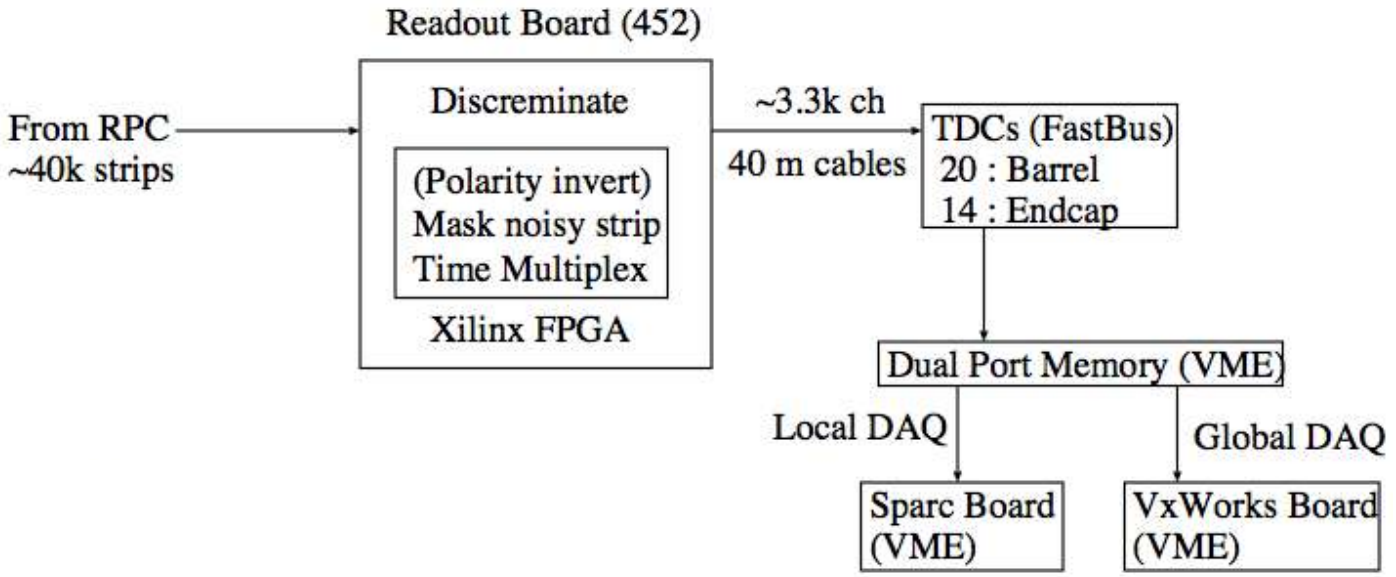
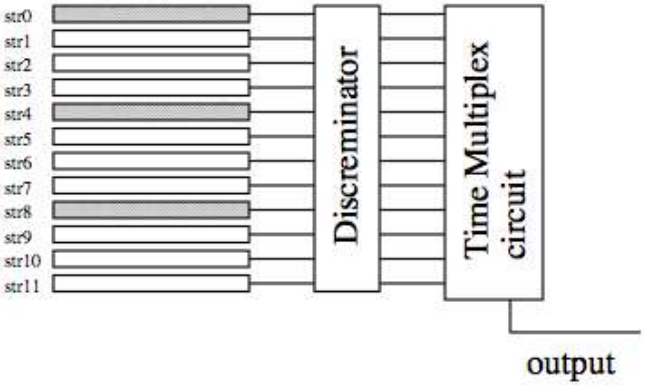
Electronics

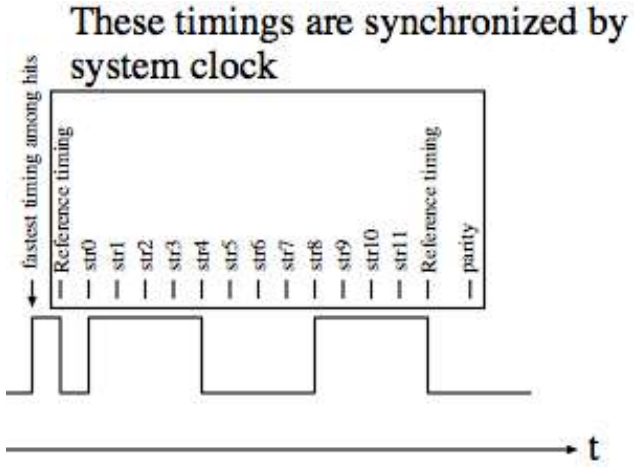
Yosuke Yusa
Virginia Tech.

Current setup

- Strip hit position information is converted to timing information in front-end.
- Data is taken by FASTBUS TDC (LeCroy 1877S) and unpacked off-line







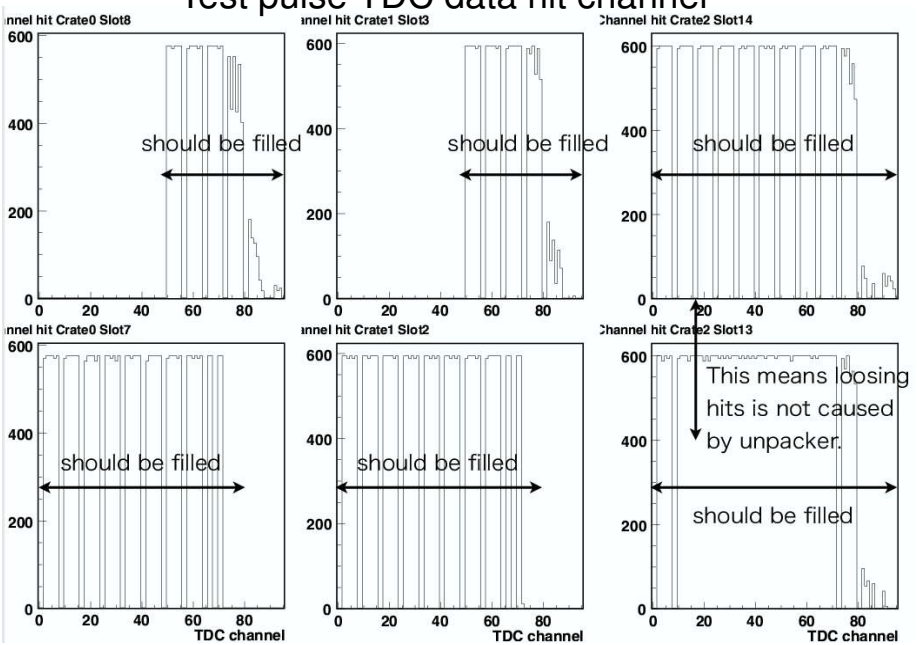
TDC upgrade

In this summer, we tried to replace FASTBUS system to COPPER one (pipe-line readout).
We have installed 3 9U VME crates and 34 COPPER boards in electronics hut.
Controller and trigger modules are also replaced.
On/off-line softwares (readout board control, data unpacker, quality monitor) are also ready.

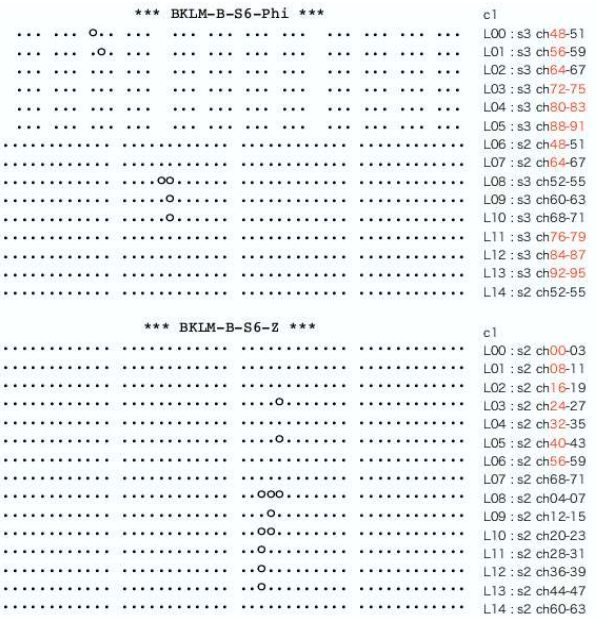
A part of TDC cables are connected
(top and bottom sectors of barrel, endcap 1 sector)
and test pulse and cosmic runs are taken.

TDC upgrade

Test pulse TDC data hit channel



cosmic ray track



In some channels, hits are lost both test pulse and cosmic run

→ We put back cables to FASTBUS and take data using old system in autumn run.

No error message was recorded in basf output log on COPPER.

No such hit lost observed when we take test pulse data in B2 test bench.

No significant difference is observed when we check test pulse shape of each channel using oscilloscope in B2 test bench.

During winter shutdown, we will change the system to COPPER and try to solve this issue.

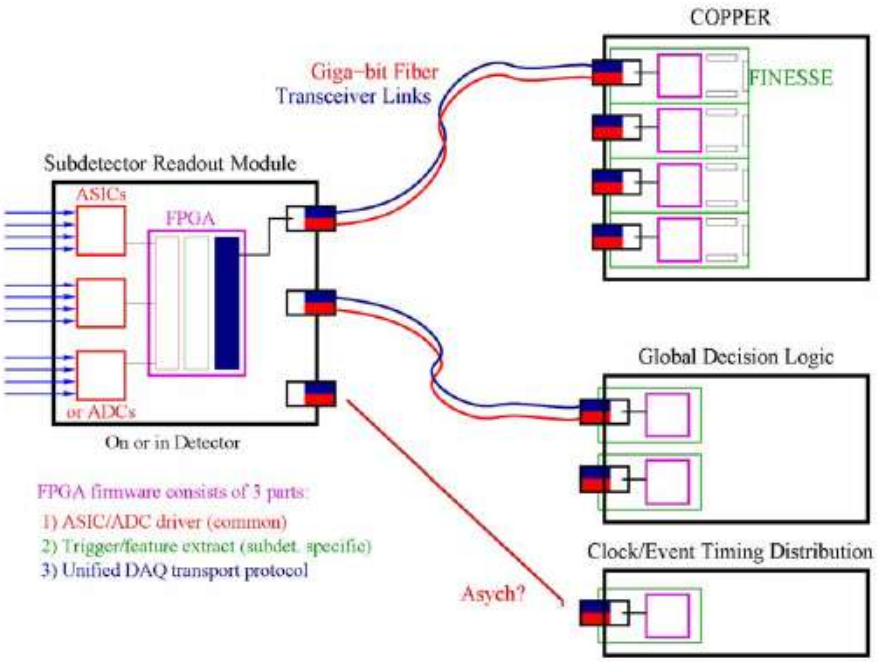
New front-end for sBelle

Due to increase of event rate in endcap part, RPC will be replaced to scintillator+SiPM detector and new detector needs new front-end electronics.
→ What kind of readout system in sBelle KLM?

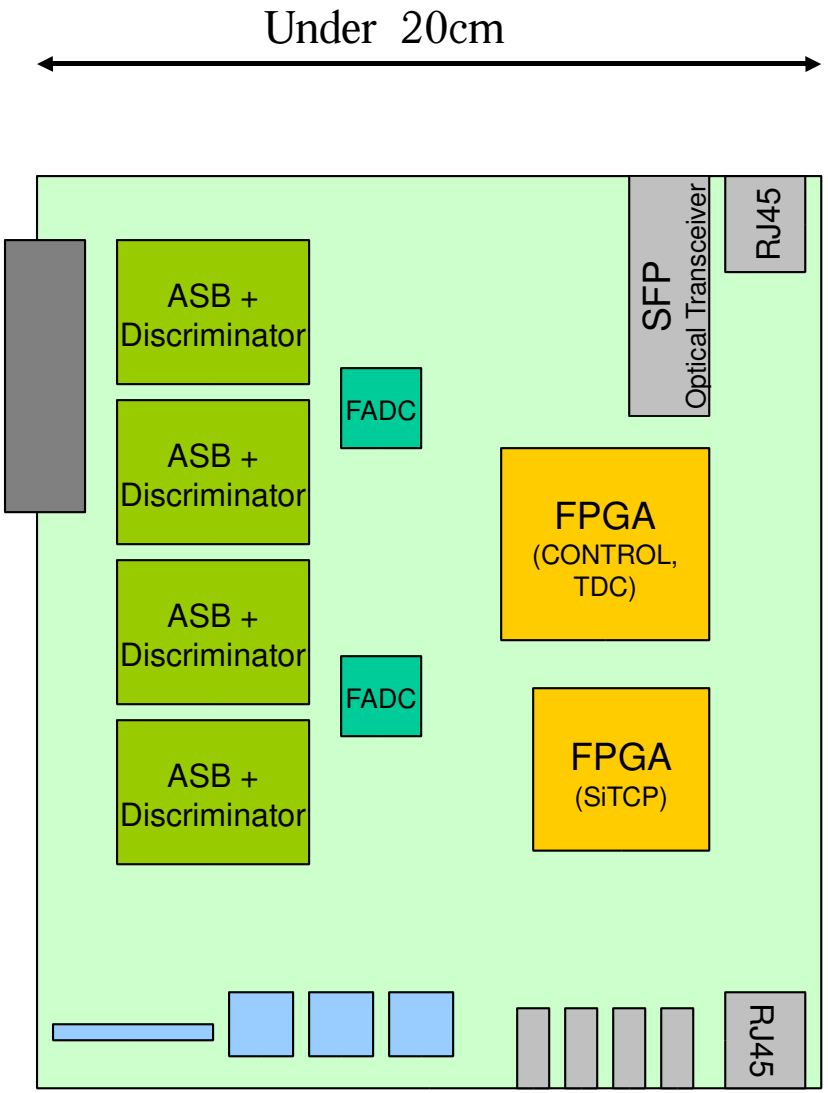
Minimum option:
Assemble pre-readout board for endcap detector and use current readout boards.
Can current Q-T scheme work under super-B high input rate environments?
In sBelle, we don't need to use TDC: no merit to do Q-T conversion.

DAQ group recommends:
Develop New readout module for "extended FINESSE".

What kind of design?
Who/Which institute do it?



CDC Readout board Prototype1



- 16ch/board
- BJT-ASB/Comparator part
- FADC: over 20MHz / 10bit
- FPGA : Vertex-5 LXT
  - TDC: 1 nsec counting
  - FADC reading
  - Control
- FPGA: Spertan3A
  - SiTCP
- RJ-45 for SiTCP
- RJ-45 for Belle DAQ timing signals
- SFP for Belle DAQ data line
- LEMO input x 3
- LEMO output x1
- Shielded substrate

Summary

- We install COPPER for KLM before autumn run
  Event lost in some channels was found, then we postpone the system change.

- For sBelle KLM, we need new front-end electronics.
  New readout board? minimum pre-readout board for endcap?
  We need discussion.

If you are interested in new DAQ scheme, please join DAQ parallel session tomorrow.