

CAP7: electronics tests

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PXD session

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CAP7 summary

- CAP7: follow up of CAP4/CAP5 in SOI, received 11/2008

Leakage current

NMOS characteristics under HV

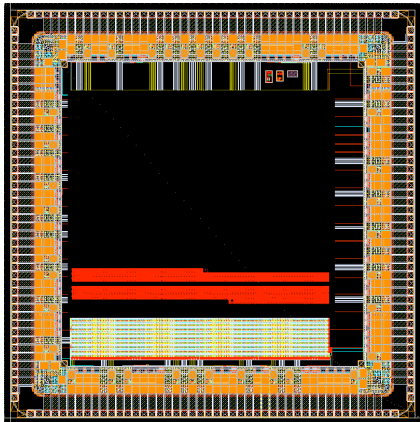
Test structures of on-pixel logic

- RS flip-flop
- D flip-flop
- Comparator

Summary/outlook

CAP7 design in .2 μm OKI SOI

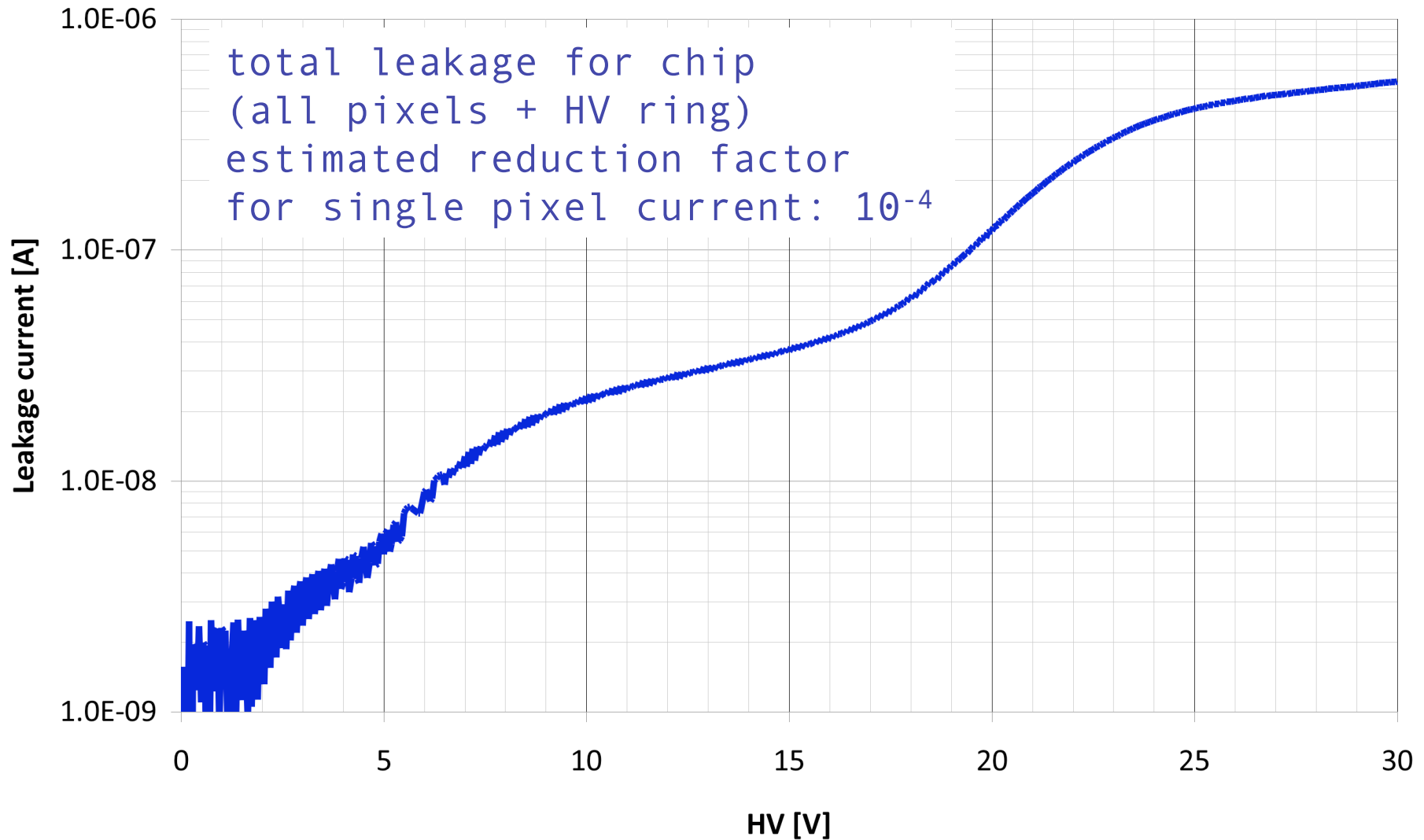
- binary design as in CAP4/5 for 2008 OKI MPW SOI run
- transparent latch replaced by d-flip flop (no chatter)
- submitted 1/2008
- delayed due to fabrication issue
- final chip received late 11/2008 beginning 12/2008
- electronic tests of unpackaged die on probe station:
 - total leakage current of chip: 20 nA @ 10V HV
 - bare nmos transistor: treshold shift of 65 mV @ 20V HV
 - on pixel logic: RSFF, DFF, Comparator;



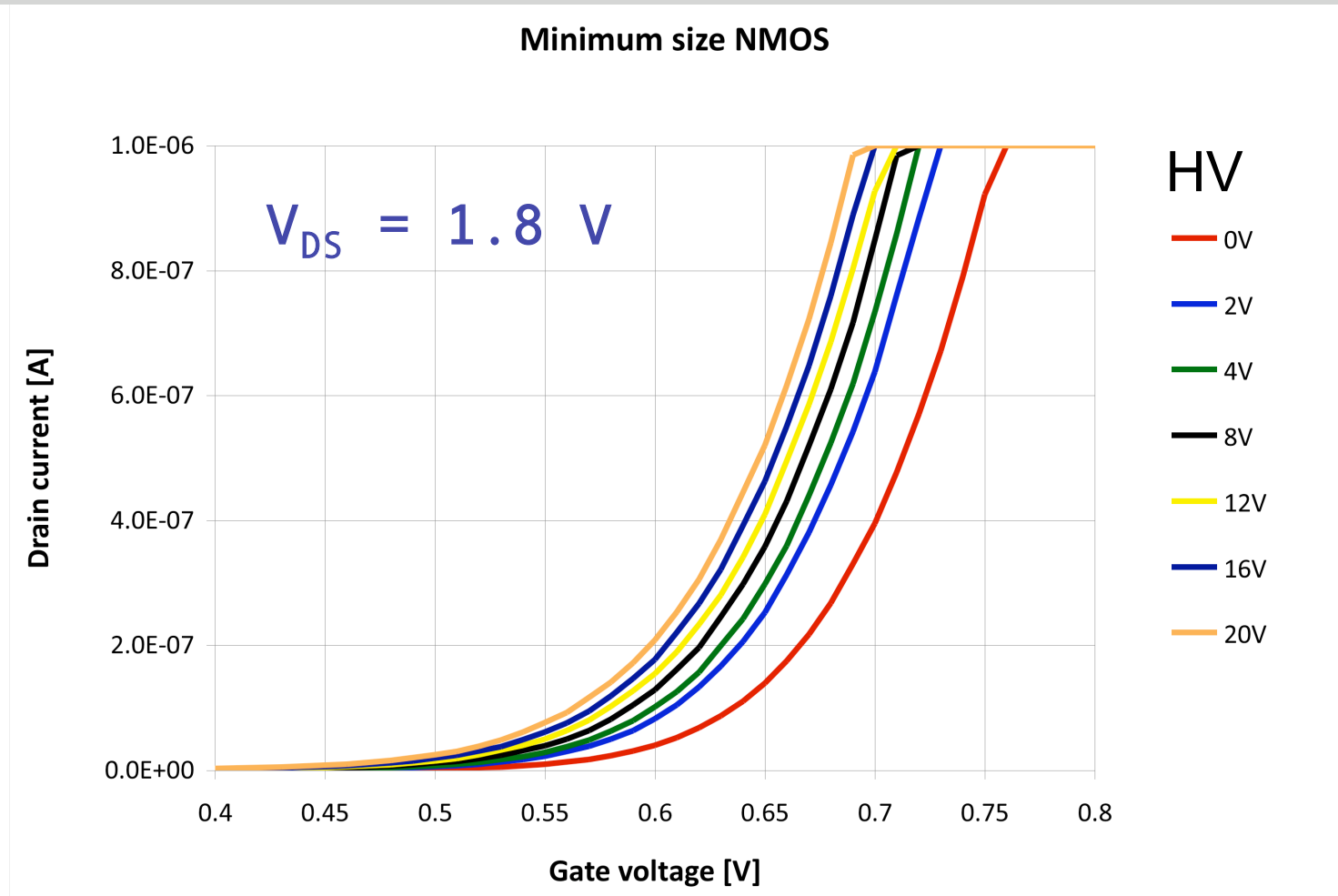
total dimensions: 5mm x 5mm
active area: ~3mm x ~3mm
total pixels: 6000
pixel cell: 35x50 μm^2
test structures each sub-component

designed by M. Cooney

Leakage current



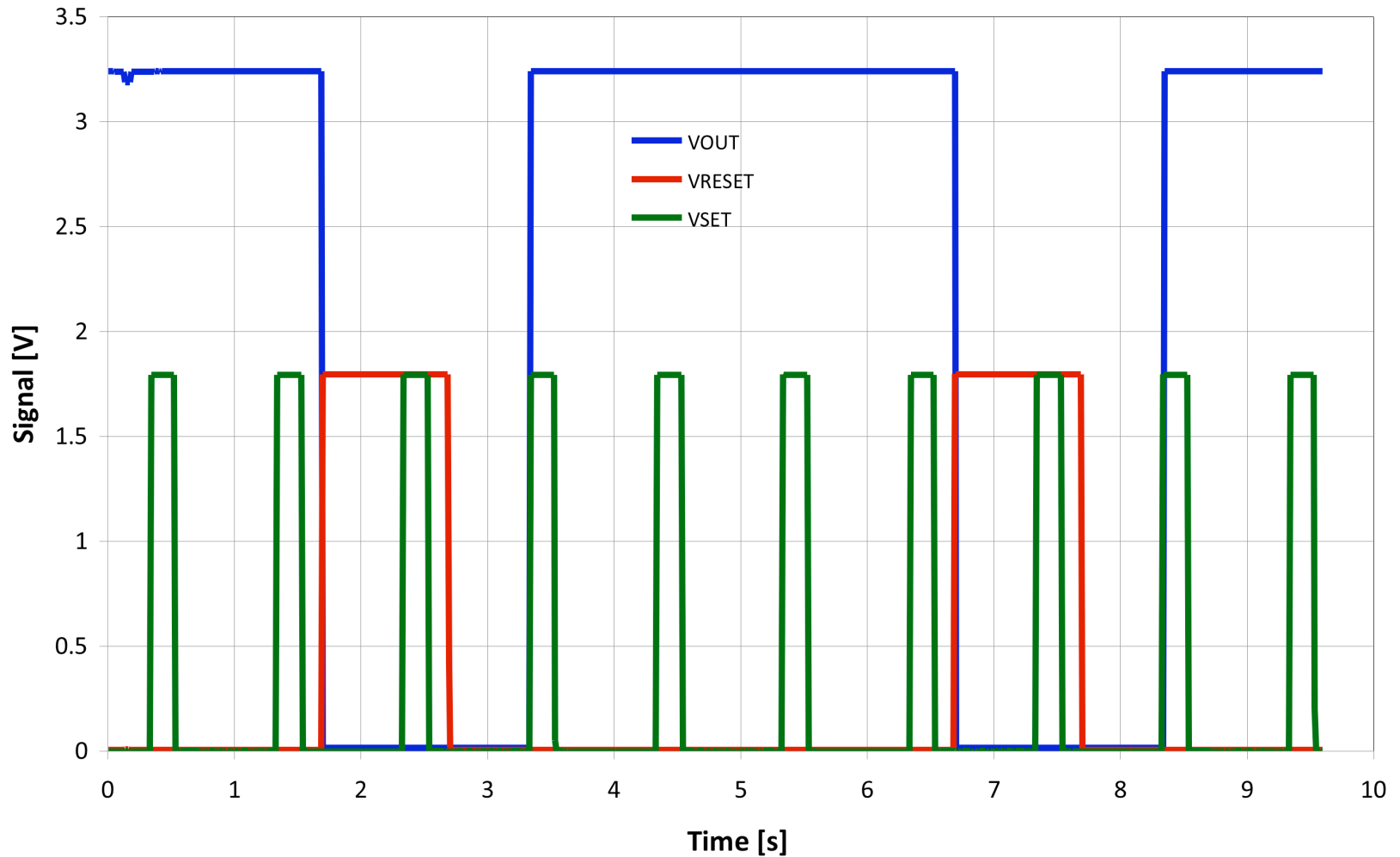
NMOS Characteristics under HV



isolated test structure
threshold shift: 65 mV at 20 V

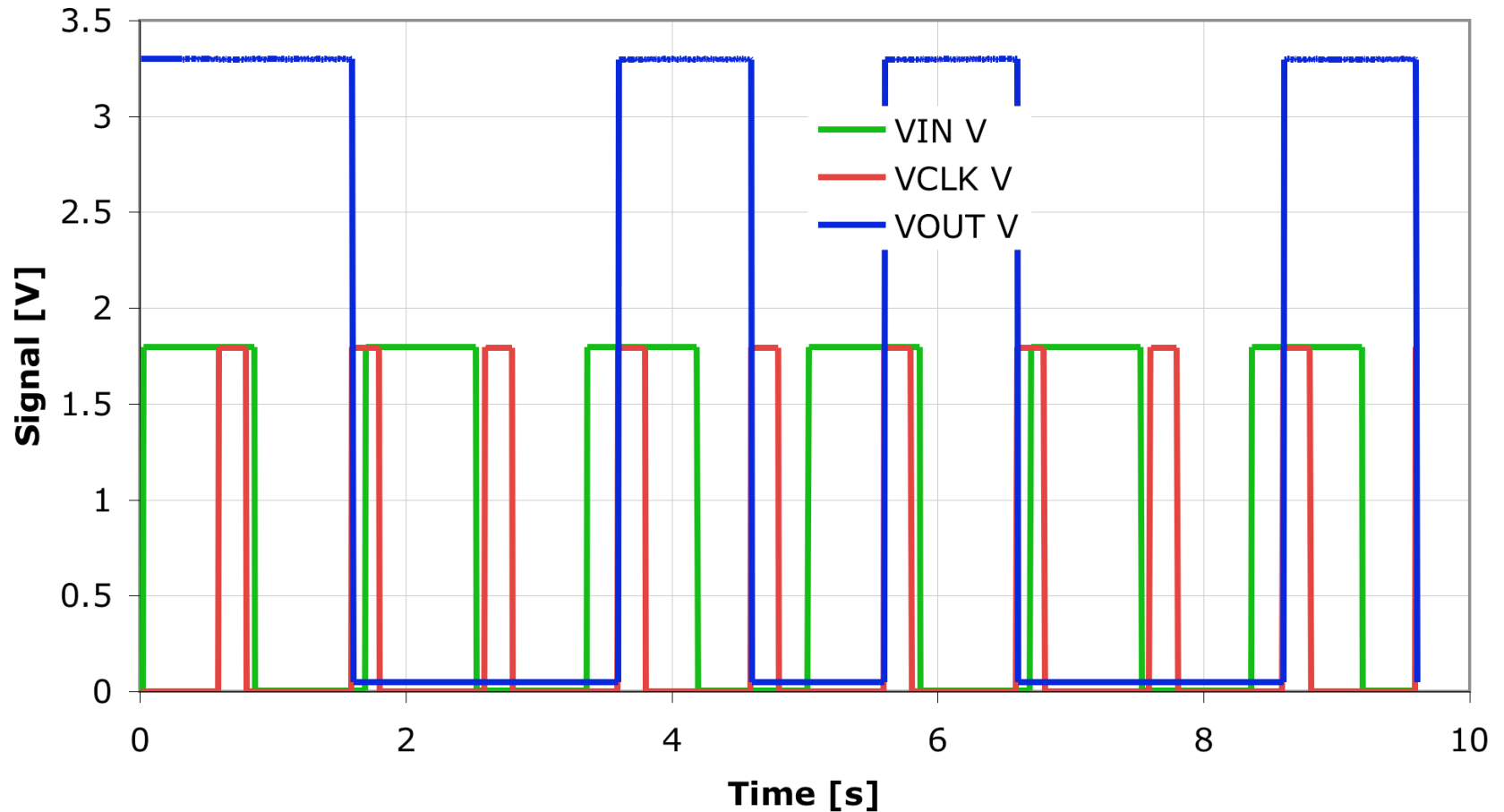
RS flip-flop

HV = 40V



D flip-flop

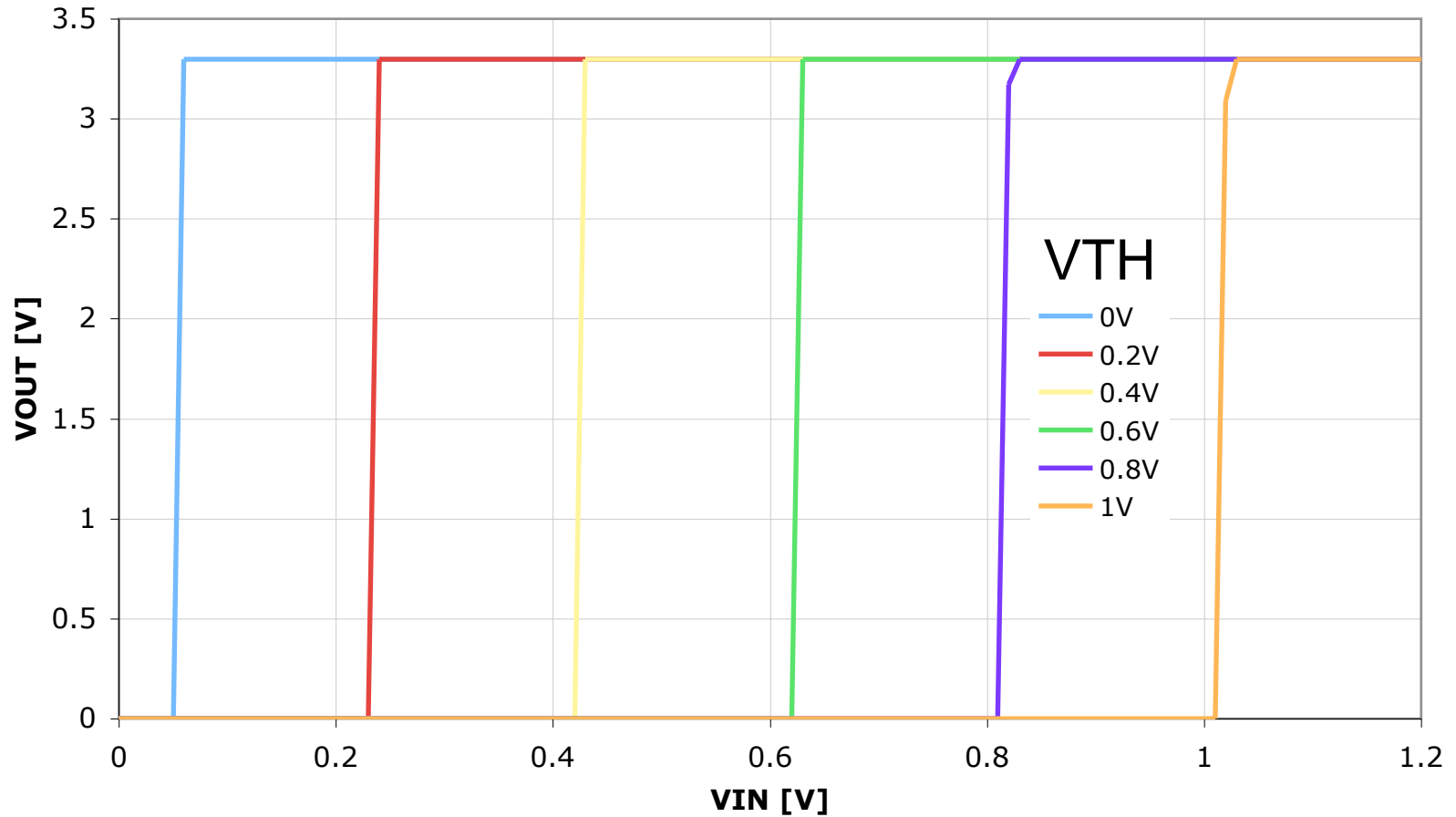
HV = 10V



updating errors for larger HV? (updates at falling edge)

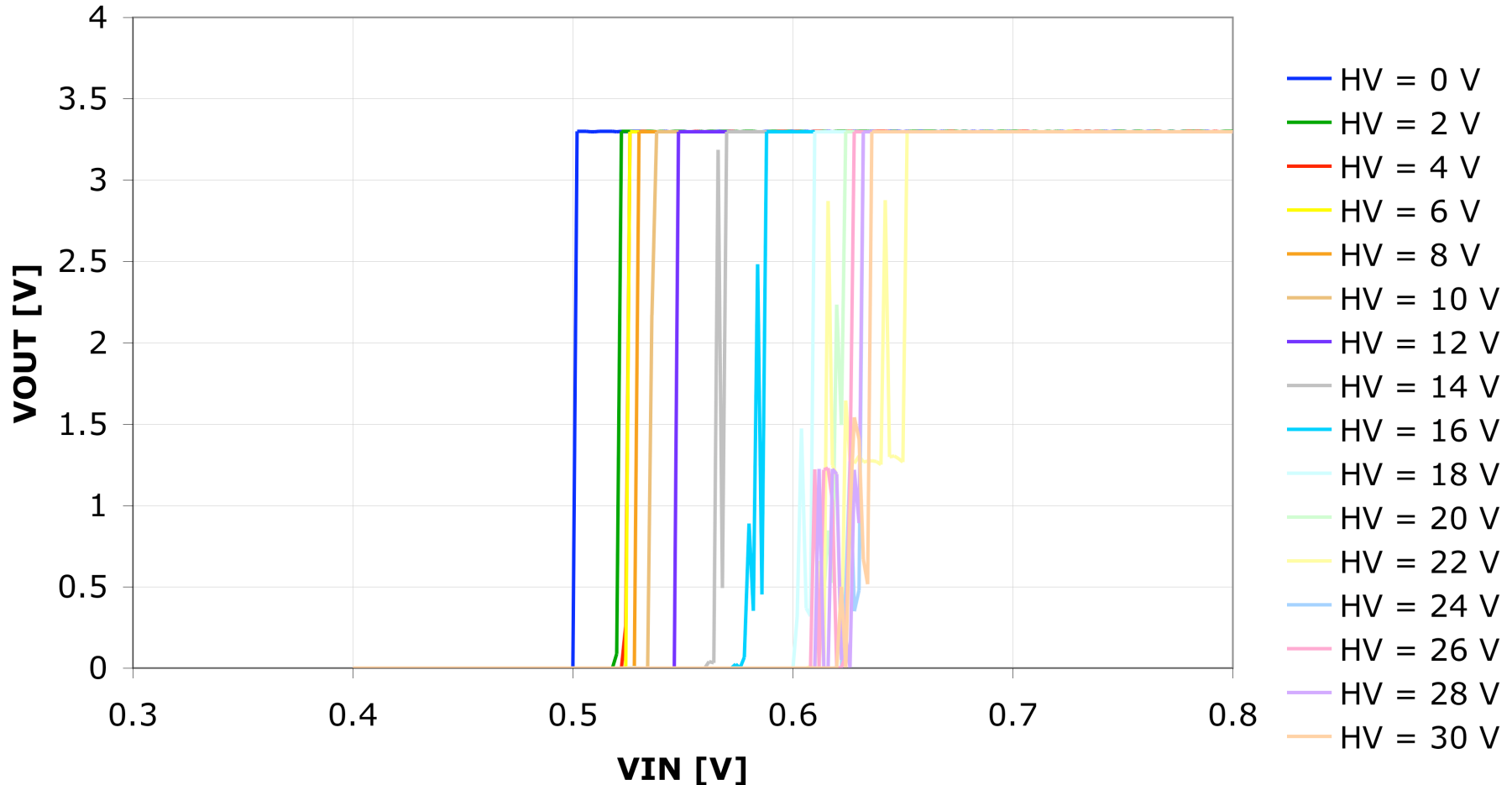
Comparator: threshold scan

Threshold Scan @ HV = 5V
VB = 0.4 V



Comparator: back-gate effect

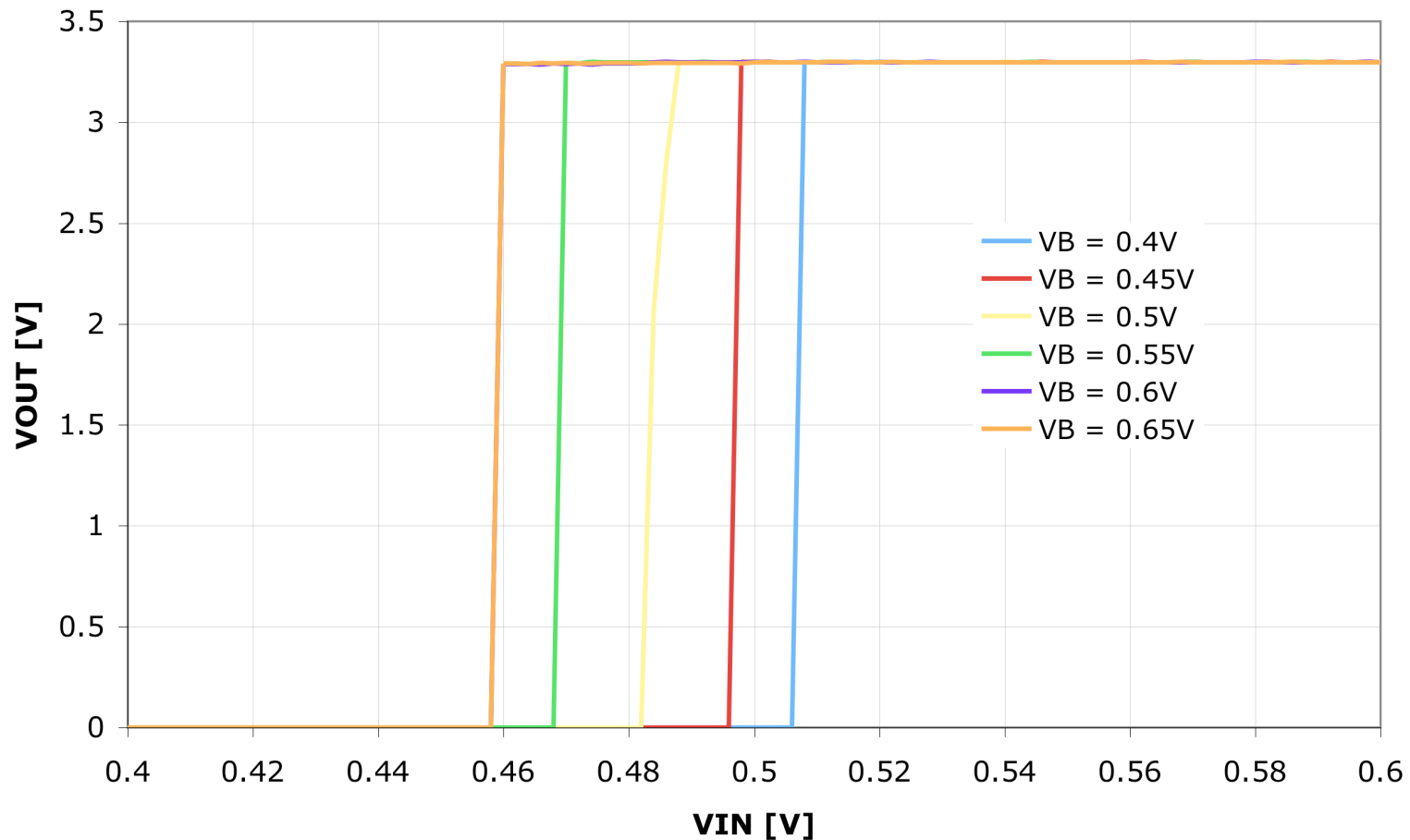
Comparator output for fixed $V_{TH} = 0.5 \text{ V}$ and varying HV



Comparator: bias scan

variation of the turn-on with comparator bias

Comparator: VB scan for fixed HV = 0V and VTH = 0.5 V



Summary and outlook

- received unpackaged version of CAP7 last week
- carried out electronics tests on probe station
- leakage current: slightly higher than CAP5
need to cross check on packaged version
- digital logic (DFF, RSFF) seems to work fine, also at medium - high HV.
- comparator:
 - + comparator works (did not work at all in CAP5)
 - threshold is rather sensitive to HV
- packaged dies due to arrive tomorrow
- readout board, firmware and software ready for testing