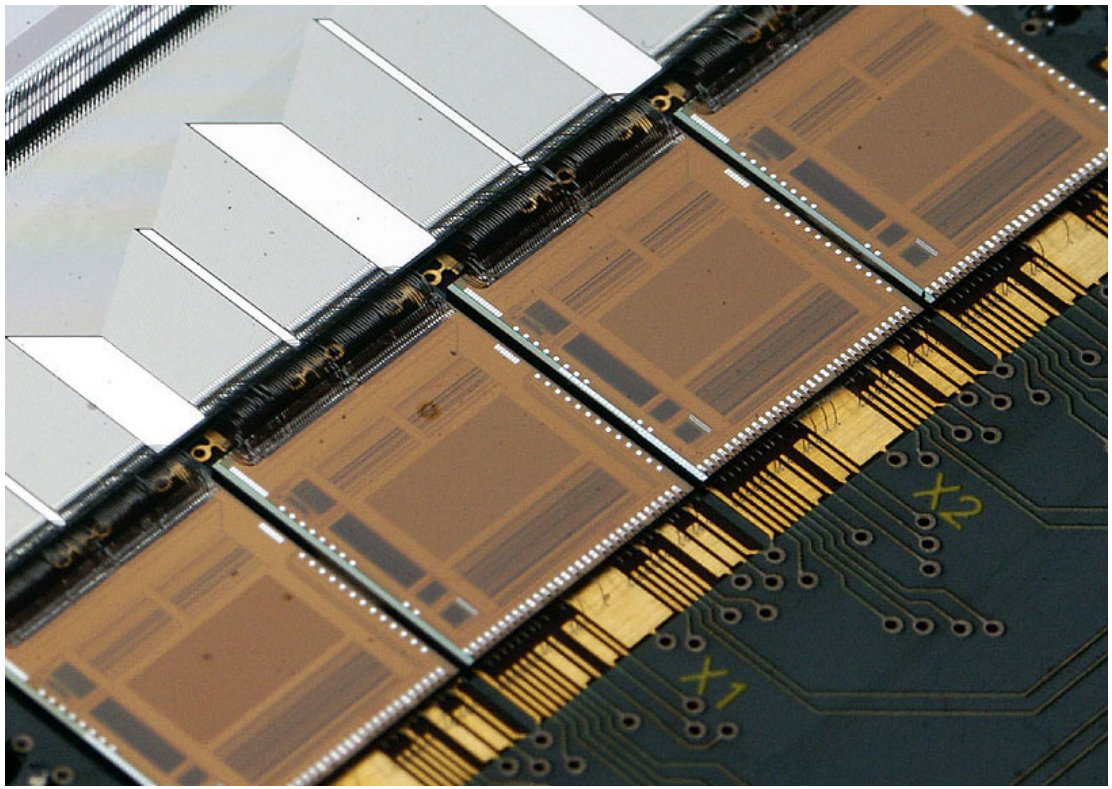
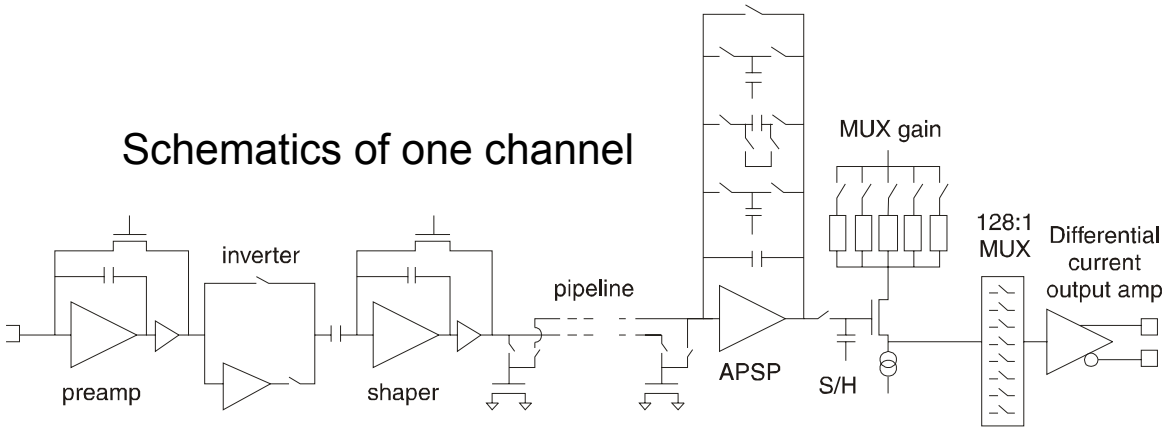
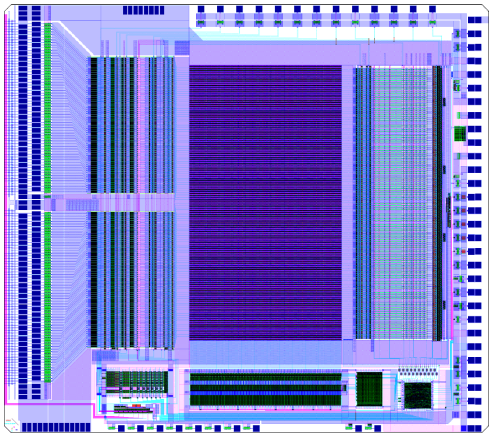


APV25 for SuperBelle SVD

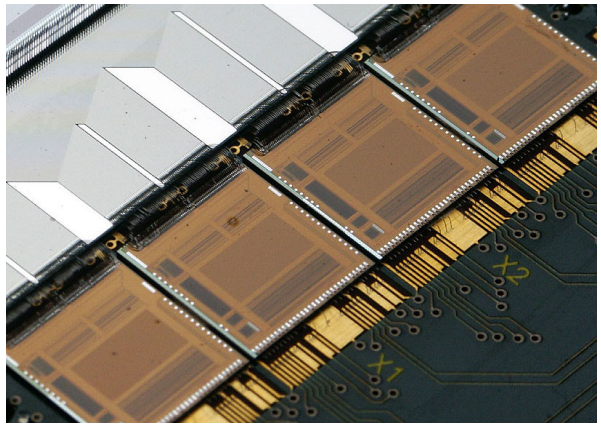
M.Friedl
HEPHY Vienna

APV25





- Developed for **CMS** by IC London and RAL (70k chips installed)
- 0.25 µm CMOS process (**>100 MRad tolerant**)
- **40 MHz clock** (adjustable), 128 channels, analog pipeline
- **50 ns shaping time** (adjustable)
- **Low noise: 250 e + 36 e/pF**
  - cf. BEETLE (LHCb) 497 e + 48 e/pF
  - cf. SVX4 (CDF,D0) 728 e + 56 e/pF
- **Multi-peak mode** (read out several samples along shaping curve)



APV25 Pipeline & Triggers

APV25 Pipeline

- **192 pipeline cells** (actually a ring buffer)
- After APV receives a trigger, the corresponding pipeline cells are labelled in an index FIFO in order not to be overwritten before the event is completely read out
- **Index FIFO** has **32 cells**

  → In worst case, **160 pipeline cells** always remain active

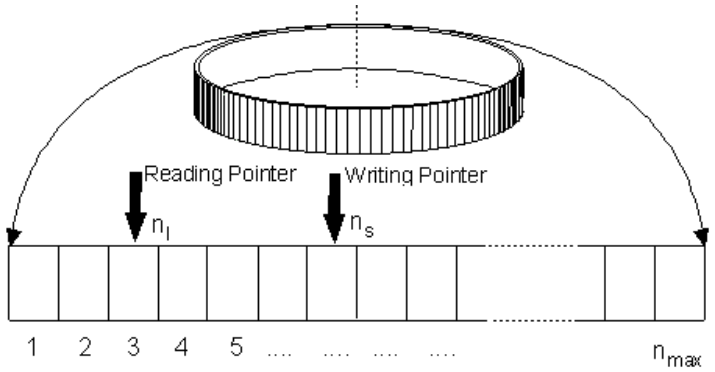
- = **3.8µs** @ **42.3MHz** clock (RF/12)

  → 3.5µs max. latency for L1

or

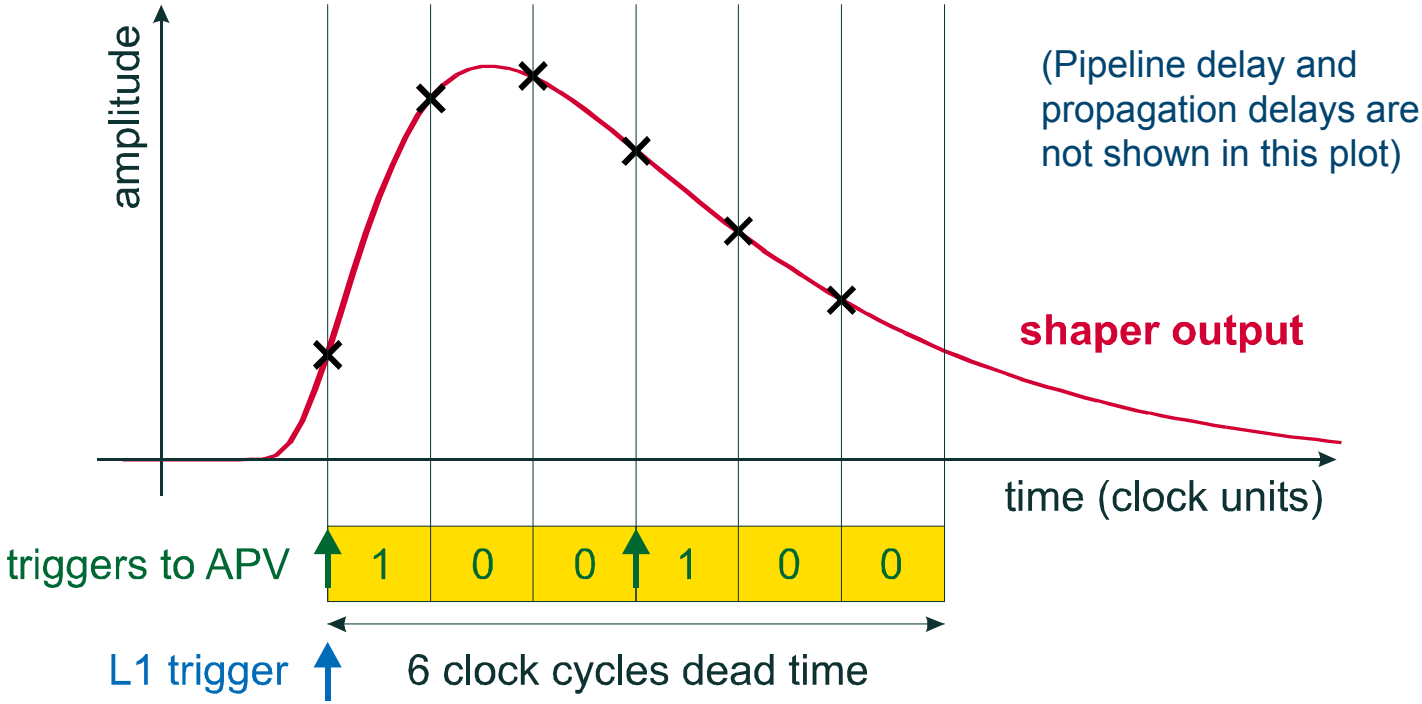
- = **5.0µs** @ **31.8MHz** clock (RF/16)

  → 4.7µs max. latency for L1



- Preferred by **Iwasaki-san**, but has implications on trigger rate (see below)

APV25 Triggers



- APV controller ("NECO") generates **2 consecutive trigger symbols ("100") to APV** from L1, resulting in 6 samples along shaped waveform
  → allows **peak time reconstruction** (few ns precision, see talk by C.I.)
- **No triggers** allowed during **6 clocks** after L1

APV25 Trigger Restrictions

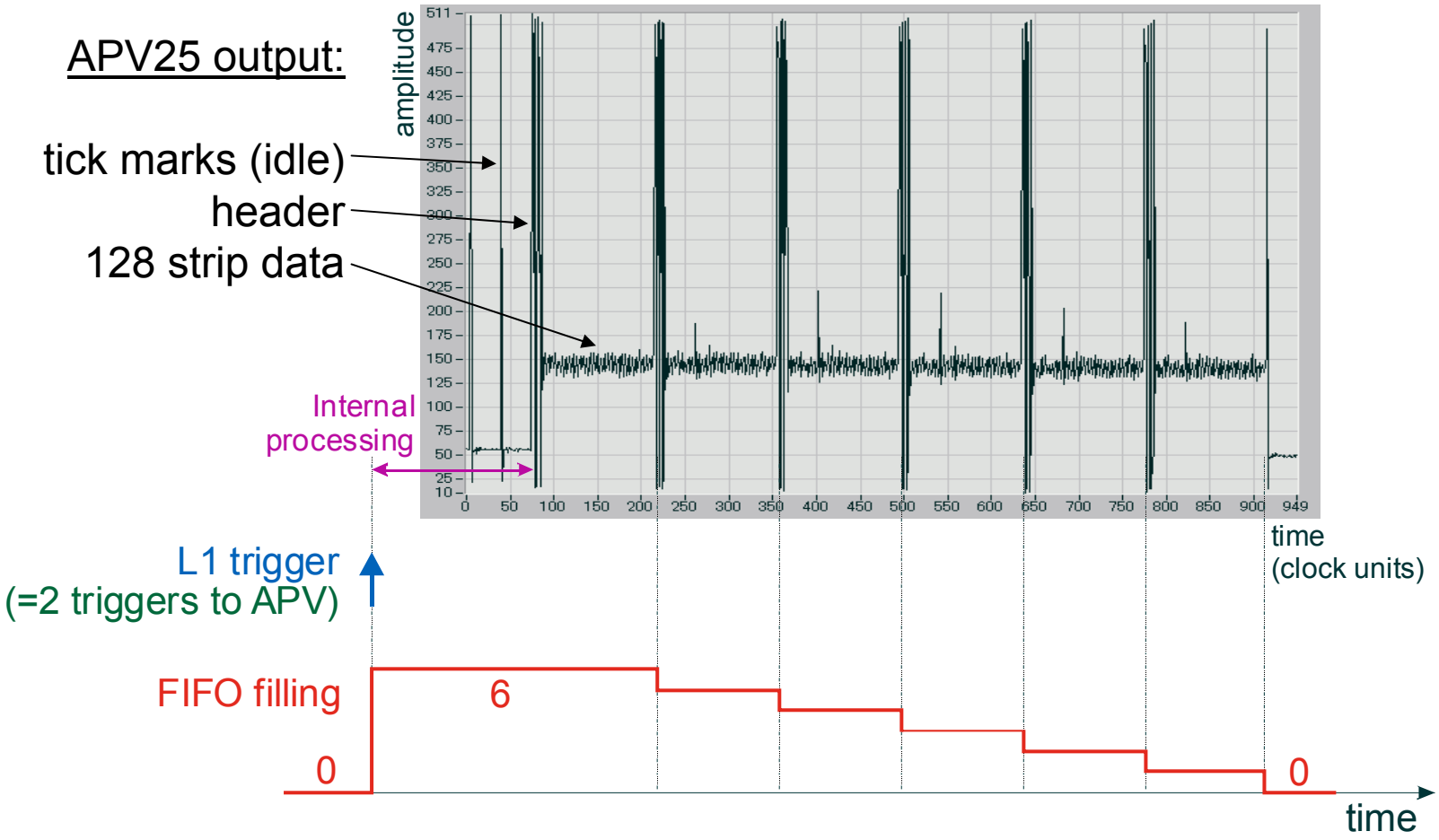
(1) Minimum L1 distance of 6 APV clocks

(2) Maximum pipeline index FIFO filling of 32

Let‘s see what (2) means…

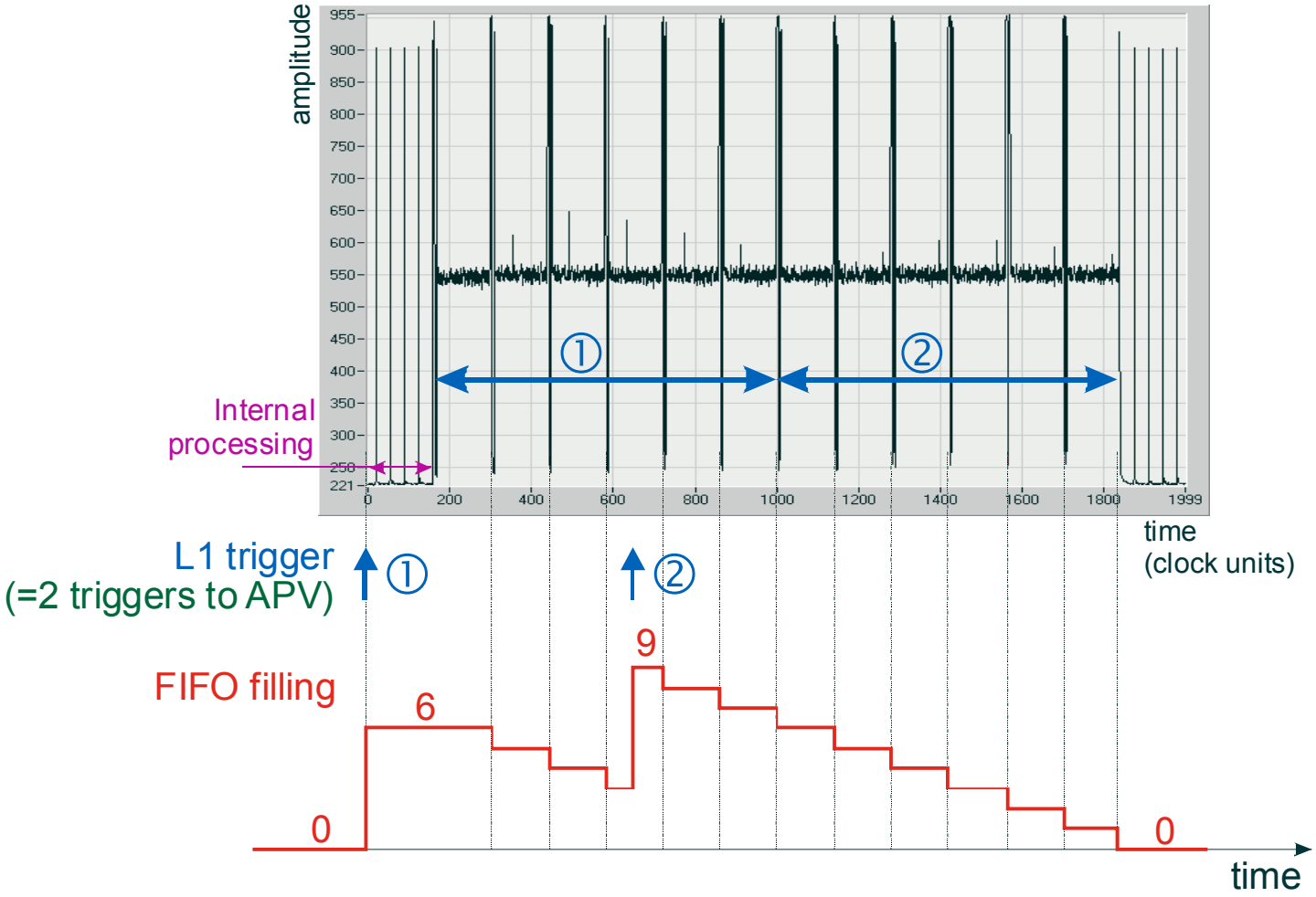
APV Output and FIFO Filling (1)

- **Single L1 trigger** resulting in 6 samples



APV Output and FIFO Filling (2)

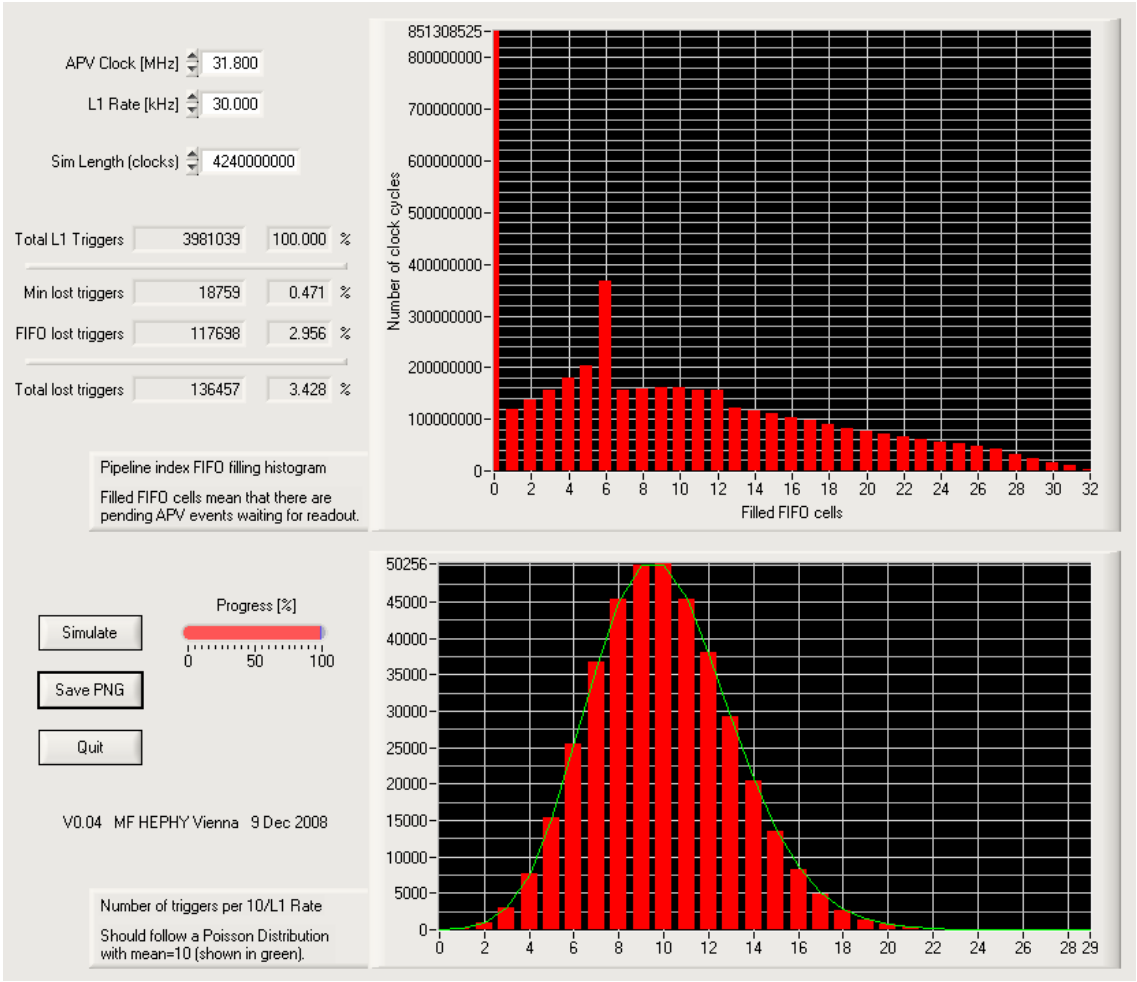
- **Two L1 triggers** resulting in 12 samples



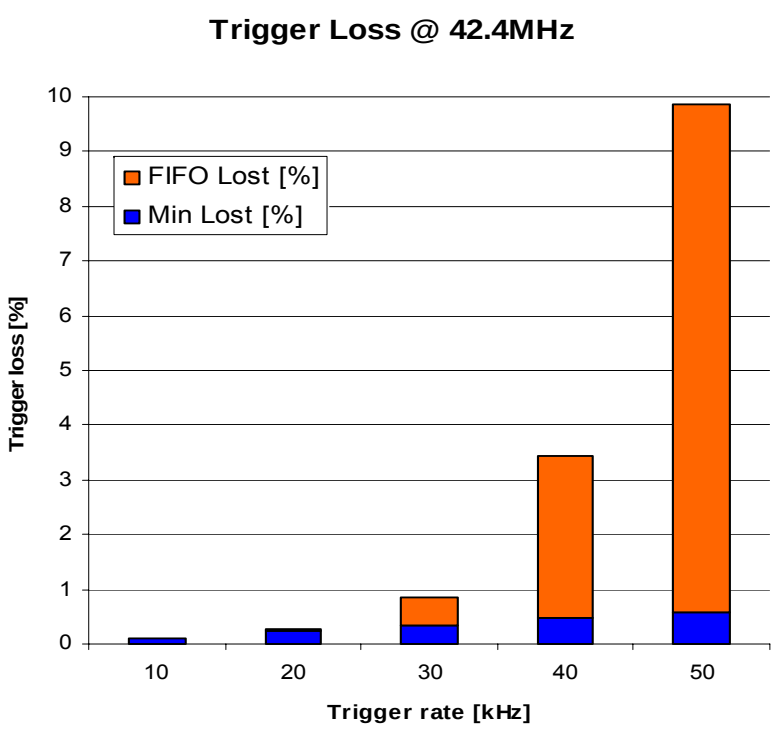
APV Trigger Simulation (1)

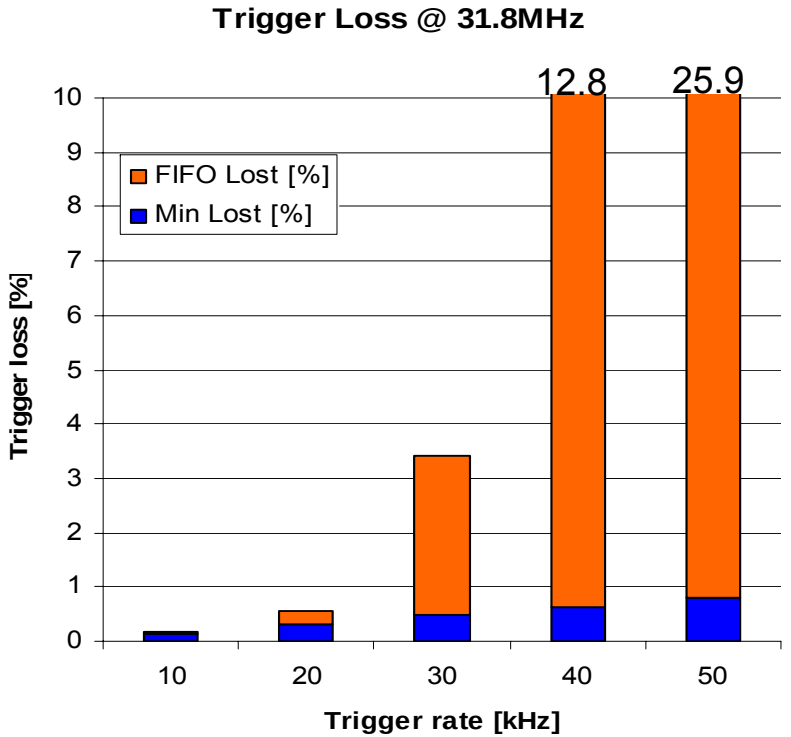
- *Input:* **CLK**, **L1 rate**
- *Model:* **APV25** state machine, **exponential trigger** distribution
- *Output:* **FIFO filling** histogram, **trigger loss**, **Poisson distribution** to check randomness of simulated triggers

Download:
http://belle.hephy.at/apvtrg.zip
(needs Labwindows/CVI 8.1 run-time engine from http://ni.com)

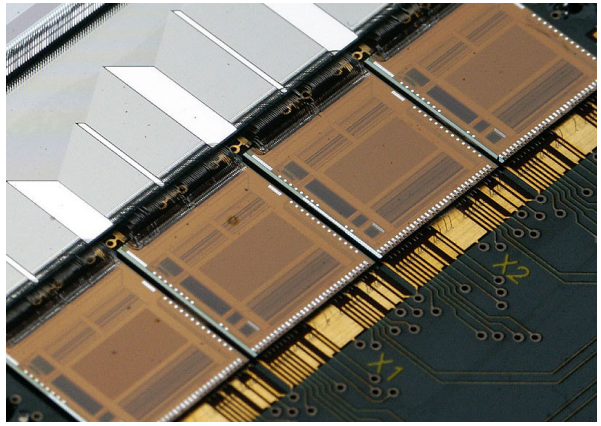


APV Trigger Simulation (2)



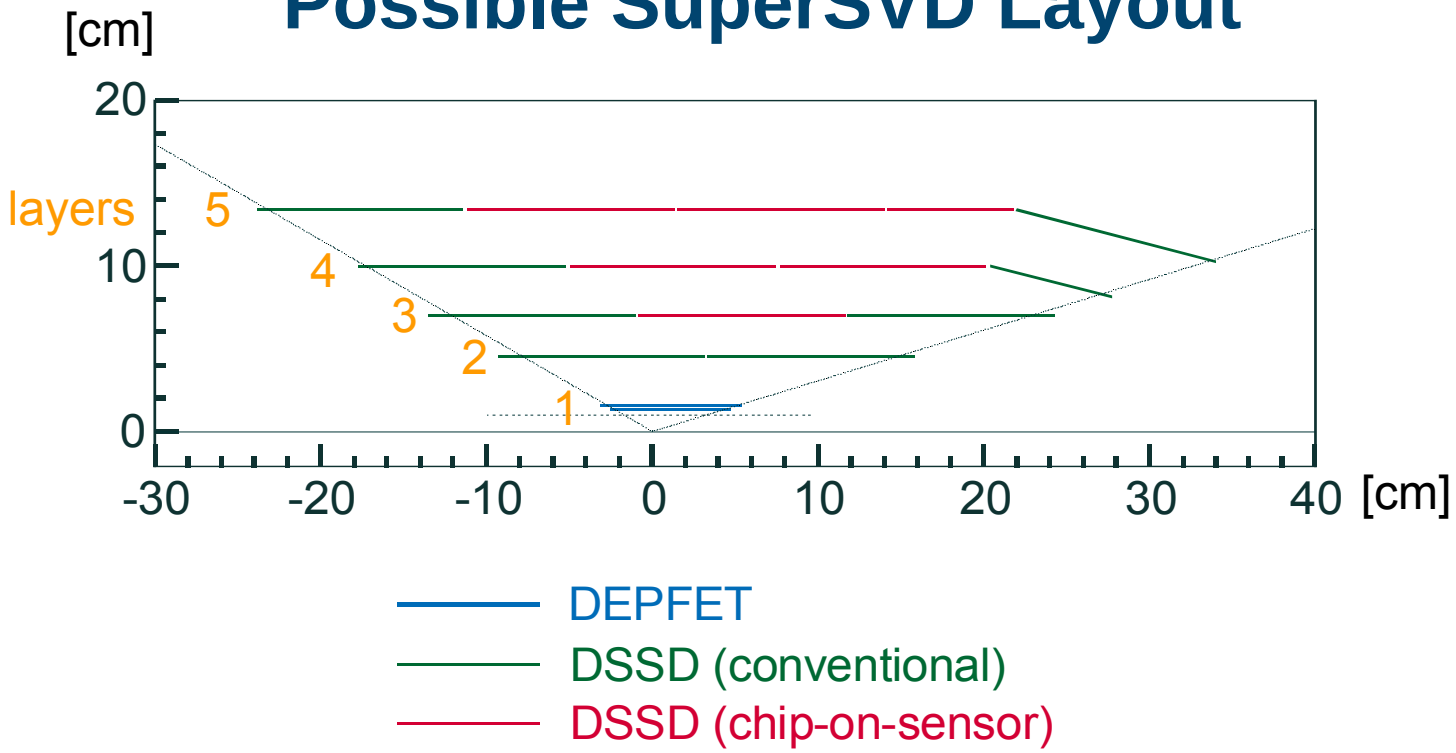


- **Min Lost**: trigger restriction (1) = too little distance
- **FIFO Lost**: trigger restriction (2) = too many pending readouts
- **Nakao-san** wishes <3% dead time @ L1=30kHz
- → **OK (0.87%) for 42.4MHz** clock, **slightly higher (3.43%) at 31.8MHz**



Chip-on-Sensor Concept

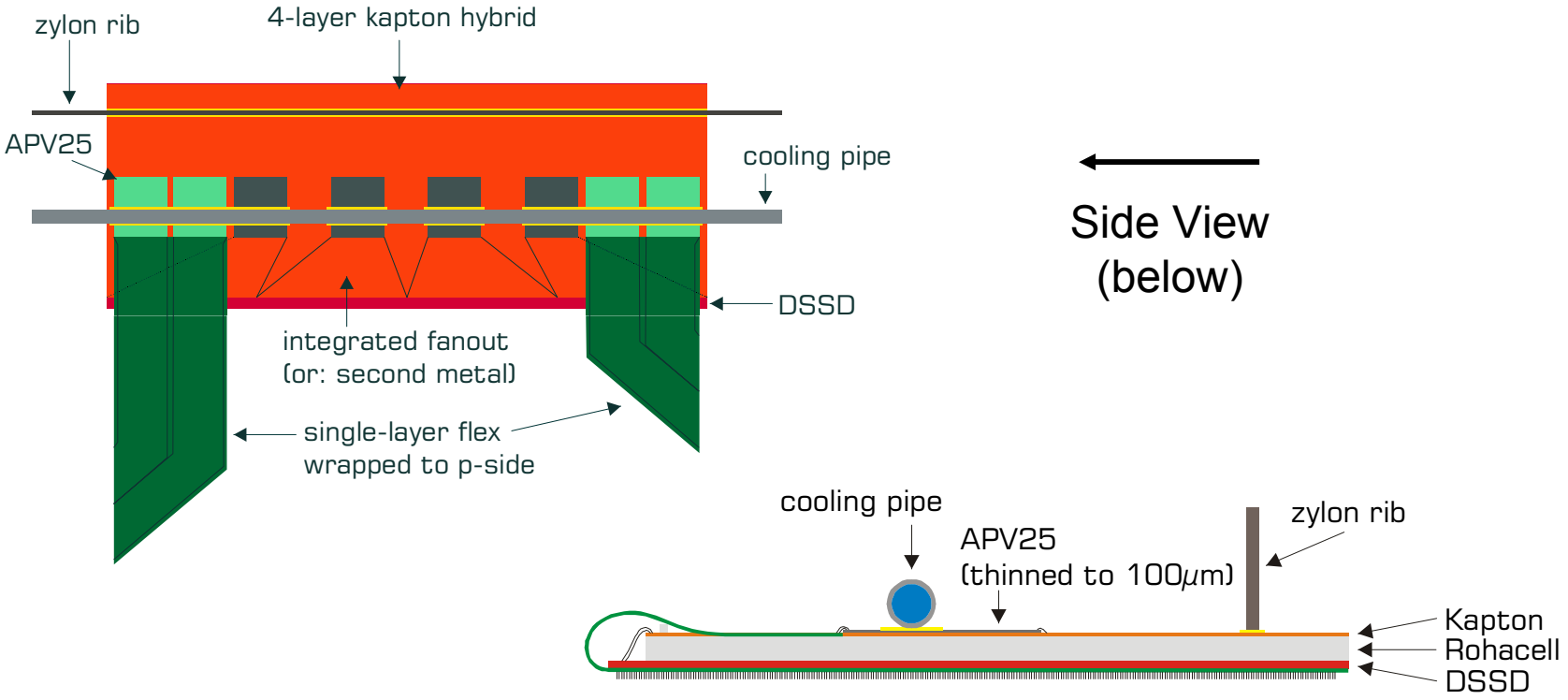
Possible SuperSVD Layout



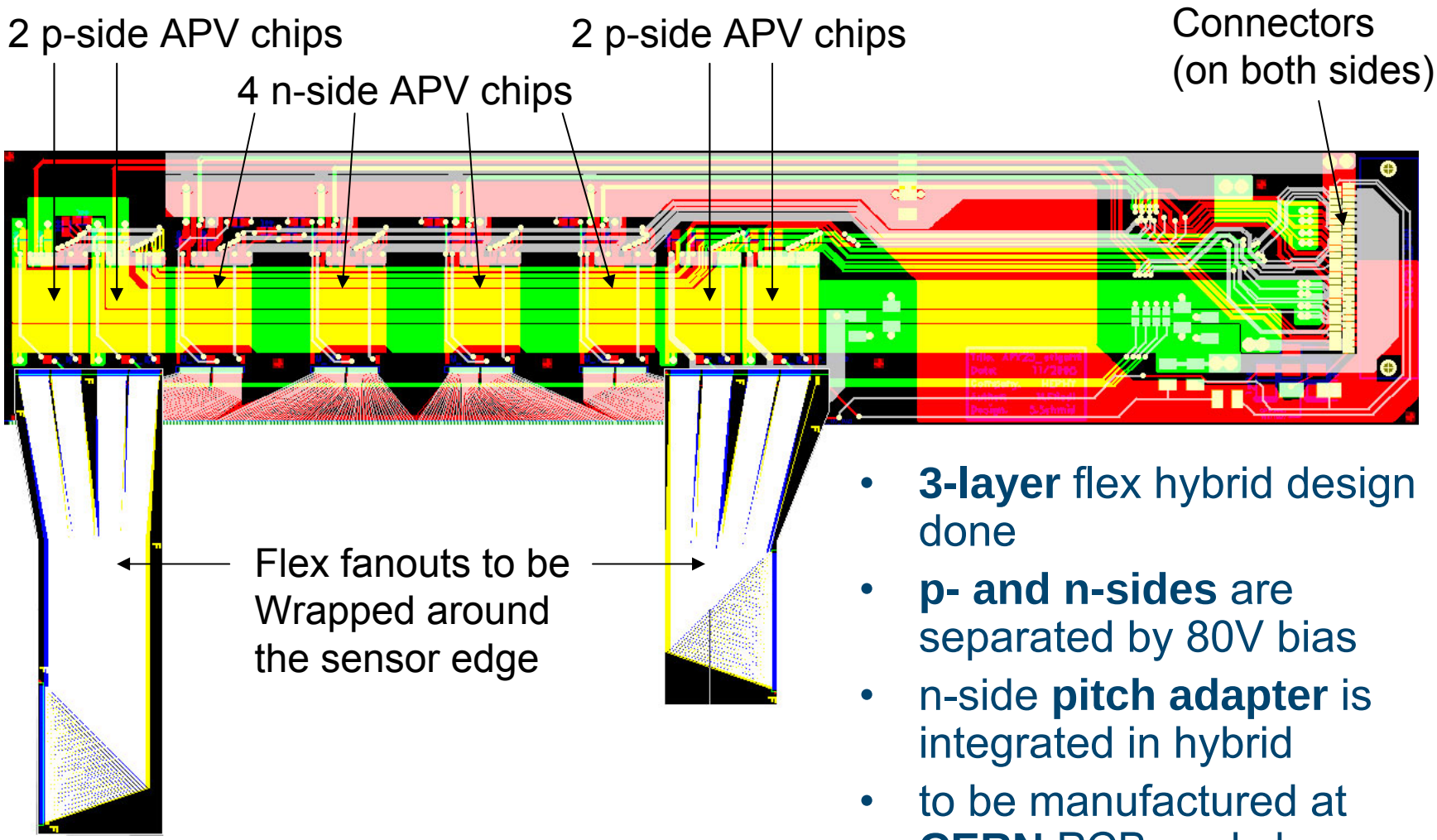
- Using **6“ DSSDs** (~12.5 cm long, up to ~4 cm wide)
- Every sensor is read out individually (**no ganging**)
  - **Edge sensors** (green) are conventionally **read from side**
  - **Center sensors** (red) use **chip-on-sensor concept** (layers 3-5)

Origami Concept

- Extension of **chip-on-sensor** to **double-sided readout**
- **Flex fan-out** pieces **wrapped** to opposite side (hence “Origami“)
- All chips aligned on one side → **single cooling pipe**



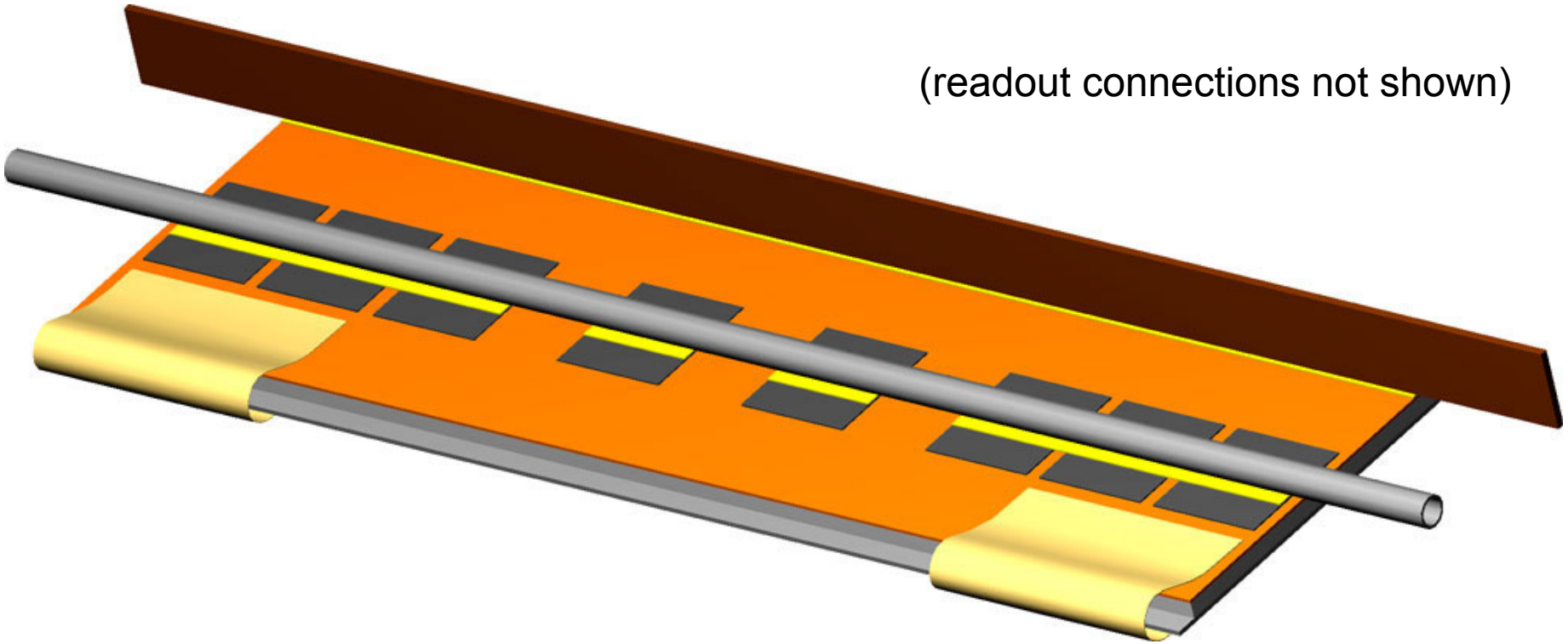
Origami Layout



- **3-layer** flex hybrid design done
- **p- and n-sides** are separated by 80V bias
- n-side **pitch adapter** is integrated in hybrid
- to be manufactured at **CERN** PCB workshop

3D Rendering

(readout connections not shown)



APV25 Purchase

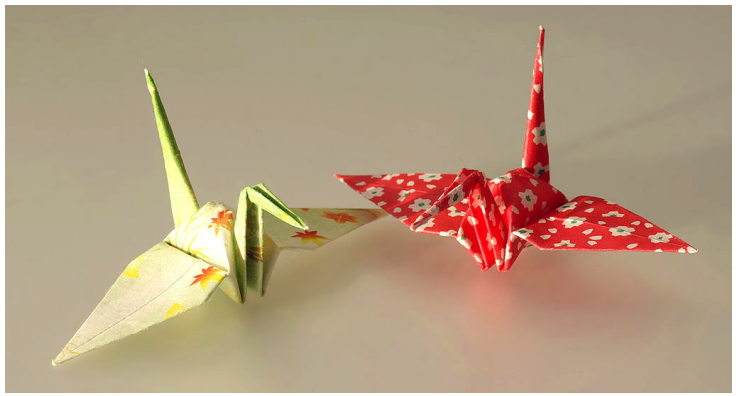
- SuperSVD needs about **2500 normal + 2500 thinned chips** (for chip-on-sensor) including spares
- Enough tested APV25 chips are **in stock @ IC London**
- **Purchase** procedure **of 4000 APV25** chips in JFY 2008 in underway
- 1000 more will be purchased next year (due to administrative limits)
- 1 APV25 costs **28 CHF** (~18 €, ~2150 ¥, ~23 $)
- **Thinning** will be taken care of by HEPHY Vienna
  - Existing chips are ~300µm thick, thinning target ≤ 150µm

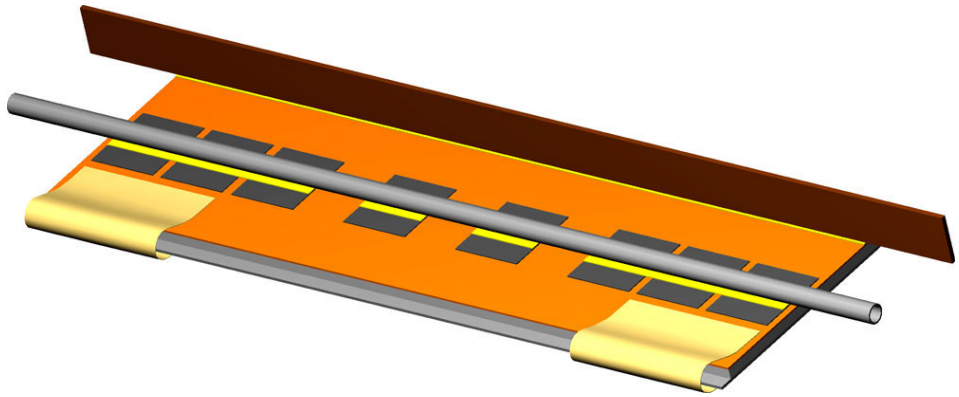
- In parallel, discussion for a readout chip **development by IDEAS** has started for a future upgrade of SuperSVD
  - Based on APV25 design

Summary & Outlook

- **APV25 chip** (developed for CMS) fits for SuperSVD
- **Pipeline length** and **dead time** simulation @ **30kHz Poisson triggers**:
  - **0.87%** @ **42.4MHz** clock, **3.8µs** pipeline
  - **3.43%** @ **31.8MHz** clock, **5.0µs** pipeline
- Trade-off between wishes of **Nakao-san** and **Iwasaki-san**

- **"Origami"** concept for low-mass double-sided readout with cooling
- We will assemble such a module in the near future





BACKUP SLIDES

Comparison VA1TA – APV25

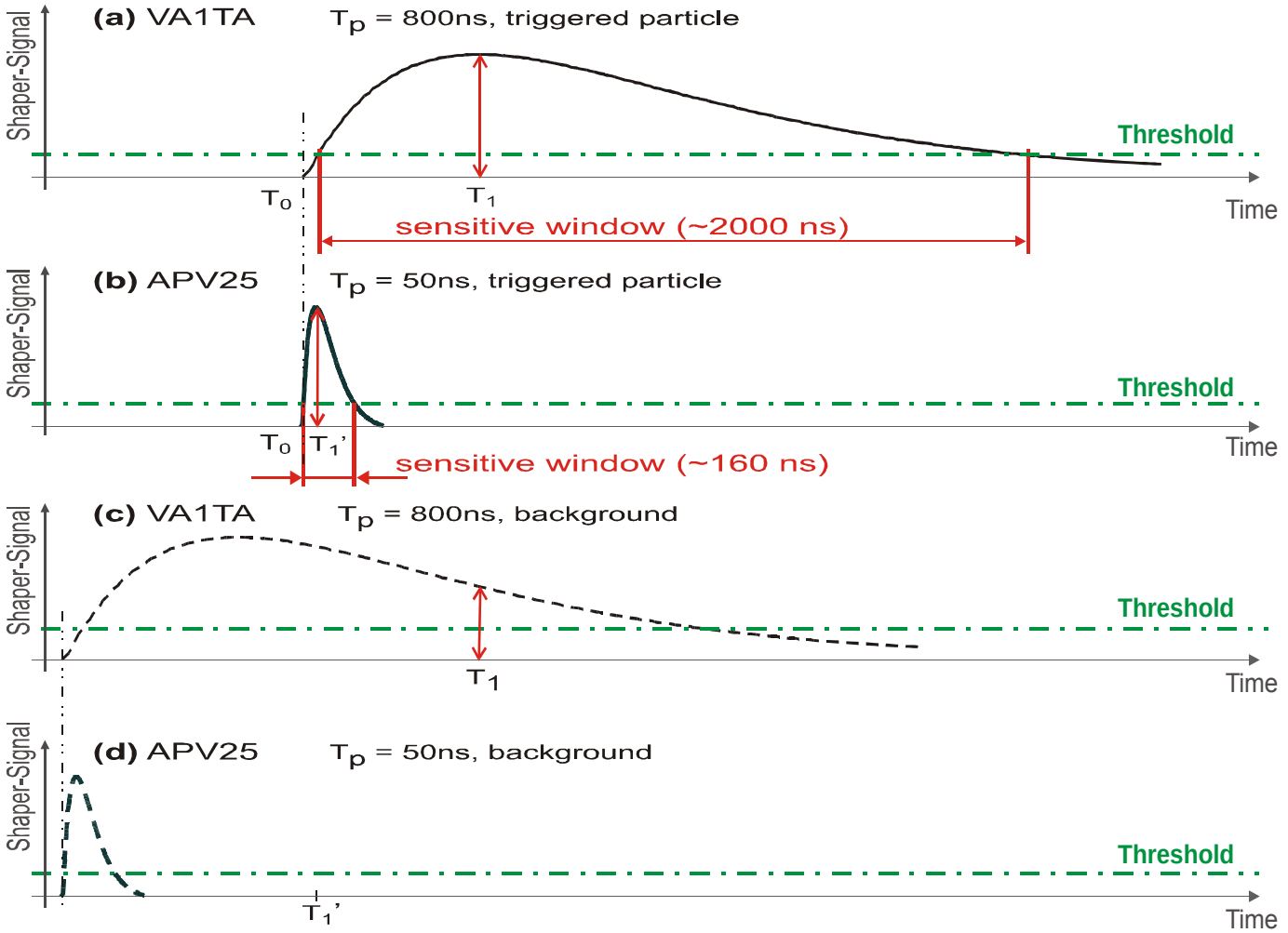
VA1TA (SVD2)

- Commercial product (IDEAS)
- Tp = 800ns (300 ns – 1000 ns)
- no pipeline
- <10 MHz readout
- 20 Mrad radiation tolerance
- noise: ENC = 180 e + 7.5 e/pF
- time over threshold: ~2000 ns
- single sample per trigger

APV25 (SuperSVD)

- Developed for CMS by IC London and RAL
- Tp = 50 ns (30 ns – 200 ns)
- 192 cells analog pipeline
- 40 MHz readout
- >100 Mrad radiation tolerance
- noise: ENC = 250 e + 36 e/pF
- time over threshold: ~160 ns
- multiple samples per trigger possible (Multi-Peak-Mode)

Shaping Time and Occupancy

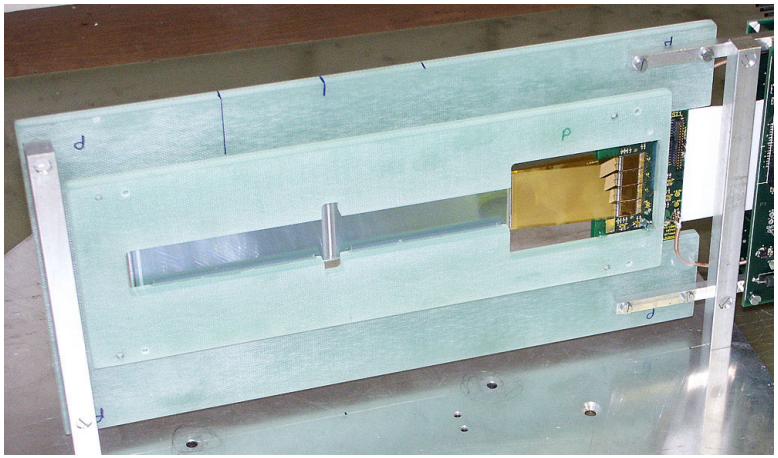


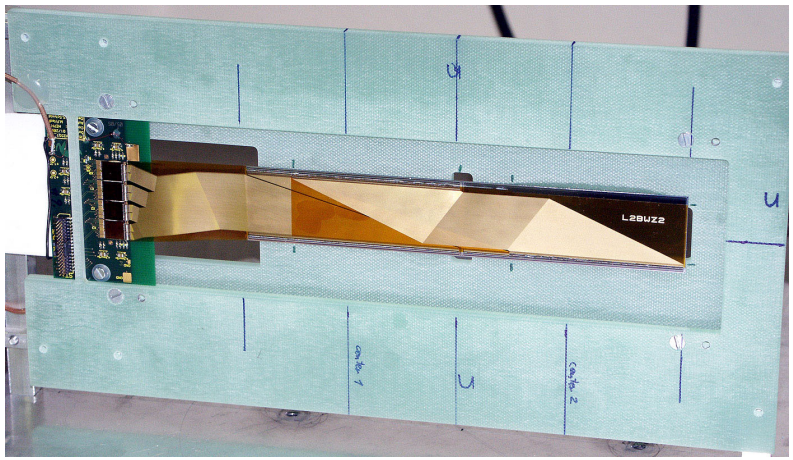
BEAM PARTICLE

OFF-TIME BACKGROUND PARTICLE

Ganged Sensors Read Out with APV25

- Prototype module with 2 **partially ganged DSSDs**





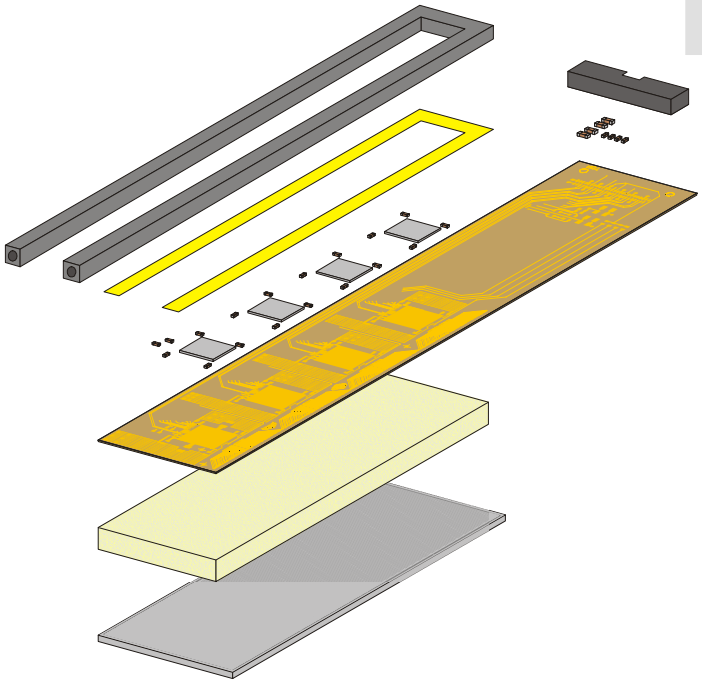
- Beam test result shows that already **ganging of 2 sensors is problematic**

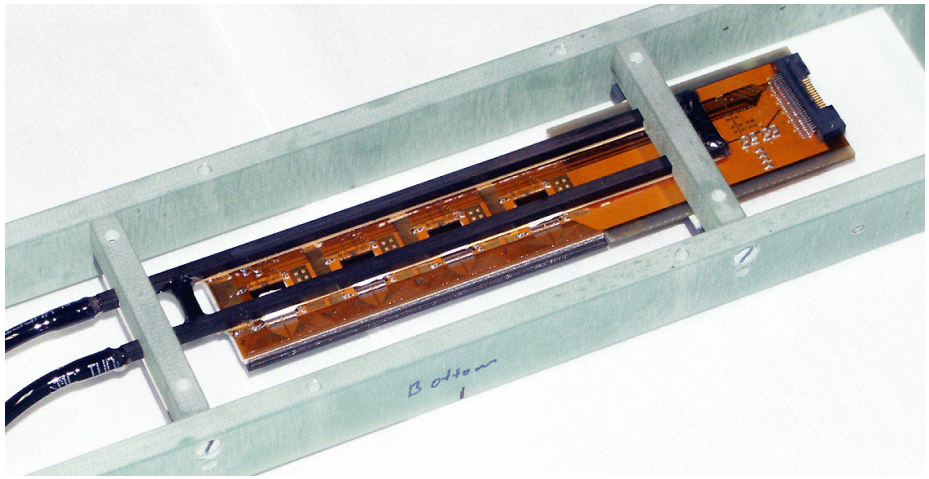
	ganged		single	
	p-side	n-side	p-side	n-side
Cluster SNR	9.4	10.1	13.1	13.9
Single Strip SNR	13.5	13.4	19.9	18.9

Flex_Module Measurement Results

- Beam test result shows that **chip-on-sensor** (n-side) delivers excellent SNR

	Flex_Module		Conventional (single sensor)	
	p-side	n-side	p-side	n-side
Cluster SNR	13.8	**18.4**	13.1	13.9
Single Strip SNR	20.9	**25.4**	19.9	18.9





Origami Material Budget

- X_0 comparison between conventional and chip-on-sensor:

Conventional (double layer kapton)

Layer	Material	X0 [mm]	Thickness [mm]	Percentage	Area coverage	Averaged Percentage
Sensor	Silicon	93.7	0.3	0.32%	100.0%	0.320%
Fanout	Polyimide (2 layer of 50um each)	300.0	0.1	0.03%	96.3%	0.032%
	Copper (10um)	14.0	0.01	0.07%	50.0%	0.036%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	50.0%	0.005%
	Gold (top: 0.8um)	3.4	0.0008	0.02%	50.0%	0.012%
Ribs	Zylon (0.5mm wide)	300.0	5	1.67%	3.7%	0.062%
Glue	Araldite 2011 / Double sided tape	335.0	0.05	0.01%	96.3%	0.014%
				Total		**0.480%**

DSSD Chip-on-Sensor (4-layer kapton)

Layer	Material	X0 [mm]	Thickness [mm]	Percentage	Area coverage	Averaged Percentage
Sensor	Silicon	93.7	0.3	0.32%	100.0%	0.320%
Isolation	Rohacell (Degussa)	5450.0	1	0.02%	96.3%	0.018%
Hybrid	Polyimide (4 layers of 50um each)	300.0	0.2	0.07%	96.3%	0.064%
	Copper (4 layers of 5um each)	14.0	0.02	0.14%	64.7%	0.092%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	64.7%	0.006%
	Flash Gold (top: 0.4um)	3.4	0.0004	0.01%	64.7%	0.008%
Flexes	Polyimide (1 layer of 25um)	300.0	0.025	0.01%	56.3%	0.005%
	Copper (1 layer of 5um)	14.0	0.005	0.04%	28.1%	0.010%
	Nickel (top: 1.3um)	14.3	0.0013	0.01%	28.1%	0.003%
	Flash Gold (top: 0.4um)	3.4	0.0004	0.01%	28.1%	0.003%
8 * APV25	Silicon	93.7	0.1	0.11%	21.4%	0.023%
SMDs	SMD	50.0	0.4	0.80%	0.8%	0.007%
Sil-Pad	Sil-Pad 800 (Bergquist)	200.0	0.127	0.06%	11%	0.007%
Pipe	Aluminum (D=2.0mm, wall=0.2mm)	89.0	0.56	0.63%	7%	0.047%
Rib	Zylon (0.5mm wide)	300.0	5	1.67%	1.9%	0.031%
Glue	Araldite 2011	335.0	0.2	0.06%	50%	0.030%
Cooling	Water	360.5	1.26	0.35%	13%	0.047%
				Total		**0.719%**

- **+50%** increase in **material**, but also **huge** improvement in **SNR**
- **Trade-off** between material budget and SNR
- According to simulation, additional material is prohibitive in 2 innermost layers, but **no problem for layers 3-5** → OK with layout