# FADC+Proc. to find time and position of a hit

M.Pernicka Vienna

***I would like to raise several issues:***

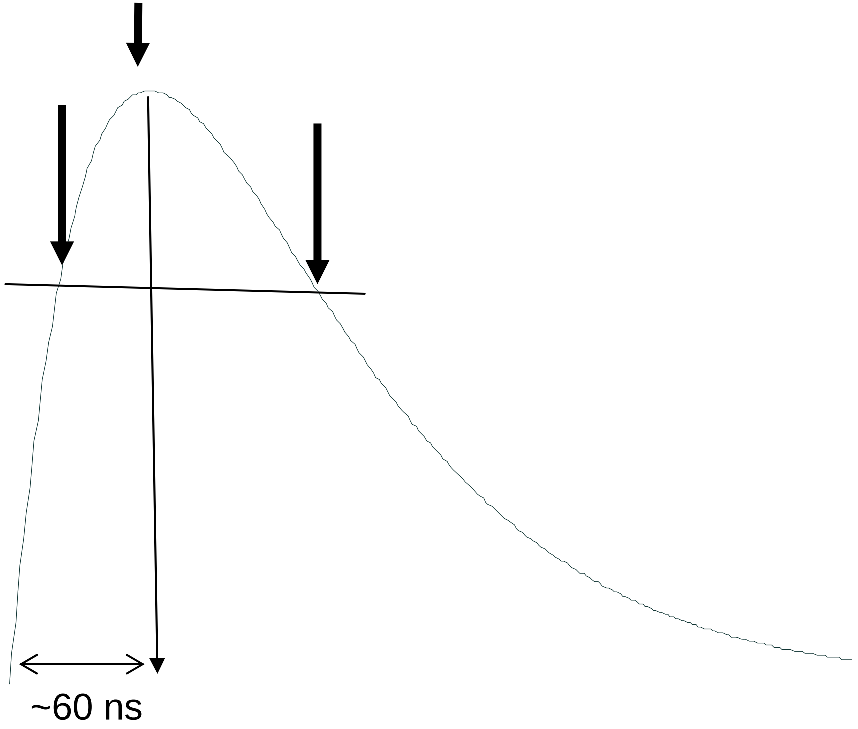
***Why we want use more than one pulse height sample of the shaped signal. The APV25 offers this possibility.***

- ***What is the production status of the FADC+proc. System.***
- ***The analogue part till the ADC.***
- ***The 2 links between FADC und Copper system.***
- ***The different data formats of the data block and what is planned for the hit time data block.***
- ***The plans for the hit-time processor.***
- ***Different error / control systems***

**The point of storing a signal has a certain jitter.**

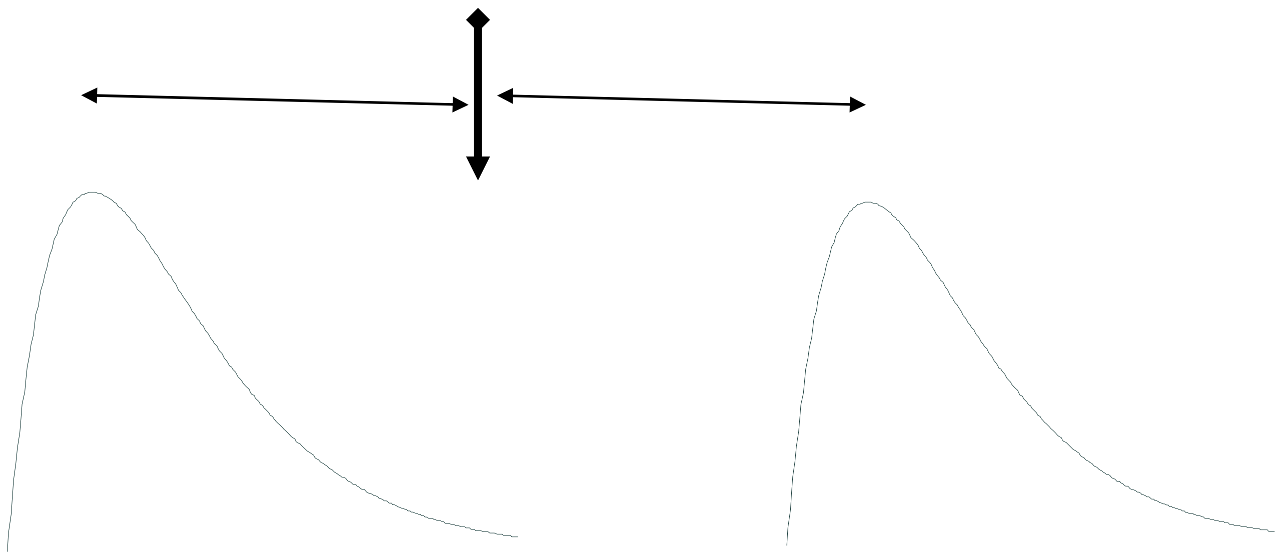
**APV25** **The Trigger is synchronised with the clock for the ( for a LHC experiment no problem)**
**The trigger itself has a time jitter**

**Therefore 3 samples around the maximum would be a great advantage ( or necessary ) The APV25 has this facility.**



The trigger can have a jitter more than the shaping time and the occupancy is still too big.

To increase the shaping time would be the wrong solution! Therefore we will measure the time of each signal to the trigger and each other! We use the 3 highest samples to calculate the time. An RMS of 2 ns was obtained (with high S/N) in various beam tests.



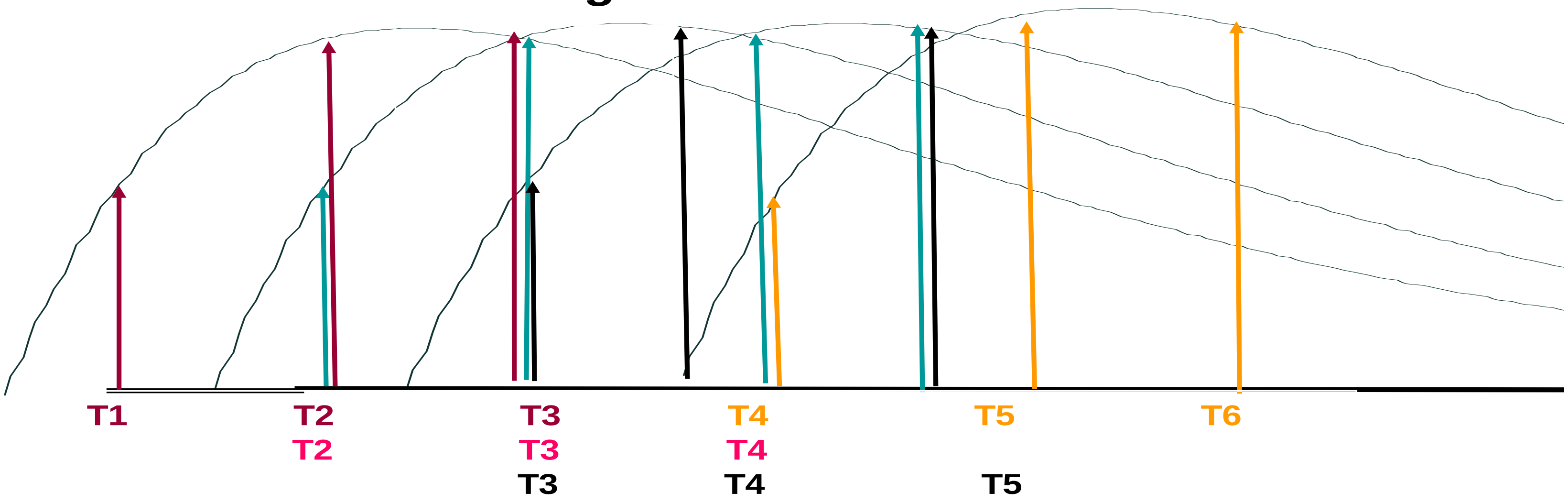
**We have to live with jitter and latency of the trigger, we have to optimise the shaping time and clock frequency (and number samples) 6 samples are foreseen … max +/-50 ns trigger jitter can be handled.**

**With 3 time samples the time range 25 ns. In reality, the time range must be bigger than 25 ns. The reason is the jitter of the trigger, noise of the signal and .... There fore we need 6 time samples (1,3,6,(9))**

**From 6 time samples we select those 3 neighbours where the middle one is a maximum or equal to a neighbour. Result coarse time 0,25,50,75 .**

**Lookup table only for a range of 25 ns. The first 25 ns starts with T1<T2 and ends with T2=T3 (T3>T5). The next 25 ns begins with (T1<T2) T2<T3 and ends with (t2<T3) T3=T4 (T4>T5) ...(T3<T4), T4<T5, T5>T6**

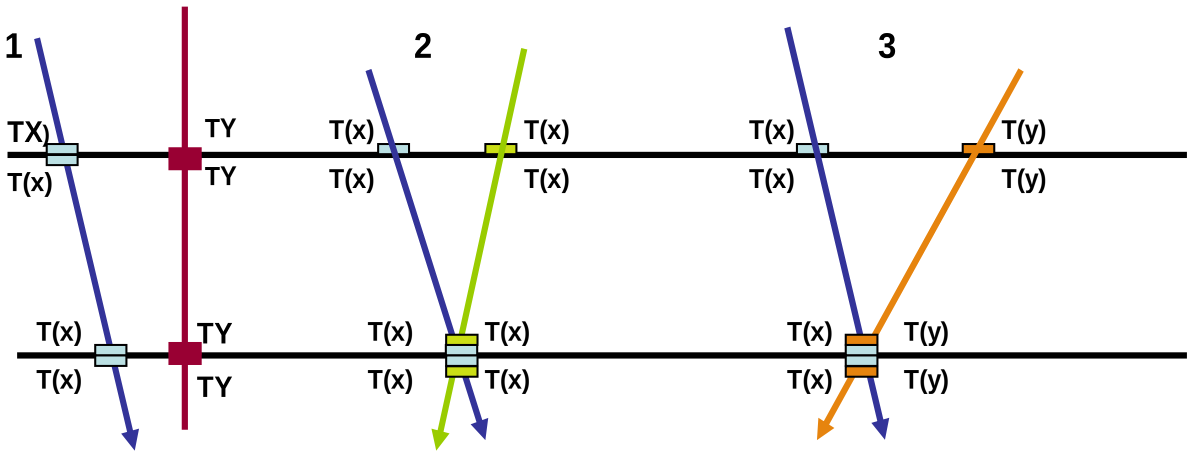
***there fore max time range 100ns!***



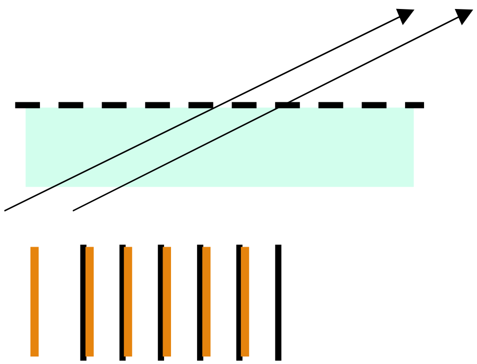

With 6 time sample we can calculate the time in a range of 4 clock width

# *To select hits which belong to the trigger*

Case:




**Problem: cluster with 2 tracks with different times or not?**



The amount of data would be for every input n*140 data ( n=1,3,6,..)

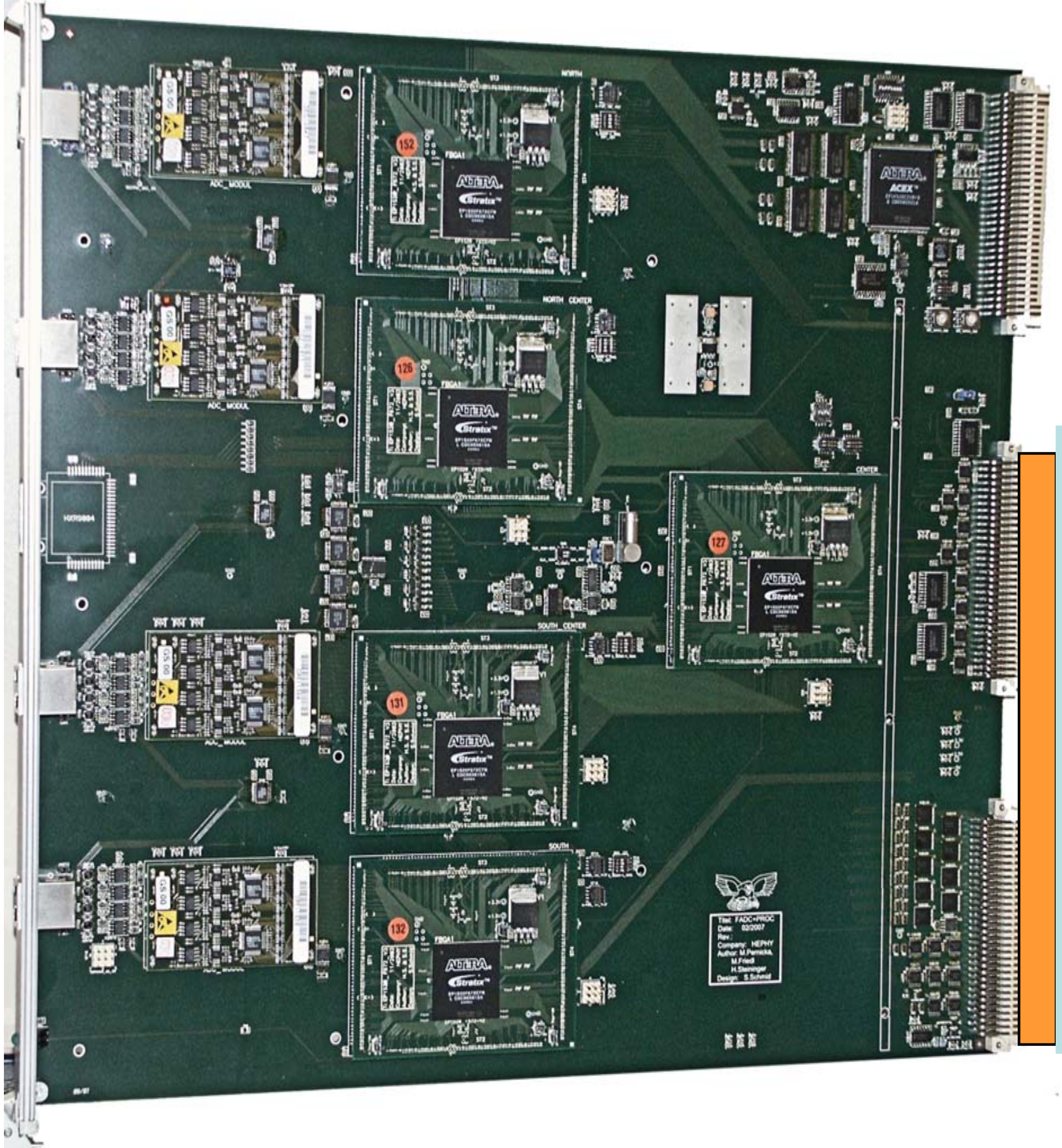
The answer was an FADC + processor module with 16 inputs and with a data processor for every input for position and time calculation. Every processing is a part of a pipeline. The limit of the trigger rate depends on the final design and could be as high as the trigger rate for the APV25.

The ``mother´´ of this module is the readout module for the CMS pixel detector with 36 optical inputs.

2 other versions are used for the CMS beam conditions monitor system.

# *2 BELLE_FADC+proc. module are ready*

***(without the facility of time calculation)***



**Mezzanine board**

From every Altera 9 transmission lines to P2

**Data bus**

**Control bus temporary**

# Some remarks on the task of the APV-FADC-Processor system

*Main aims:*

You need output data of the ADC ( transparent mode ), to calculate ADC clock delay to the main clock, pedestal and threshold. An external gate signal is used as write signal of the ADC data in the memory and create on the control module a trigger and cal signal to the APVs Done by the VME system crate processor.

To get the hit information after reorder and 2-pass common mode correction.

To build for every hit 6 time samples. That means 6 times more data for one hit. The hit-time calculator reduces it to one. (Not included yet.)

(To include neighbours in space above pedestal and under threshold. Again more data.)

To get for every hit data the time. We will use the 3 time information from 6 time samples around the max. to find the time of the hit. (Neighbours in space can be included). In an unclear situation like 2 max are found, no max is found because max outside of the 6 time samples or shaping curve do not fit in the expected one, the full information, that means 6 time blocks are transmitted for further processing. That would increase the data amount but without any loss of information.

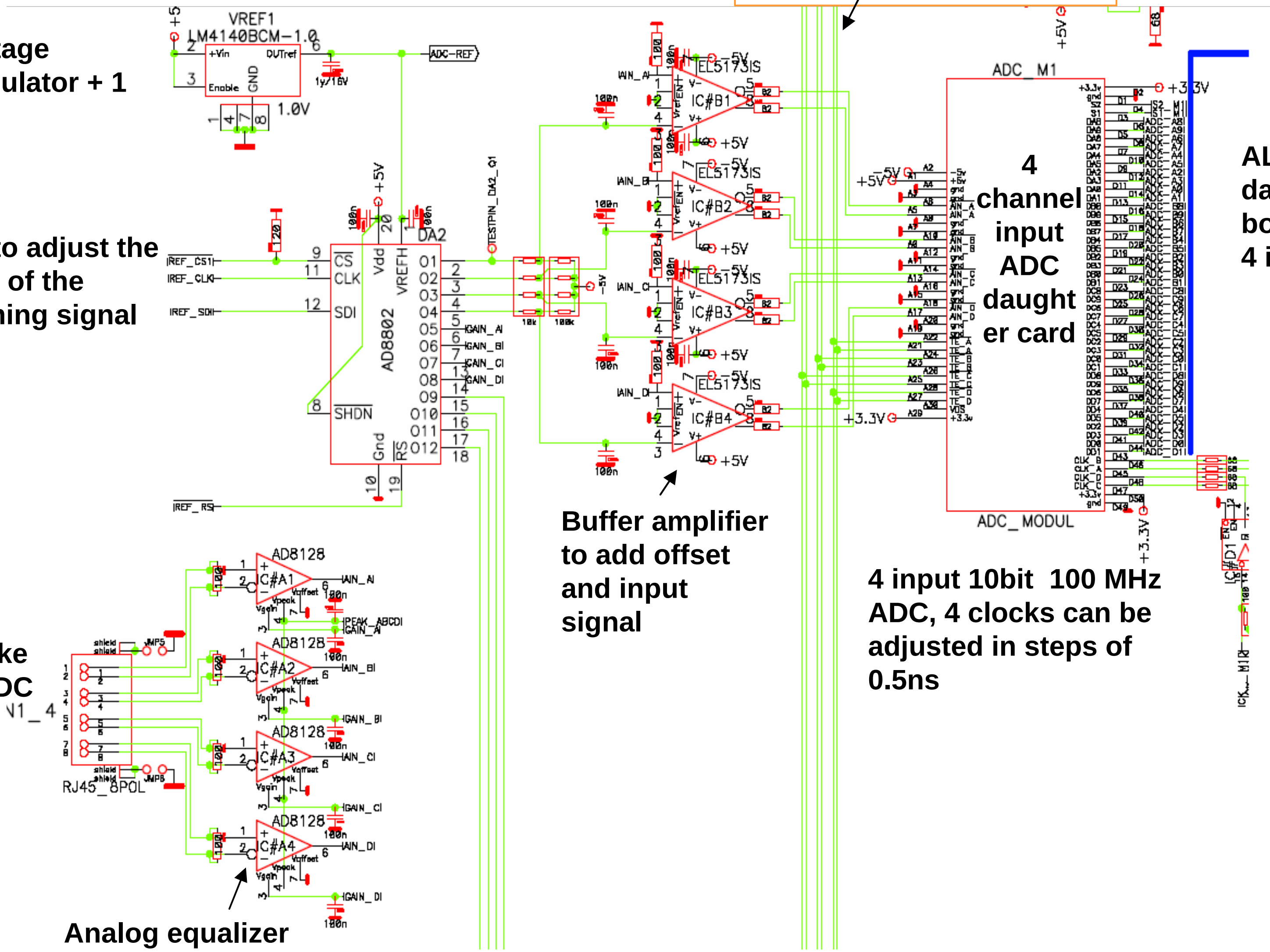


**A lot of test facilities for testing the different data processors are fore seen.**

Test pulse generator,
3 channel DAC, can create hit data

Voltage Regulator + 1 V

DAC to adjust the offset of the incoming signal




4 channel input ADC daughter card

ALTERA daughter board for 4 inputs

Buffer amplifier to add offset and input signal

4 input 10bit 100 MHz ADC, 4 clocks can be adjusted in steps of 0.5ns

4 inputs like SVD-2 FADC RJ 45

Analog equalizer (parameter: length of cable)
gain adjustment

# *The use of bit 31 – 0 for the different data types*

* With or with out neighbours

***decided by VME command***

**OR** **OR***

| Main header always | Input header yes/no | Transparent data need strobe | Hit date | Hit + transp. Date, test | **Hit + time date** | **Inp Trailer yes/no** | **Main Trailer always** |
|---|---|---|---|---|---|---|---|
| 31 type header = 0<br>30-27 trigger type/4 ???<br>25-23 type of data / 3 | 31typ of header =1<br>29-23 event number from input. | 31-23 Transpar. Data after reorder need a window sig | 31-23=0 transparent data belong to the hit | 31-23 transp data ADC, some times or cont. date 0 | 31=1<br>30-27 quality of data, type<br>26-23 Time of hit | 31=type of trailer =1 | 16-31<br>CRC<br>check sum |
| 20-16 time of clock/ trig include later Alt-C | 0<br>19-16 input = 4 | 7<br>19-16 input = 4 | 22-20 time block 1bis6<br>19-16 input = 4 | 22-20 time block 1bis6<br>19-16 input = 4 | 22-20 time max 1 bis5<br>19-16 input = 4 | | |
| 14,15 crate ?<br>13-9 module n<br>Alt-C | 15-9 Ped Correction-2<br>7 | | 15-9 position<br>7 | 15-9 position<br>7 | 15-9 position<br>7 | may be input error bits | may be module error bits ? |
| 7-0 Event number, from Copper syst. / | 8-0 Ped Correction-1 | 8 – 0 Transparent data | 8-0 Pulse height data | 8-0 Pulse height data | 8-0 Pulse height data | | |

**Fin es se**

*

M. Pernicka Vienna

The final aim

# *The use of bit 31 – 0 for the different data types*

| Main header always | Main header always, for one module information |
|---|---|
| 31 type header = 0<br>30-27 trigger type/4<br>25-23 type of data | Module input header<br>**?**<br>**?** |
| 20-16 time of clock/ trig include later Alt-C | Time between trigger and clock bus-data |
| 14,15 crate ?<br>13-9 module n<br>Alt-C | Has to be included by VME |
| 7-0 Event number, from Copper syst. | Bus- signal from controller |

| Input header yes/no | Every input has its header, can be switched off by VME |
|---|---|
| 31typ of header =1 | Input header |
| 29-23 event number from input. | Input number counting the arriving header APV25 |
| 0 | Code N U |
| 19-16 input = 4 | 16 inputs on module exists |
| 15-9 Ped Correction-2 7 | Correction for the second common mode correction, can be + or - |
| 8-0 Ped Correction-1 | Correction factor for the first common mode correction, can be + or - |

| Transparent data need strobe | Need a trigger signal from the controller (Neco) and a strobe signal (bus) to collect APV25 data. Will be used by VME system |
|---|---|
| 31-23 Transpar. Data after reorder need a window sig | Transparent data from input n after reorder. Input number+1 |
| 7 | Code NU |
| 19-16 input = 4 | Input |
| 8 – 0 Transparent data | Transparent data from input one |

| Hit date | From a single hit position and time block information |
|---|---|
| 31-23=0 transparent data belong to the hit | Transparent data which belong to the hit, still not included |
| 22-20 time block 1bis6 | Number of the time block, at the moment 6 |
| 19-16 input = 4 | |
| 15-9 position 7 | An APV25 has 128 signal outputs |
| 8-0 Pulse height data | Each signal above a threshold in o0ne of the 6 time blocks |

Hit + transp. Date, test

31-23 transp data ADC, some times or cont. date 0

22-20 time block 1bis6

19-16 input = 4

15-9 position 7

8-0 Pulse height data

The hit data are read out by finesse and spy memory, (VME) and the transparent data from one input and one time block with reduced frequency 1/256 under control from VME

At the moment 6

Standard hit information

**Hit + time date**

31=1
30-27 quality of data, type

26-23 Time of hit

19-16 input = 4

15-9 position 7

8-0 Pulse height data

The final data for a hit with position and time

Still open

Time of the hit to the leading edge of clock

Standard hit information

| | |
|---|---|
| **Main Trailer always** | The end of a data block of the 16 oinputs |
| 16-31 | |
| CRC | CRC16 (Cyclic Redundancy Check) |
| check sum | |
| may be module error bits ? | The kind and use of `` errors ``are still open |

# *The use of the bit 68-64 bits on FADC board bus system and for the data link to FINESSE*

| | | Main header always | Input header Yes/no | Data | Dummy | Input Trailer | Main trailer |
|---|---|---|---|---|---|---|---|
| Head | 67 | 1 | 1 | 0 | 1 | 0 | 0 |
| Trailer | 66 | 0 | 0 | 0 | 1 | 1 | 1 |
| Stop | 65 | 0 | | stop-bit | 0 | 0 | **0** |
| Da En | 64 | 1 | 1 / 0 | 1 | 0 / 1 | 0 | **1** |

**Control bits for finesse**

**On connector**

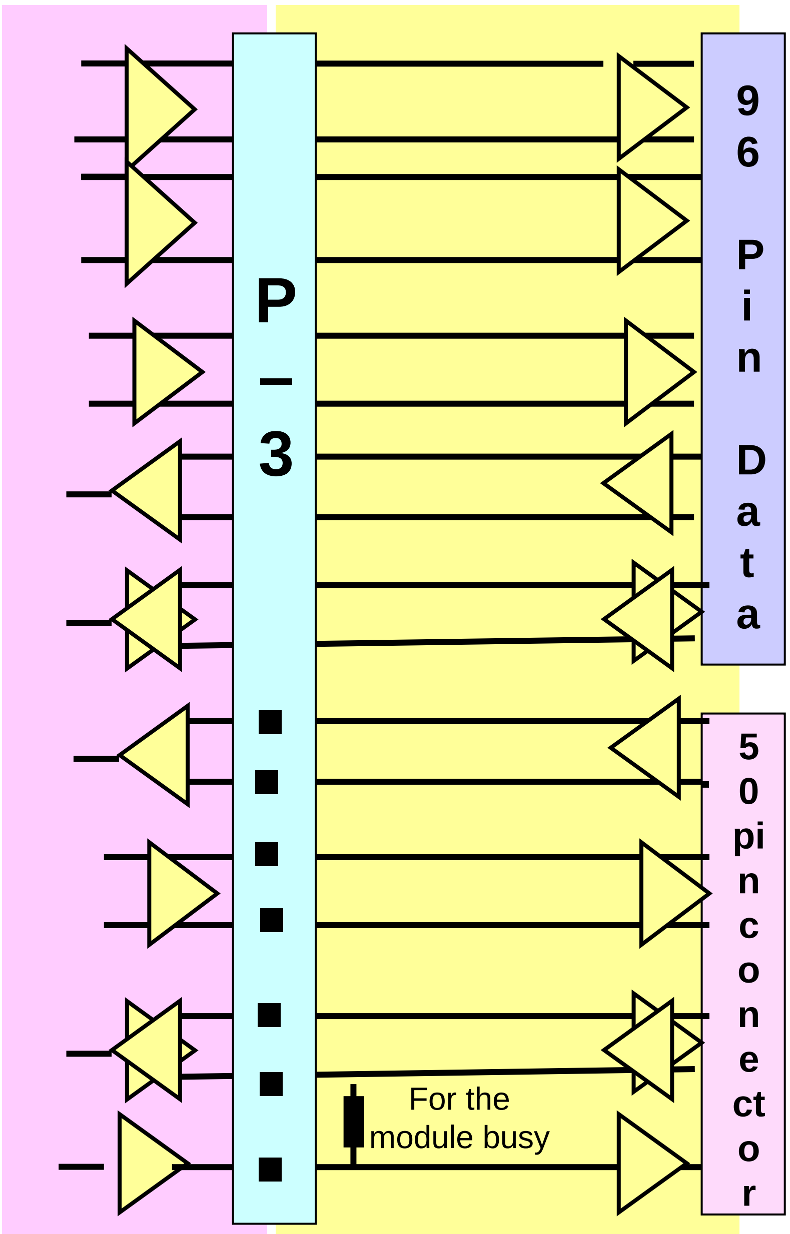
**HEADER 37/85**

**TRAILER 39/87**

**HALF_EV 38/86**

**DA_EN 36/84**

# Mezzanine board for BELLE FADC+proc




32 Data bus XD_0=bis XD_31

4 control lines DA_EN, HALF_EV, TRAILER.HEADER

DCLK  clock 40 MHz

BSYFD  busy Finesse

2 spares

DC/DC
+ 5 V/ -5 Volt

ADCRST;TRG; SCK, TAG0-7, TYP0, / TYP1-3 will be included in new version

ADCBSY (BUSY), ADC_ERR (ERROR1_CON), SPARE1_WR_CON (or data)

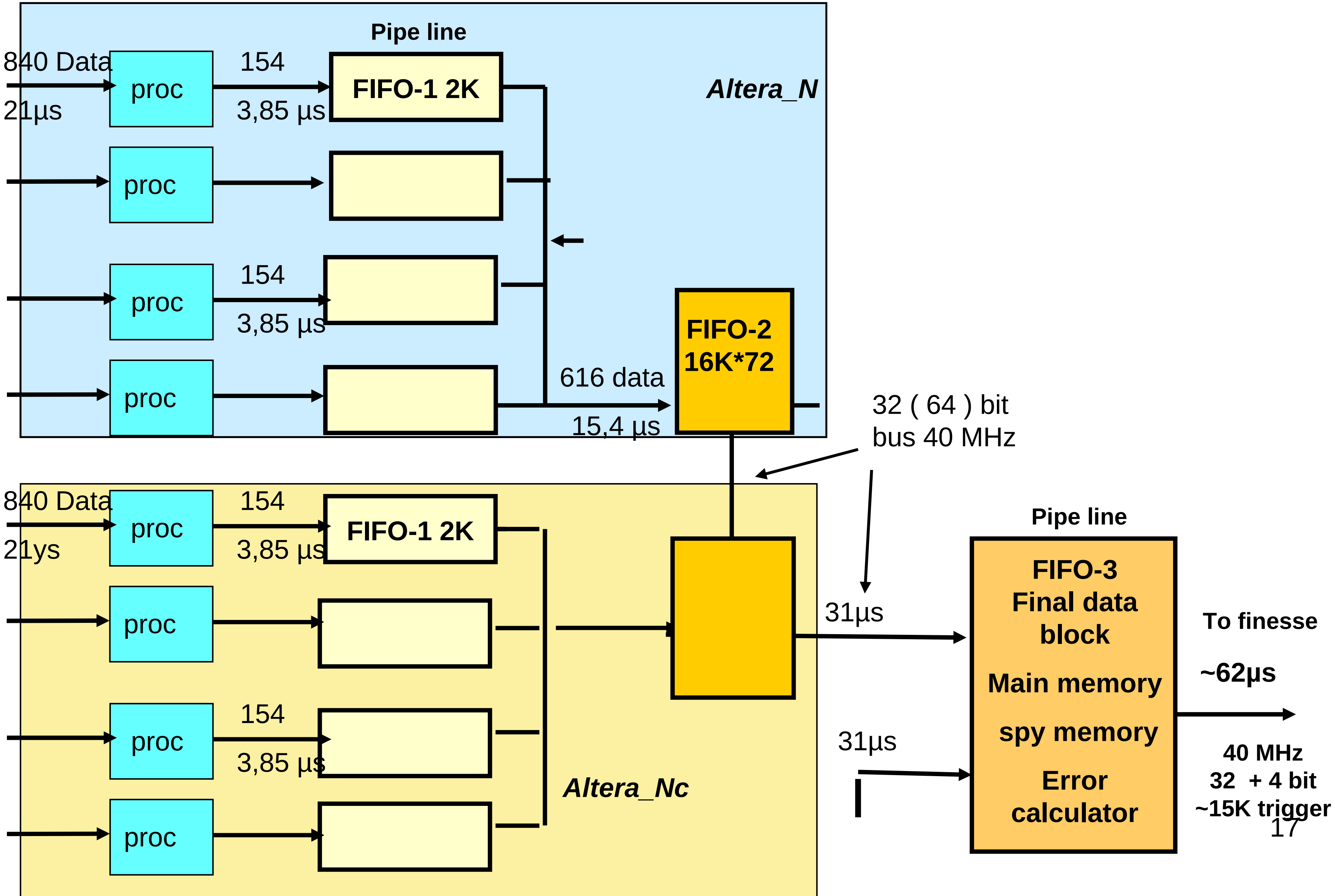
2 spares

ADCBSY (BUSY_COM )

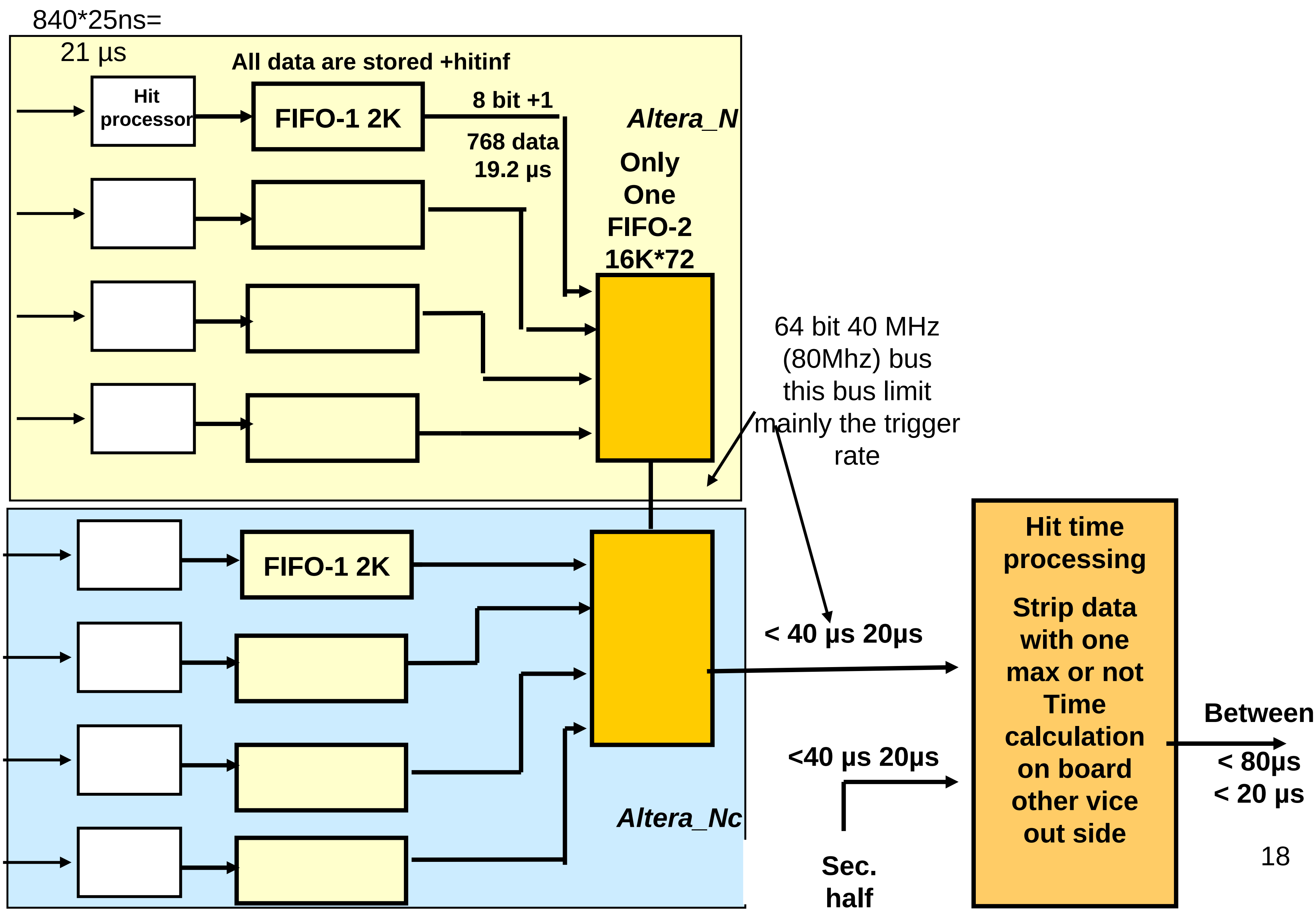
All TW control lines are also bus lines later. At the begin a connector with 50 pins is used for the distribution of the control signals, now we use the P3 bus. .

# The 3 steps of FIFO's for normal 6 time one hit information read out

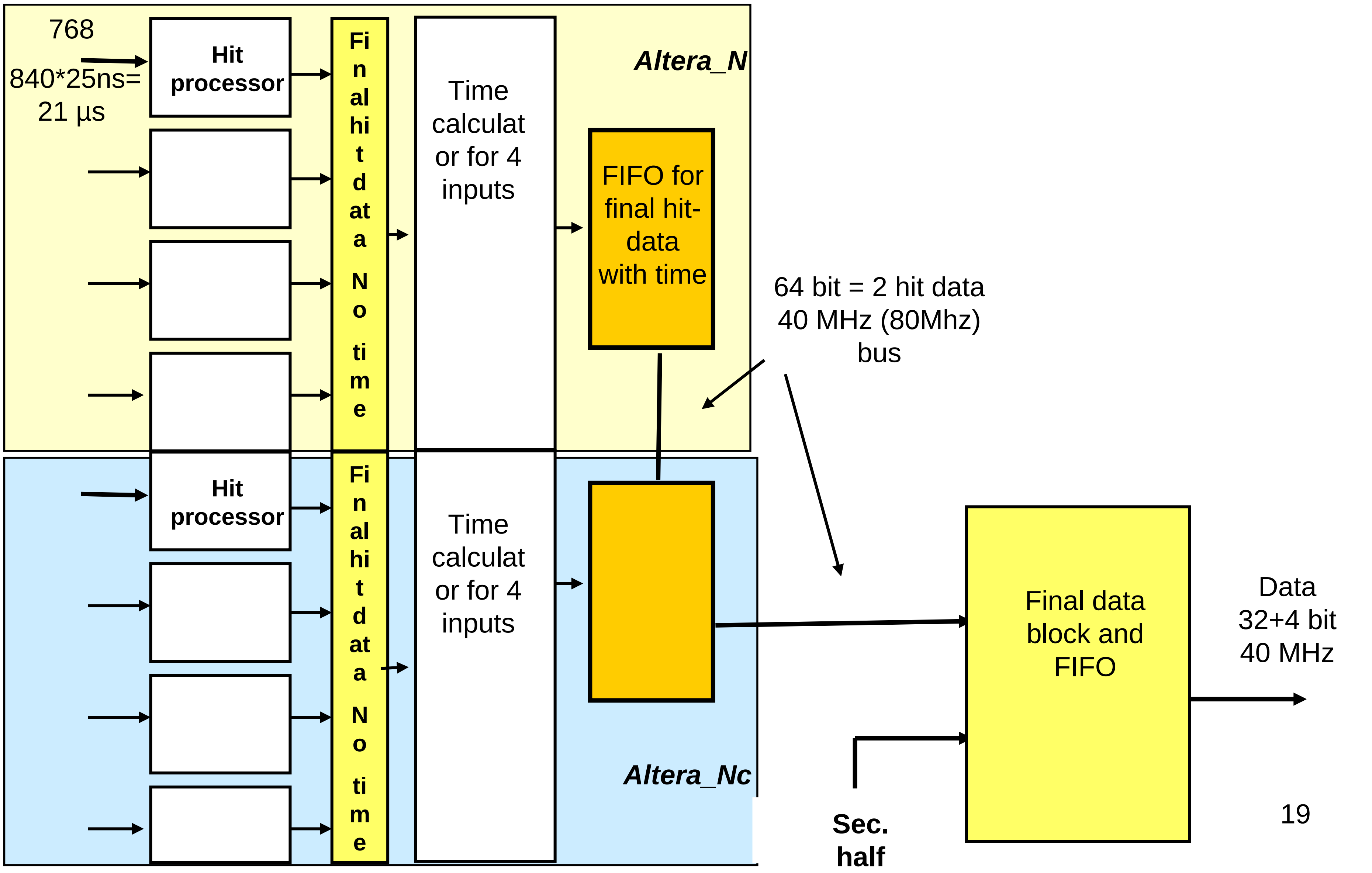
**time calculation for 16 inputs at 20 % occupancy**



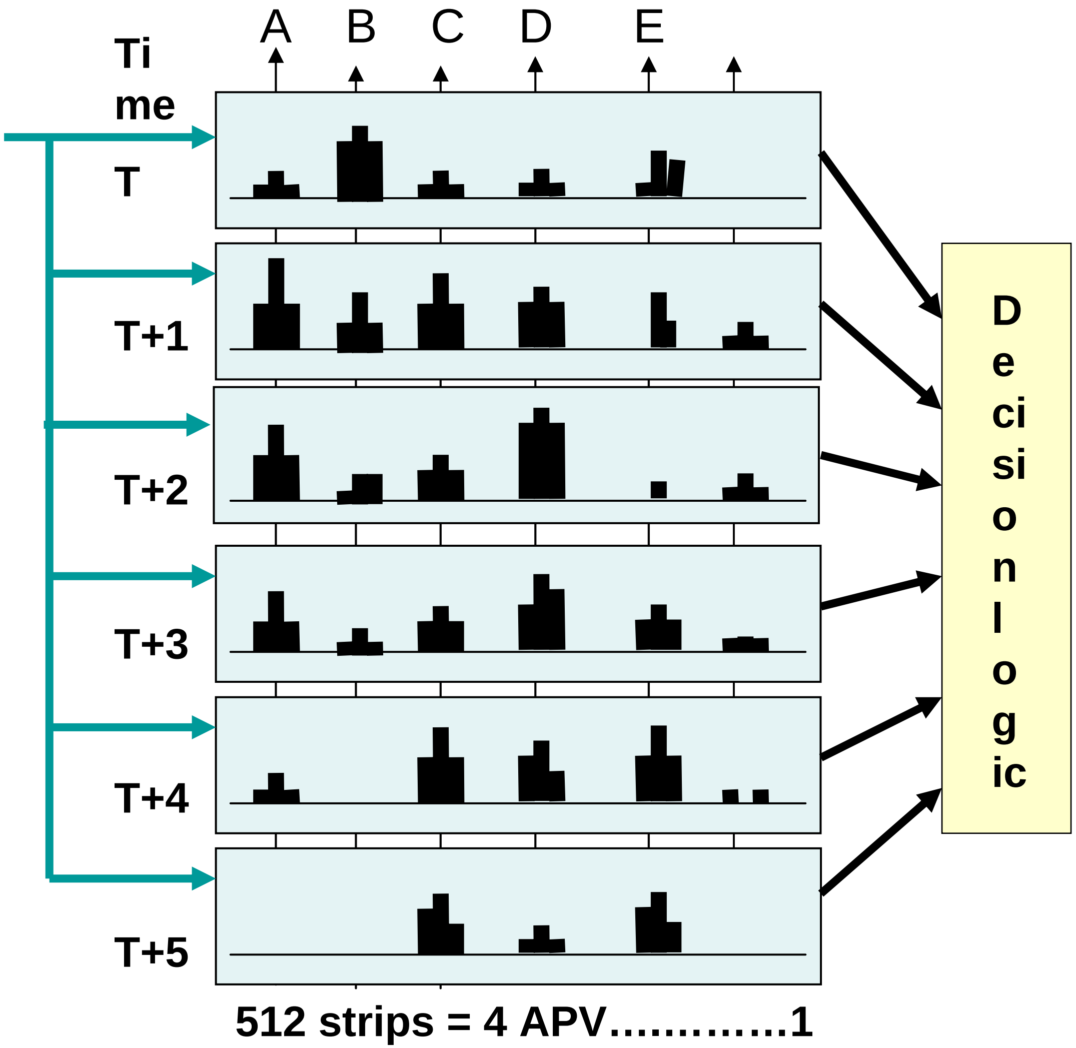
# The 3 steps of FIFO's for hit with time information read out



# The 3 steps of FIFO's for hit with time information read out



# Type of events

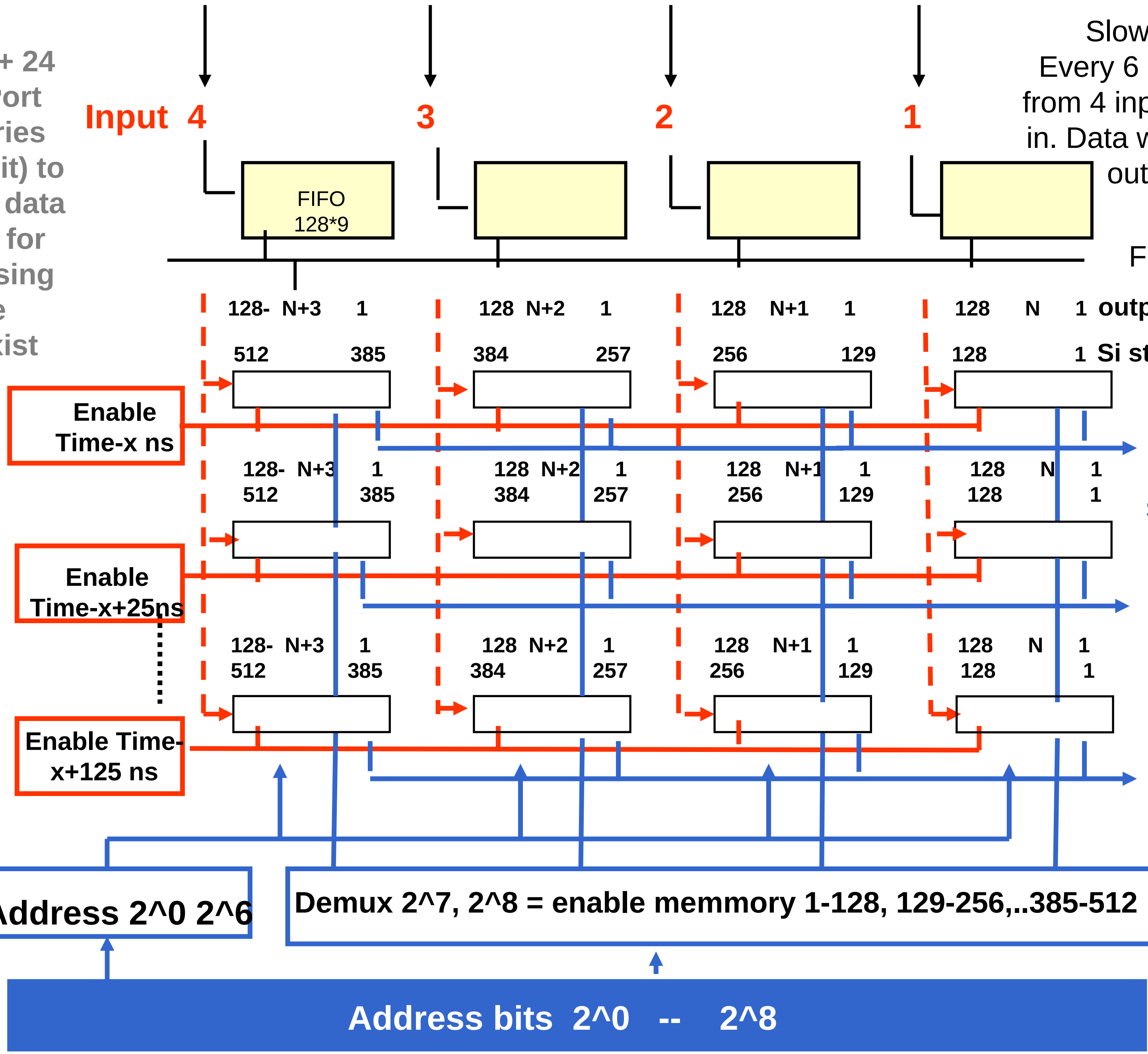



A strip cluster

- A, A single hit, time calculated by `` Look up table ´´ or …
- B, Max high of shaped pulse at the boundary above a certain value, will be used when necessary, time window 150 ns, but without time information or may be value 0 and 150 ns and marker bit.
- C, 2 max. time information's are found, between a smaller sample, the time has to be found outside, may be together with CSC det. data. Marker bit included.
- D Only one max. time info but the pulse shape do not fit in the expected shaping curve. Detected I in the `` Look up table´´. Final calculation out side.
- E 2 real max – 2 times – but can only handled outside
- F, small pulses, inside, hit pulse high information but time critical, marked

Look up table decide outside

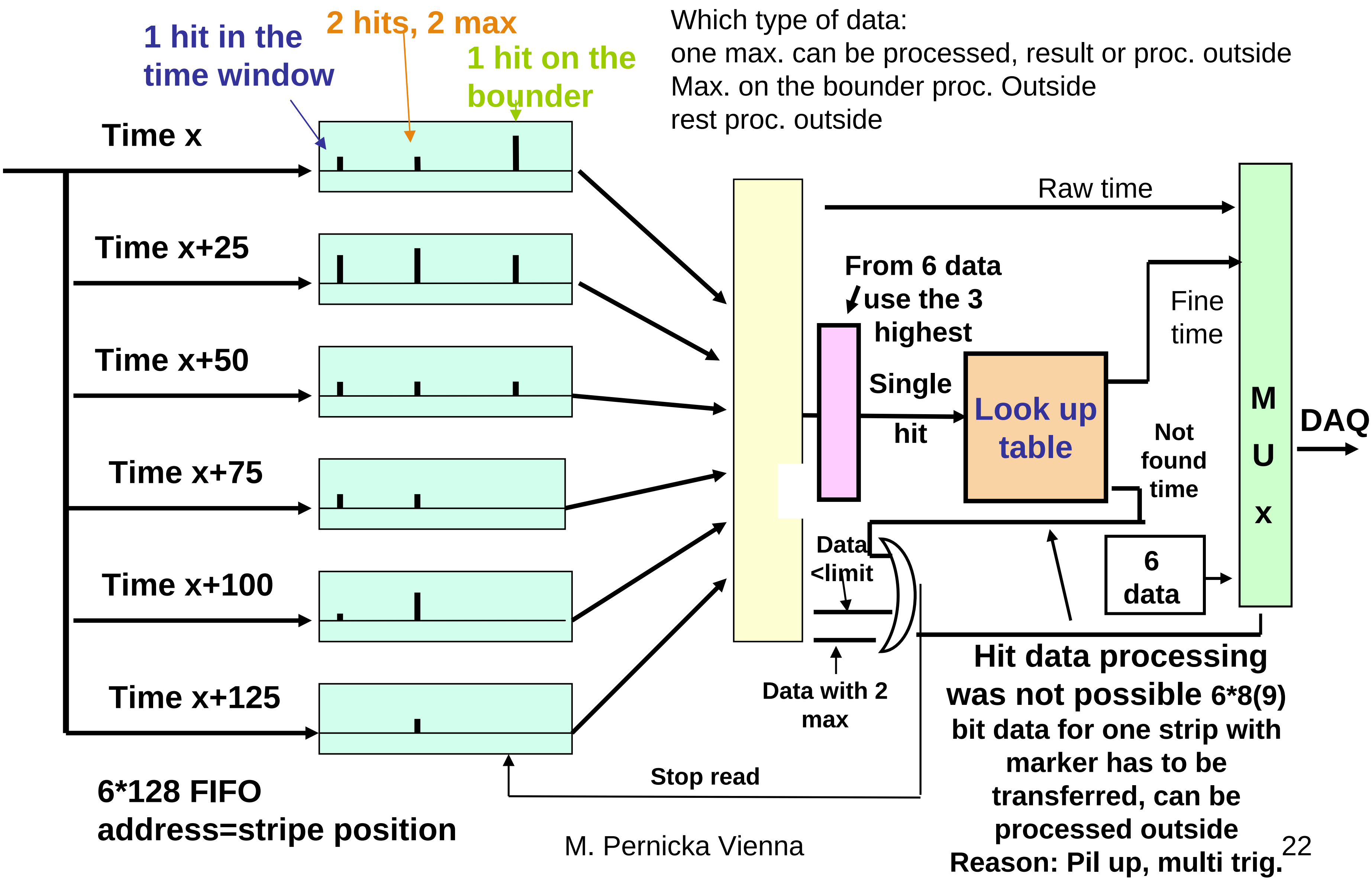
**4 FIFO + 24 Dual Port memories (128*9 bit) to transfer data format for processing time 194 exist**



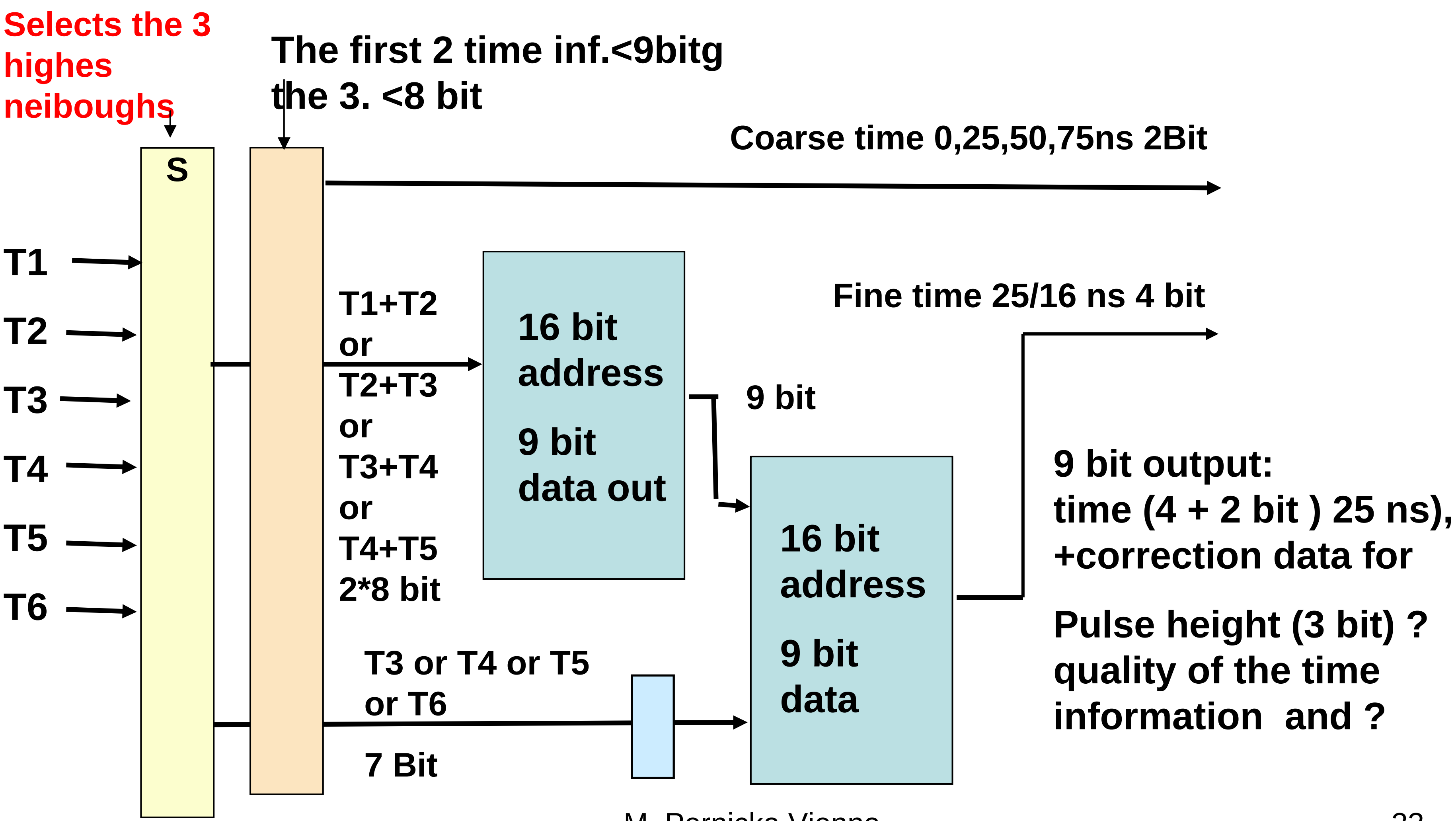

Slow read in Every 6 clocks data from 4 inputs are read in. Data with and with out hit bit

**512 Output data every strip data has up to 6 pulse height information's = One strip with 6 times readout time 4*128*25ns**

# *A possibility to realise hit time processing for 4 inputs = 4 APV25 (one detector)*



# *One of several possibilities to measure the time under evaluation (* ***The pedestal value of the signal should be for the Look Up Tables alwas the same )***



# *Control system for the hit data decision logic.*

**Counter for these cases**

hits which where processed by the look up table
hits which do not fit in the shaping curve
where more than one maximum was found
where max of amplitude on the boarder

The ratio between counters should be more or less constant. Could be done for every APV25

**Data control system:**

1. **Compare channel event number with that from system. Done on board. Channel event number counted from the number of APV25 headers.**

2. **Look for missing APV25 signal inputs**

3. **First and second correction value for the common mode. The sum of pos. and neg. values should be roughly equal.**

4. **It should be possible to build a histogram from the calculated time of the different inputs-APV25. There should be maximum, where our trigger is expected.**

5. **The ratio of found hit time and unprocessed data.**

# Summary

- **A, 2 modules exist and are tested as far as possible, Reorder, Hit calculation, data format, … are tested and work.**
- **B, The firmware is still without time calculation.**
- **C, The APVDAQ 9U VME for the control signals exist**
- **D, A test with the FADC+proc. APVDAQ 9U control module and Copper system was done at Vienna and now at KEK.**