tsim-general

Eunil Won
Korea University

- Goal for SBelle
- Sub-detectors

tsim

- tsim is a trigger simulator developed for Belle experiment
- tsim has been quite useful in studying trigger performance in the beginning of the experiment
- In superBelle case we would like to re-enforce this activity, in particular -

  We need it for at least
  - CDC
  - ECL
  - PID
  - KLM

tick-by-tick tsim

- It is quite useful to estimate the latency of the trigger logic (Belle tsim-CDC already has it)
- In the case of pipelined trigger system, it is quite useful in debugging your VHDL codes (in particular for a large scale coding)

tick-by-tick simulation for
- CDC
- ECL
- PID

Now let's hear what sub-groups' status are!