Level 1 CDC trigger

- mainly 3D tracking

Y. Iwasaki (KEK) and Eunil Won (Korea U)

Reminder

✓ Fast trigger : within 3 - 3.5 usec

✓ Tight but efficient logic : S/N >> 0.1 , efficiency ~ 1.0

✓ Rate @ L = 8 x10^{35} /cm^2/s

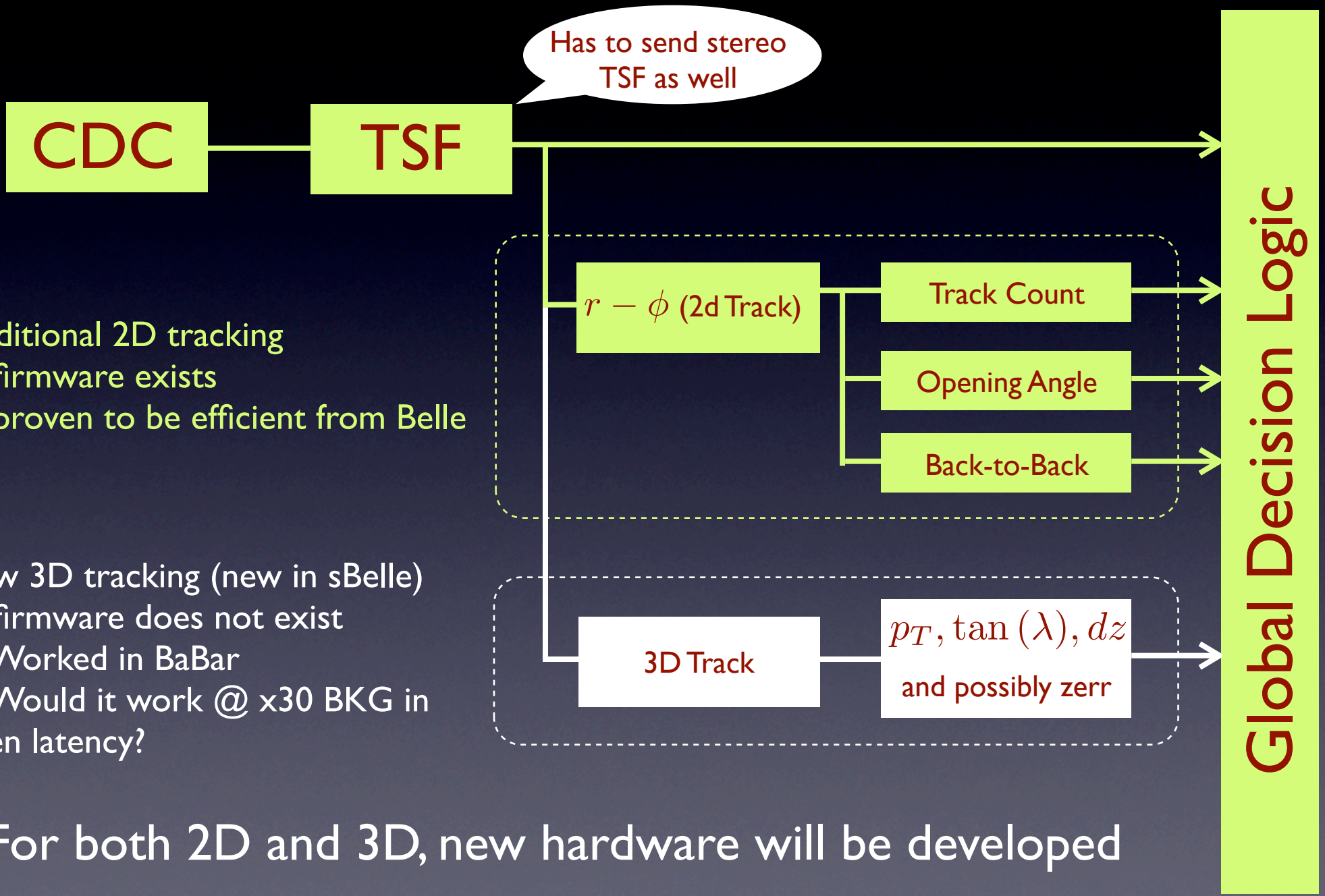
Average L1 rate ~ 10 kHz, Maximum ~ 30 kHz (worst 100 kHz, see July meeting talk by Y. Iwasaki : so more sophisticated algorithm is needed)

✓CDC specific

charged track info : order 2000 bits to GDL

✓We have two strategies : 2D and 3D tracking in L1

L1 Track trigger outline



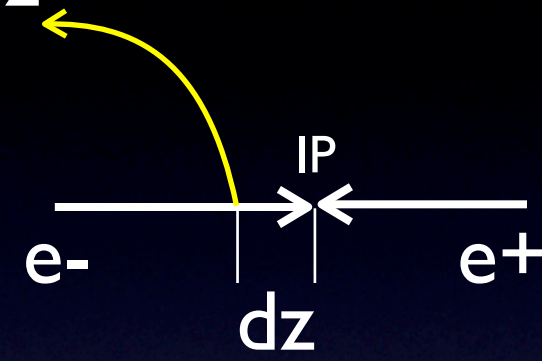
Traditional 2D tracking
- ✓ firmware exists
- ✓ proven to be efficient from Belle

New 3D tracking (new in sBelle)
- ✓ firmware does not exist
- ✓ Worked in BaBar
- ✓ Would it work @ x30 BKG in given latency?

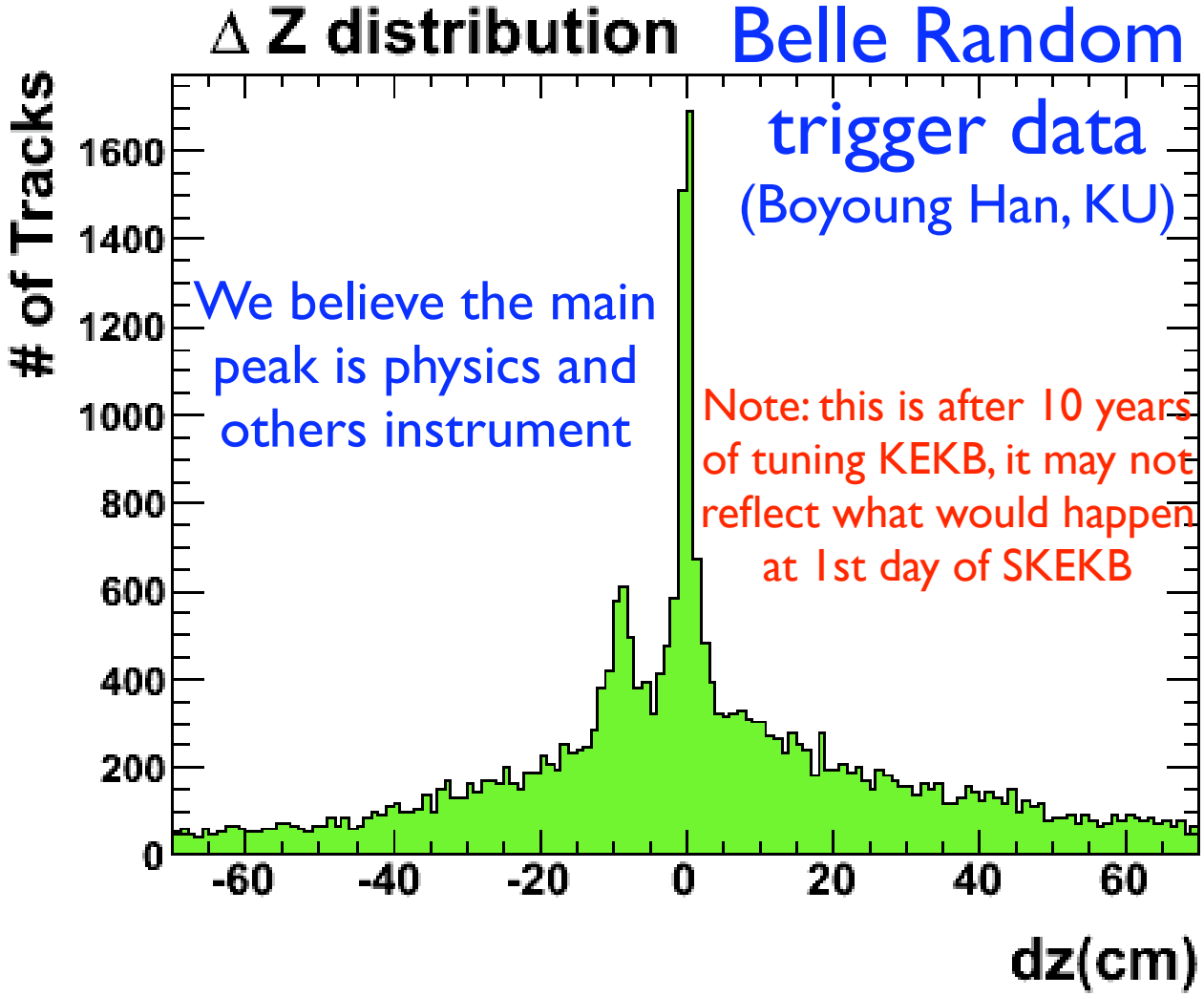
For both 2D and 3D, new hardware will be developed

3D Track Triggering

Idea is not to trigger on events with large dz



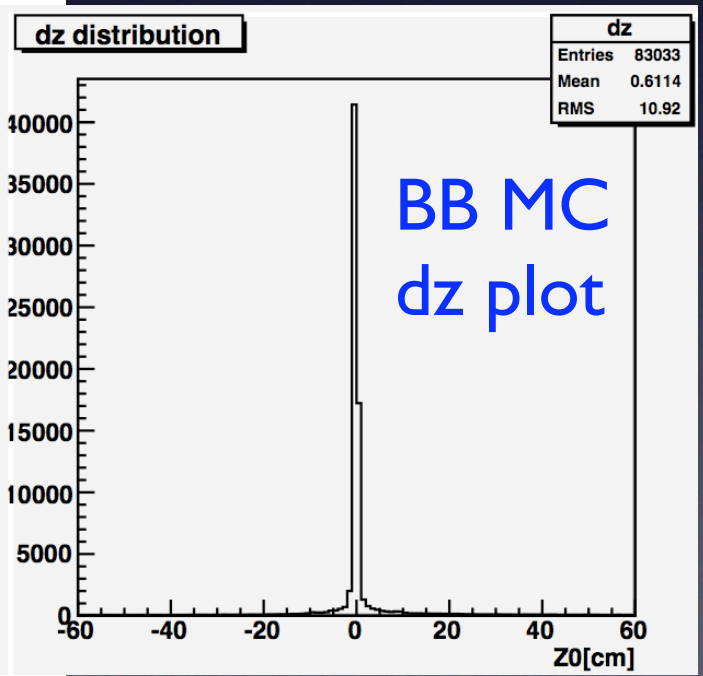
track dz and pT(=1/kappa) distribution:



Belle Random trigger data (Boyoung Han, KU)

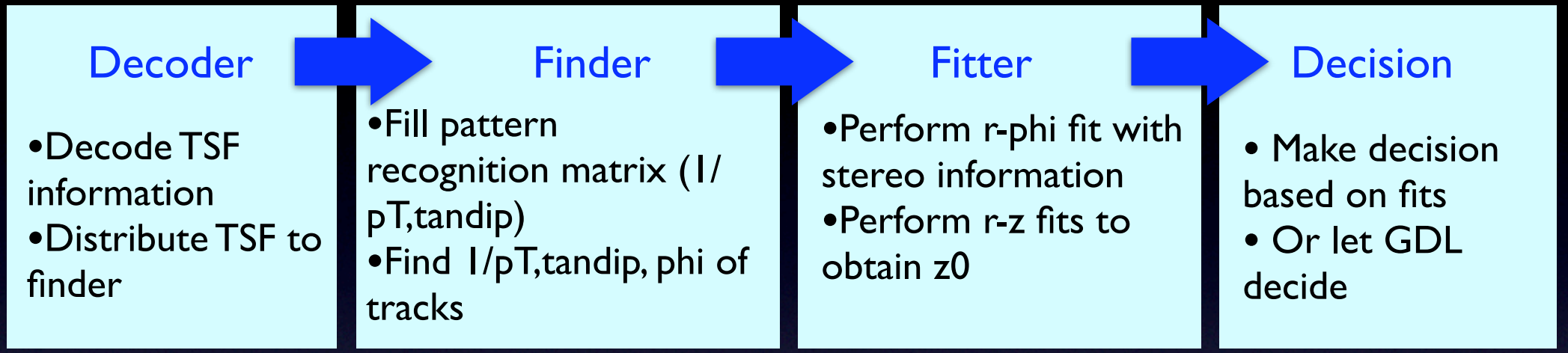
We believe the main peak is physics and others instrument

Note: this is after 10 years of tuning KEKB, it may not reflect what would happen at 1st day of SKEKB



BB MC dz plot

Outline of the 3D Algorithm



Latency distribution (from BaBar exp)

36 ticks | 60 ticks | 96 ticks | 6 ticks

- The sum of latency ~ 200 clock ticks
  - for 500 MHz, 200 * 2 ns = 0.5 us
  - for 100 MHz, 200 * 10 ns = 2 us
- But running FPGA at 500 MHz is usual exercise?
- Would this algorithm fit in single FPGA?
  - one board houses one FPGA covering 1/8 of full CDC volume

Latency Friction

Trigger group

- Sophisticated trigger is desired
- 5 us seems their favorite number (BaBar : 12 us) but 3.5 us is OK?

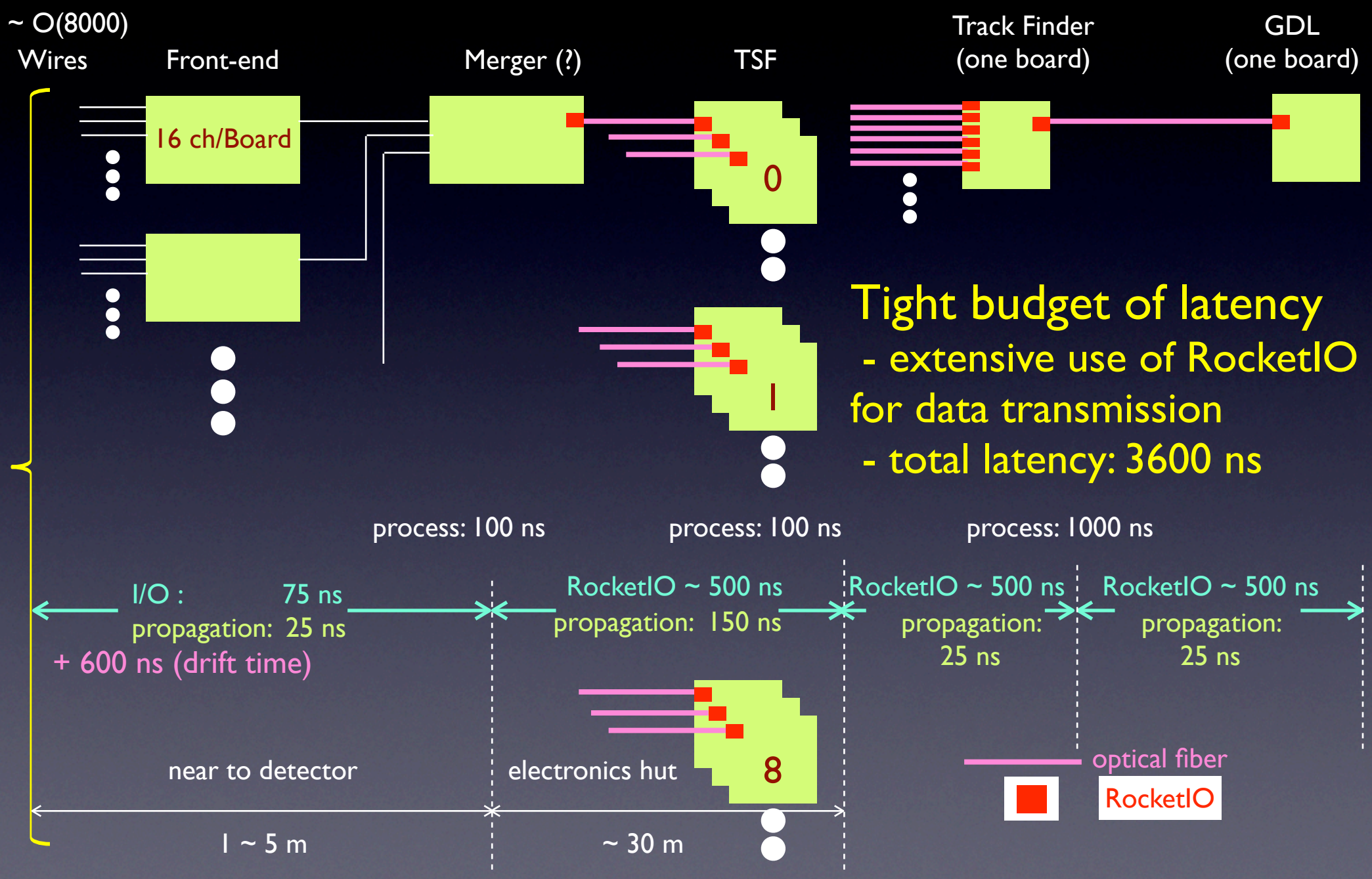
DAQ group

- Minimum dead-time is desired
- ~ 3% seems their limit (Correct me if I am wrong)
- Not only latency, but also time for two consecutive L1 triggers
- At least now they know situation with SVD

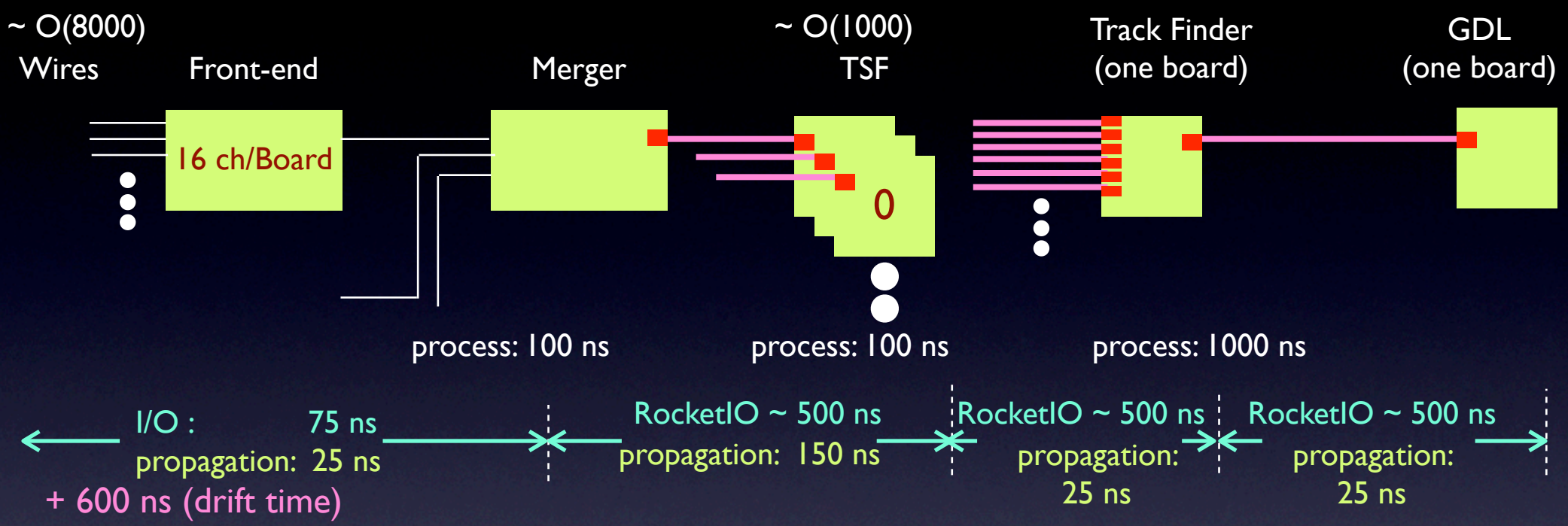
Largely it is 3D triggers that generates this friction (so it is me)

Detailed discussion on the latency : DAQ session

Trigger lines for CDC



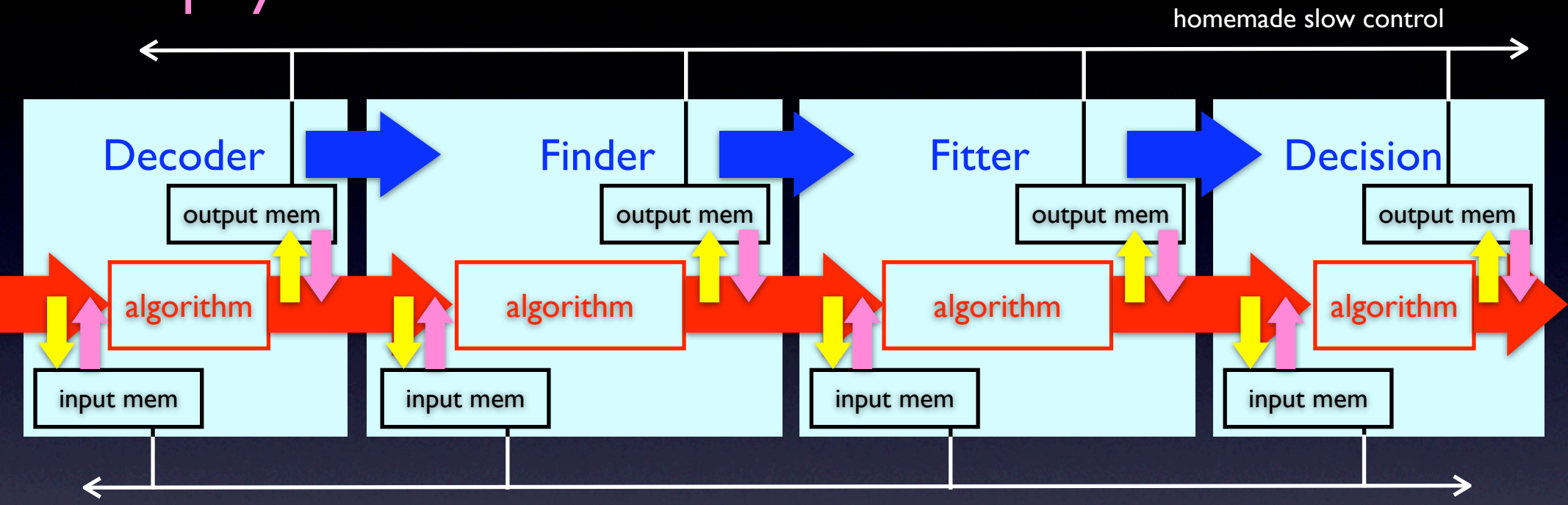
Latency Budget for 3D



- The assumption of 0.5 us from RocketIO realistic? (will be measured)
- The 3.6 us latency scenario: we are left with 1 us in the beginning
- For 3D tracking, 1.0 us maybe "OK": w/ running @ 250 MHz = 200 + 50 (spare) ticks

A firmware design model (from BaBar)

- A "play-record" model



- The upstream "plays" data and input/output of module "record" data into memory
- The recorded data can be readable/writable via homemade slow control
- This has been tremendous help in developing/debugging the firmware in particular in a large scale VHDL coding

I'm thinking of something similar to this - we have VME access

Hardware Development Status

- TSF, TF (2D), 3D fit board, and GDL will have all same form factor (VME 6U) : assuming RocketIO
- In total, O(25) is needed
- Hardware design status is same as in GDL case (see Y. Iwasaki's talk)

Algorithm Development Status

- TSF firmware: exists

- 2D TF
  - ✓present algorithm can be used without modification
  - ✓"Half 3D tracking" : Hough transformation is under development (Y. Iwasaki)

- 3D track trigger
  - ✓ Just started in the framework of tsim-CDC
  - ✓ A lot to be done (pattern recognition, finding and fitting)
-
- GDL
  - ✓ A lot of parts can be reused (See Iwasaki's talk)

Summary/Issues

- Hardware in good progress
- Algorithm in good shape except 3D track triggers
- What do we do if the latency becomes problem?
- Will 3D work @ x30 BKG?

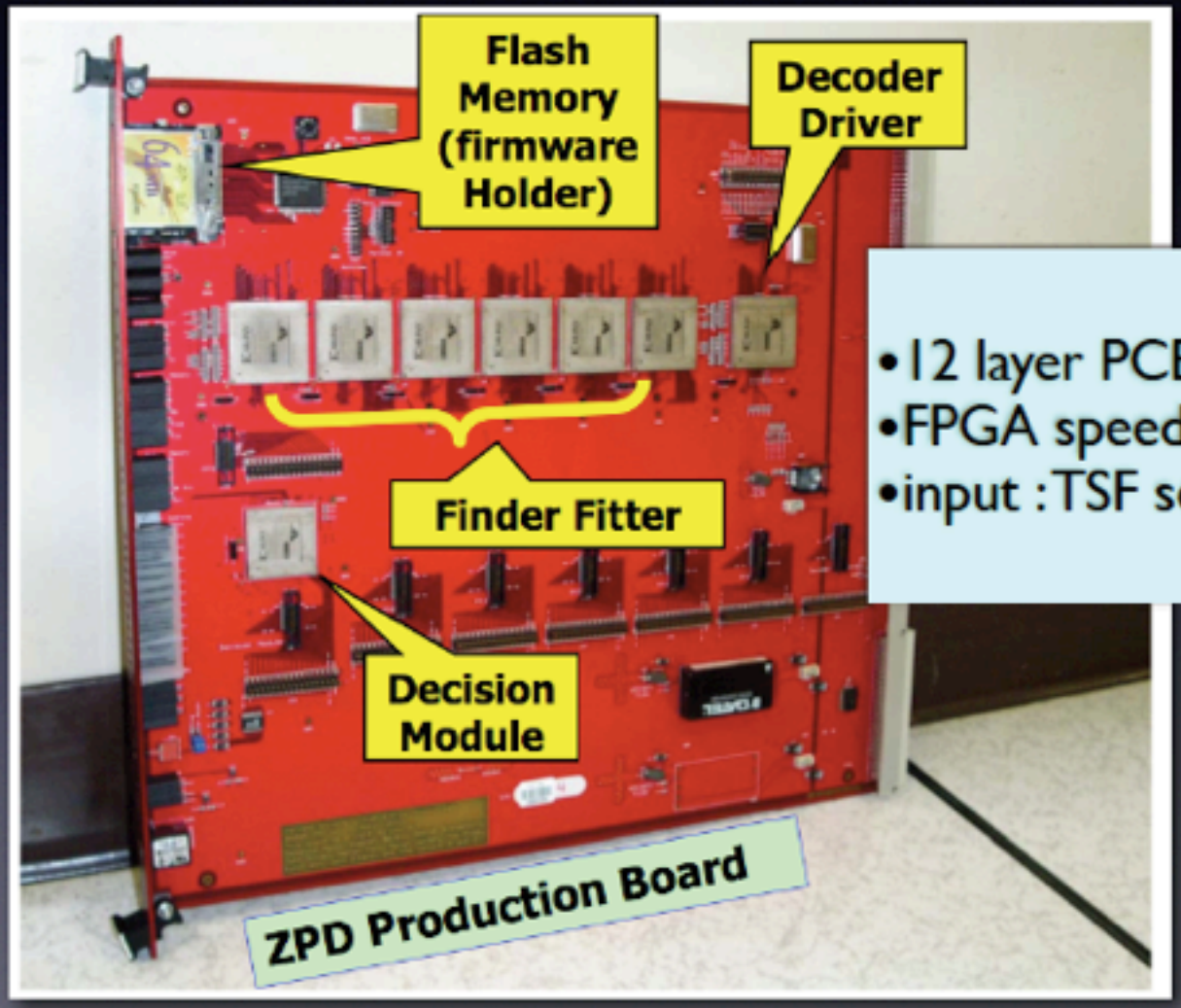
Backup Slides

Hardware Configuration

- VME 9U (EURO card) + J3/P3 for BaBar specific data/ control bus (fully pipelined)

Fastest as of 2001-2

- 8 FPGAs on board (6 Xilinx Vertex2 XC2V4000 + XC2V3000 + XC2V1000)

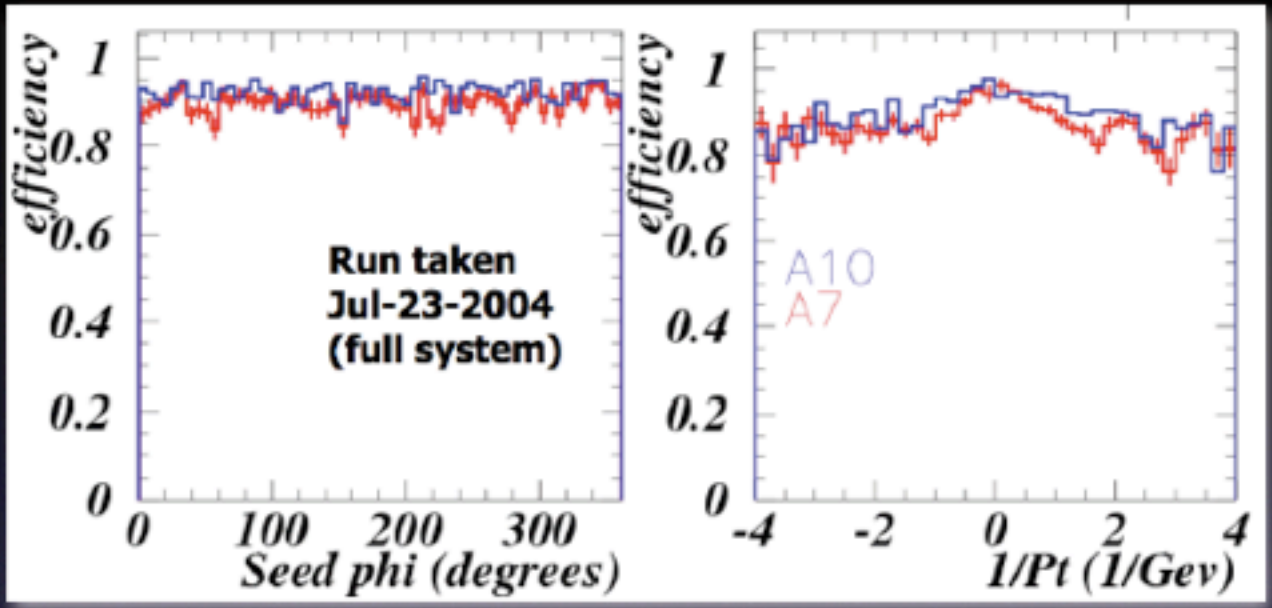


- 120 MHz (main algorithm)/60 MHz (decoding/decision) clocking

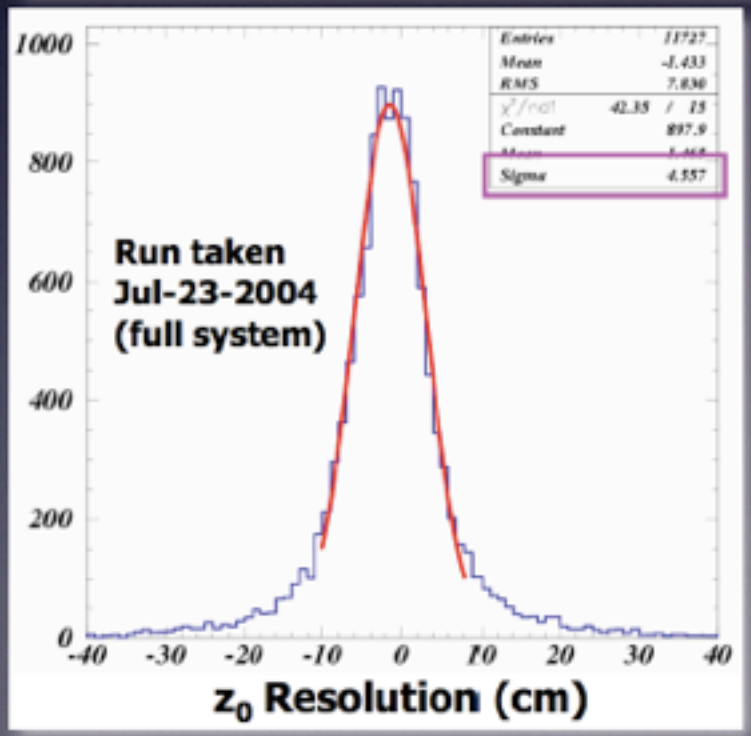
- 12 layer PCB design
- FPGA speed grade: -4
- input : TSF segment from J1,2/P1,2

- Firmware loading via CF card (in total 8 different sets can be stored)
- One board covers 3/8 of 2π : total 8 boards with overlaps

Performance of BaBar 3D Track Trigger



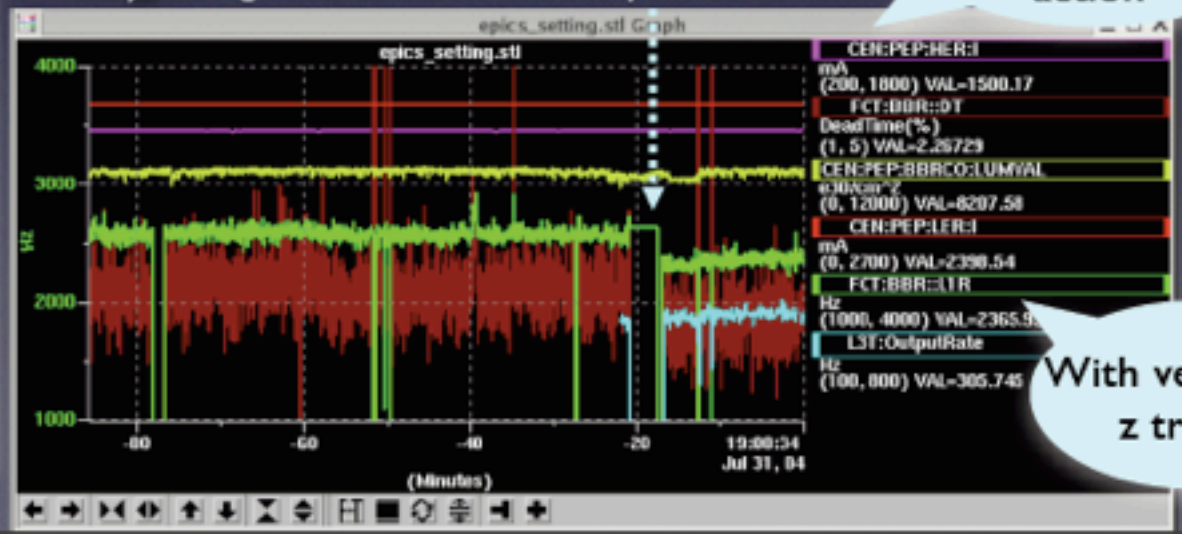
High efficiency (~90%) over full 360° and wide range of pT



The z0 resolution is ~ 4.6 cm and is in good agreement with their simulation

This is precise enough to select signal tracks exclusively

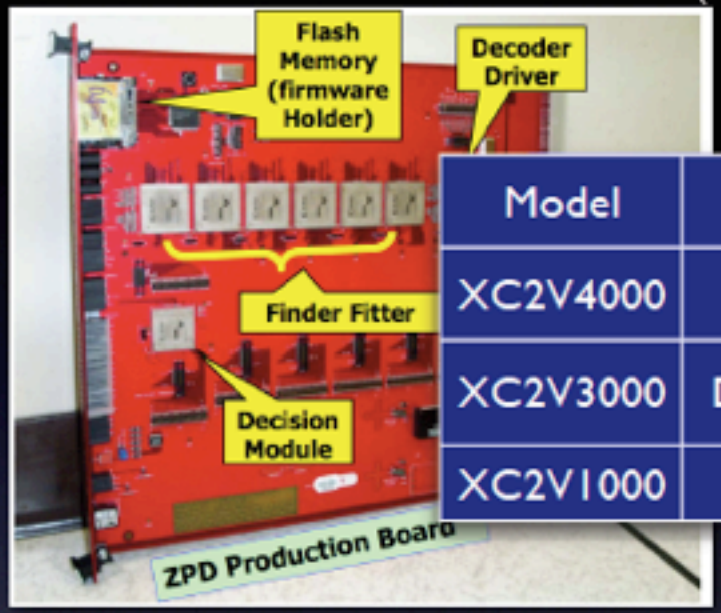
EPICS snapshot at the trigger in action



With very loose z trigger

Can we produce z0 in sBelle?

- BaBar has one board (has 8 FPGAs) for 1/8 of 2π



Model	Function	CLB	Usage
XC2V4000	Finder and Fitter	23,040	44%
XC2V3000	Decoder and Driver	14,336	27%
XC2V1000	Decision Module	5,120	70%

Total 23040*6+14336+5120=160k (17.6k)

Grand total: 160k*8=1.2 M blocks (140k)

(weighted by usage: but place&route nontrivial if usage is high!)

- If we use Vertex5 (the lastest, largest, and fastest from Xilinx as far as I know. Does Altera have better ones?)

Model	CLB
XC5VLX330	51,840

No way we can fit into a single board

One board covering 1/8 may be OK

(Note: TSFs are grouped in layers, not in phi)