Summary of the SVD session

19 March 2009

T. Tsuboyama (KEK)

Agenda of the meeting

15:00 SVD (3h00') (3-go-kan, 1F seminar hall)

- Introduction of new members
- Progress since last meeting (15') (PDF) — Toru Tsuboyama
- APV25 and Origami (15') (Slides) — Markus Friedl
- Prototype batch of DSSD from commercial vendors & Proposal for SVD Layout (15') (Slides) — Thomas Bergeaur
- DSSD R&D in Tata Institute (15') (PDF ; Slides) — Kamesh Rao
- DSSD R&D by Kyungpook Univ. (15') (Slides) — DongHa Kah
- Ideas of Monitoring (15') (Slides) — Samo Stanic
- Ideas of forward silicon tracker (15') (Slides) — Masako Iwasaki
- Task List (15') (PDF) — Toru Tsuboyama

Progress after the last meeting

- HPK DSSD production
  - HPK showed an intention to restart DSSD production but has not give us their decision.
  - → Bergeaur's talk
- APV25 purchase
  - We bought 4000 chips, just enough for SVD production.
  - → Friedl's talk.
- IR discussion started with engineers → Iwasaki's talk
- Super BEAST → If SVD/PXD is not installed at T=0, we need a radiation measurement system.
- Hara moved from Osaka to KEK.
- His main task is computing and software for the Super BELLE.

DSSD prototyping (Bergeaur)

- Prototype of a double sided sensors from 6” wafer are important in order to examine the *Origami concept*.
- Quotations from Micron and SINTEF were compared.
- From view point of technology, both company gave reasonable answer.

Comparison of the two Quotations

	SINTEF	Micron
N-type FZ bulk material	3.5-12 kOhm cm, <100>, not in stock (Topsil)	8kOhm cm, <100>, in stock (Topsil+ etching and polishing @ external company)
Thickness	300 um +/- 25um	300um +/-5 um
Full depletion voltage	max. 90V	40V (according to resistivity)
Poly-Si bias resistor	5-100 MOhm (typically 10 MOhm)	10 (+/- 5) MOhm
Strip Isolation	P-stop	P-stop
Masks	14 pcs. 7x7 inch (Photronics), with working copies	15 pcs. 7x7 inch (Photronics), master only
Number of bad strips	10 (per side)	• 38 per side (first 10 pcs.) • 7 per side (remaining 20 pcs)

Lead time comparison

	SINTEF	Micron
Commencing		6 months
Wafer Procurement	10 weeks	-
Completion	30 weeks=**7.5 months**	**9 months**
Contingency	+/- 1 month	+/- 1 month
Quotation Validity	30 days	End of December 2009

DSSD prototyping (Bergeaur)

- Cost: SINTEF = Micron *2.
- SINTEF is more communicative than Micron.
- Micron has only 1 for each job.
- If HPK does not answer soon, we should start with Micron.

Cost Comparison

	SINTEF	Micron
Masks	5.5 M¥	4.4 M¥
Probe card + Test setup	0.9 M¥	0.3 M¥
Testing, Packaging	1.6 M¥	0.4 M¥
Administration	1.6 M¥	-
Review and adaptation of photo mask	25 k¥ per hour (**not included in sum!**)	-
Processing	13 M¥ (23 pcs)	2.5 M¥ (first 10 pcs.) 5 M¥ (next 20pcs.)
Total Sum	**22.5 M¥ (178 k€)**	**15 M¥ (120 k€)**
Sensors received	**23**	**30**
Cost per sensor	~1 M¥ (8k €)	~0.5 M¥ (4k €)

Comments

- **Pro/Cons**
  - SINTEF is much more expensive than Micron (twice as much!)
  - SINTEF takes everything more seriously
  - Micron has only 1 person for each job
- Maybe we should consider also to contact Canberra for a quotation, to check if Micron's price is low or SINTEF's numbers are too high
- If Hamamatsu is really re-starting DSSD production in the future we should anyhow go with Micron for a prototype batch **now** for R&D (e.g. Origami concept)
- However: The total number of sensors for the new SVD is not so high that HPK will do so only for us.

Answers received

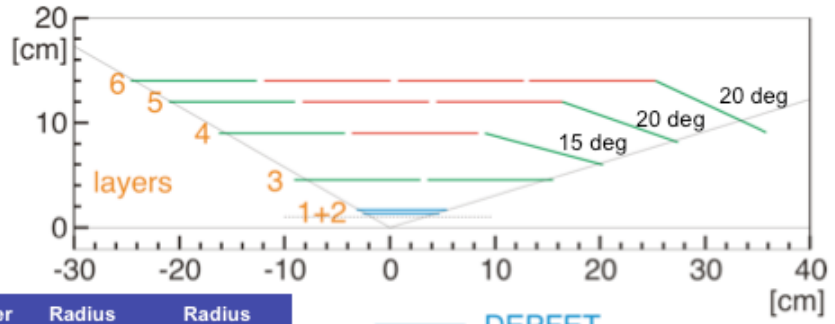
I have received answers from both companies:

- **SINTEF**
  - active communication between me and the senior physicist to clarify several technical aspects
  - Lengthy quotation with all technical details, detailed payment and delivery scheme
- **Micron**
  - No communication with them until I have received an email with the quotation. No discussion about technical details.
  - However, I met their director at TIPP09 conference and discussed with him a bit.

Proposal for DSSD layout (Bergeaur)

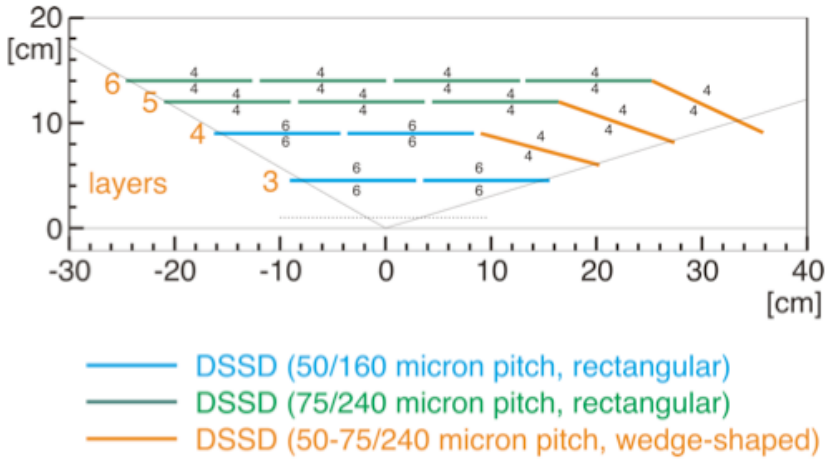
- With sensor from 6” wafers, SVD can be build by using just two type of sensors.
  - horizontal: rectangular
  - slanted: trapezoidal
- In order to save number of APV25 chips, wider readout chip in the outer two layers.

Proposed 6” SVD Layer Arrangement

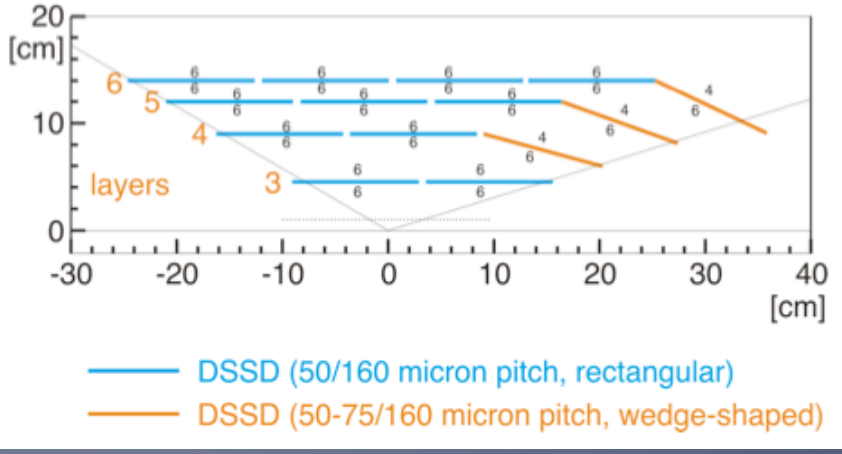


Layer	Radius (barrel)	Radius (slanted)
6	14 cm	10.7 – 14 cm
5	12 cm	8.3 – 12 cm
4	9 cm	6.1 – 9 cm
3	4.5 cm	-

SVD Layout with 3 sensor types



SVD Layout with 2 sensor types only



Cost estimate

- Calculation is done assuming Micron sensor.
- DSSD production cost
  - $=\Sigma$(setup cost + sensor cost)
- Number of APV chips and DAQ system is reduced in "3-layout" design.
- In total, 3-layout design is slightly cheaper.
- Power supply and COPPER/ FINNESSE is not included in the cost.

Summary Costs

	2-layout design	3-layout design
Rectangular (50/160µm pitch)	216	48
Rectangular (75/240µm pitch)	-	168
Wedge-shaped (50-75/160µm pitch)	64	-
Wedge-shaped (50-75/240µm pitch)	-	64
Sum:	**280**	**280**
Total active area:	**1.27 m²**	**1.27 m²**
Total sensor costs (Micron):	**640 k€**	**680 k€**
Number of APVs	**3232**	**2464**
Total SVD costs: (excluding power supplies)	**1933k€ (2.5 oku¥)**	**1666k€ (2.1 oku¥)**

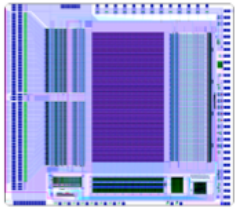
Comments

- Calculation is very preliminary
- It contains
  - Full APV readout chain
  - **NO** power supplies and NO COPPER/Finesse
  - Costs of silicon sensors based on Micron quotation (**WITHOUT** any spares and prototypes)
- If we want to go to with SINTEF, sensor price will be almost doubled
- HPK will probably not re-start DSSD production for such a small number of sensors

APV25 and Origami (Friel)

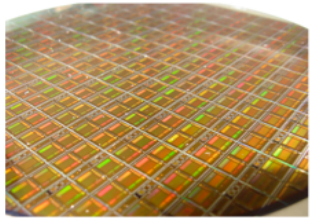
- 4,000 chips were purchased.
- 1,500 chips will be thinned.
- First wafer was thinned and diced in a French company.
- Result is excellent.

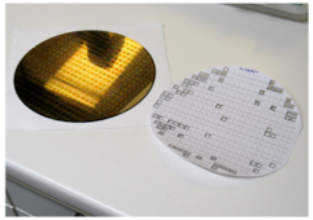
APV25 Purchase



- Current Belle purchase
  - **1500** diced **„normal“ APV chips** (~300µm thick)
  - **2500 uncut APVs** on wafers (for thinning)
- Future order
  - **1000** more **„normal“ APVs** which did not fit in current purchase due to financial limits
- **8 wafers** with a total of **2674 known good dies** were delivered to **Vienna** on 9 Jan 2009
- One wafer contains 360 APVs in total
- Each chip was tested on the wafer, yielding an average of 93% good dies
- The **1500 normal APVs** are at **KEK**, financial transaction underway

APV25 Wafer Inspection





APV25 wafers (8")

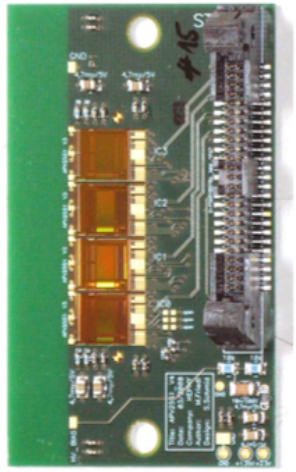
Wafer map showing test results (used to ink mark bad dies on wafer)

More photos: http://www.hephy.at/gallery2/v/electronics2/8inchwafer

- On 19 Jan 2009, we sent 1 wafer (319 good dies) for
  - Thinning (100µm target), dicing and waffle packing
- Received back on 4 Feb 2009
  - **105µm (nominal) thickness**
  - 314 (out of 319) good dies (= **98.4% yield**)

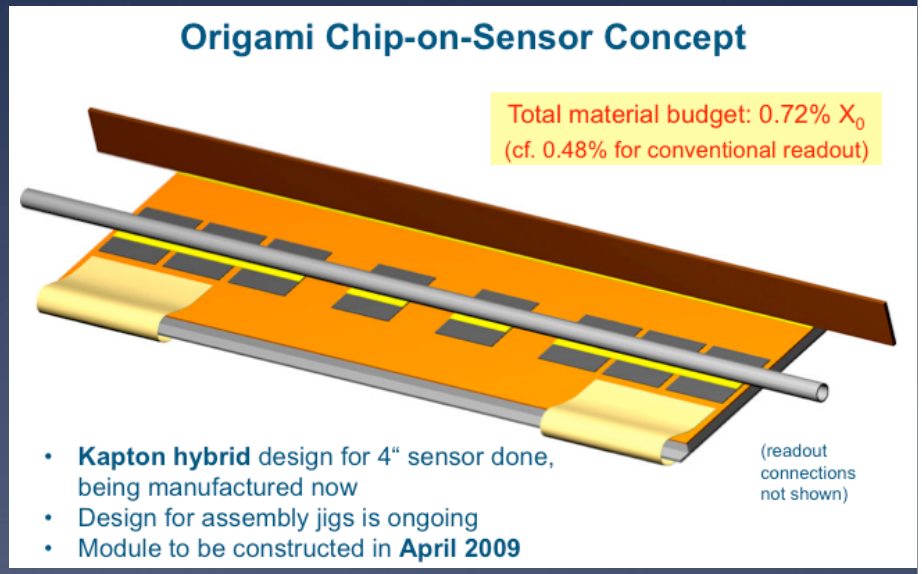
Investigation of Thinned APV25 Chips

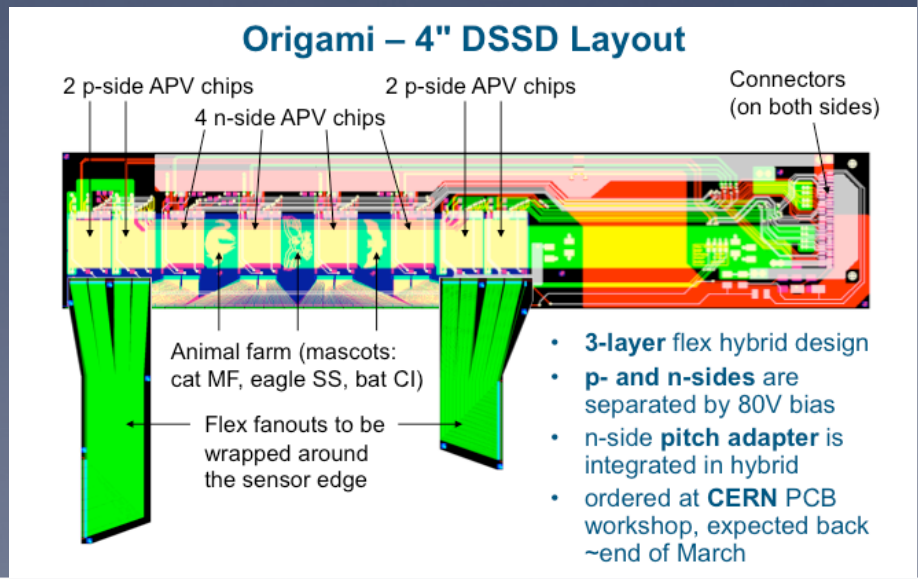
- **Thickness measurement: 106.6** +/- 3.2 µm
- Thin dies are still quite rigid, easy handling
  → thinning mechanically OK
- Mounting 16 thinned chips on hybrids
  + 4 normal chips for electrical measurements
- **All perform equally well**
  → thinning electrically OK
- Next step: **populate 2 Origami modules**, one with normal, one with thinned APVs
- If again no difference, we will proceed with thinning all the chip-on-sensor wafers



Origami concept (Friedl)

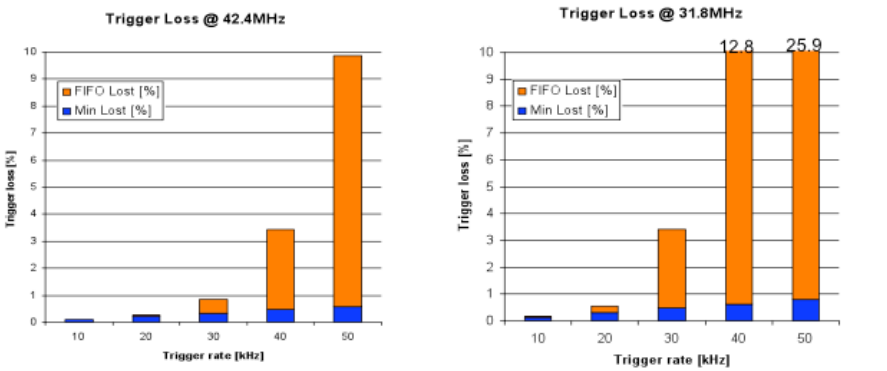
- Origami scheme is necessary to read out large area detector with APV25.
- At cost of 0.3% X_0, high S/N is assured.
- The strips in back is readout with APV25 on top of the sensor.
- First PCB is in production by CERN. Test of origami scheme will be done soon.





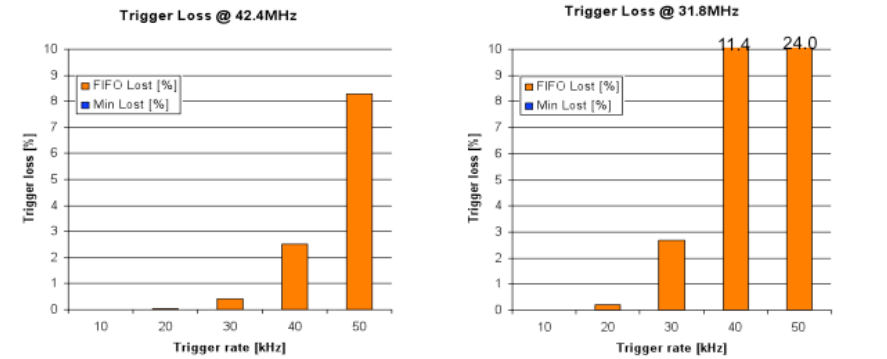
Trigger issue

- GLD decision requires ~5 μsec.
- At 42 MHz, the 192 stage pipeline of APV25 can hold data for 4.6 μsec.
- At 32 MHz operation, pipeline can hold data for ~6 μsec.
  - Dead time > 3% at 30 kHz trigger rate.
- With >500 nsec between adjacent triggers, the problem is relaxed.



- **Min Lost**: too little distance between triggers (6 clocks min.)
- **FIFO Lost**: too many pending readouts (filling APV25 buffers)
- **Nakao-san** wishes <3% dead time @ L1=30kHz
- → **OK (0.87%) for 42.4MHz** clock, **slightly higher (3.43%) at 31.8MHz**

External 500ns Dead Time Requirement (ECL)

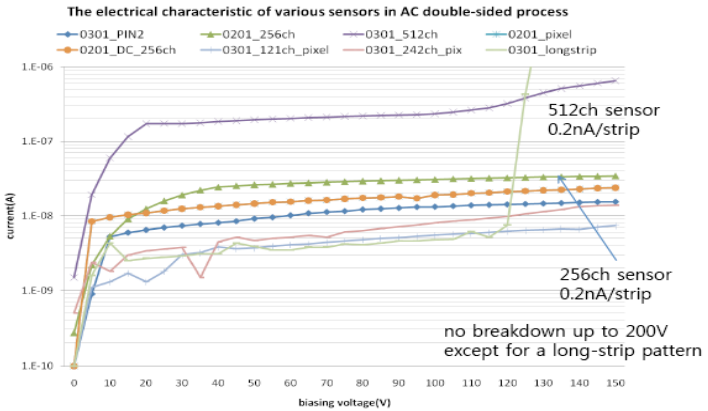


- **Nakao-san's** wish (<3% dead time @ L1=30kHz) met in both cases
- → **0.42% for 42.4MHz** clock and **2.7% at 31.8MHz**
- 500ns dead time (as required by ECL) not accounted for APV25
  - Hence minimum lost figure is always zero

Detector R&D

* R&D in Korea and India are now in good shape.

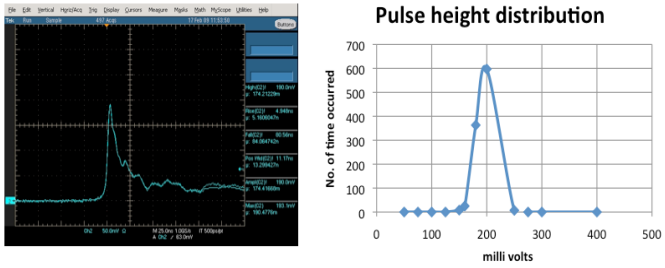
- The leakage current distribution of the AC DSSD and various sensors



2nd Open Meeting of the SuperKEKB 10

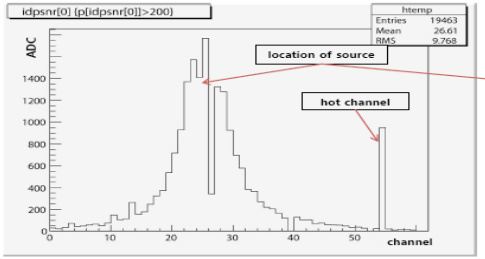
Third Batch : <111> , Resistivity 9k – 12kohm, Single sided

Response of silicon detector with 1064nm pulsed laser
Tested with single sided detector

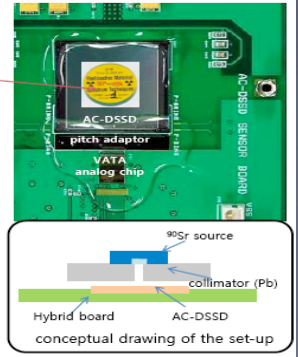


Sr-90 beta source test of the AC-DSSD

- ADC pulse height distribution of the P-side



ADC v.s. channels

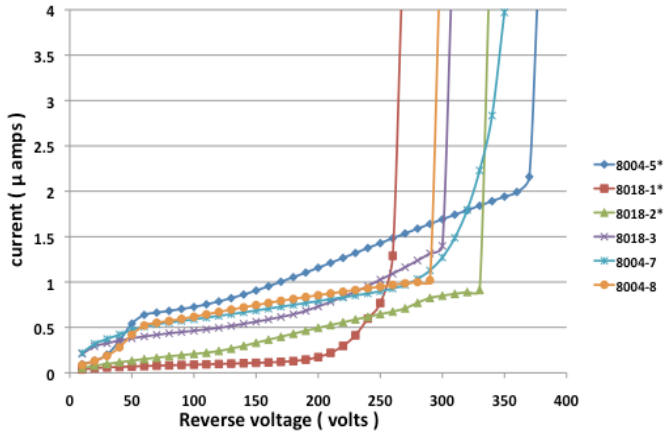


conceptual drawing of the set-up

Fourth Batch : <111> , Resistivity 2k –4kohm Single sided

Fourth Batch

I –V characteristics of SSD with resistivity of 2-4kohm (03–03–09)

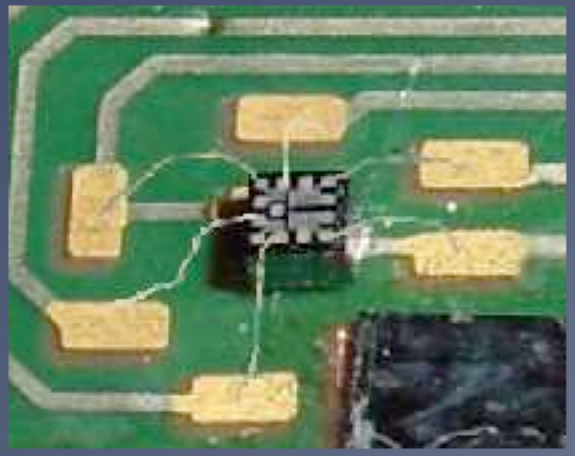


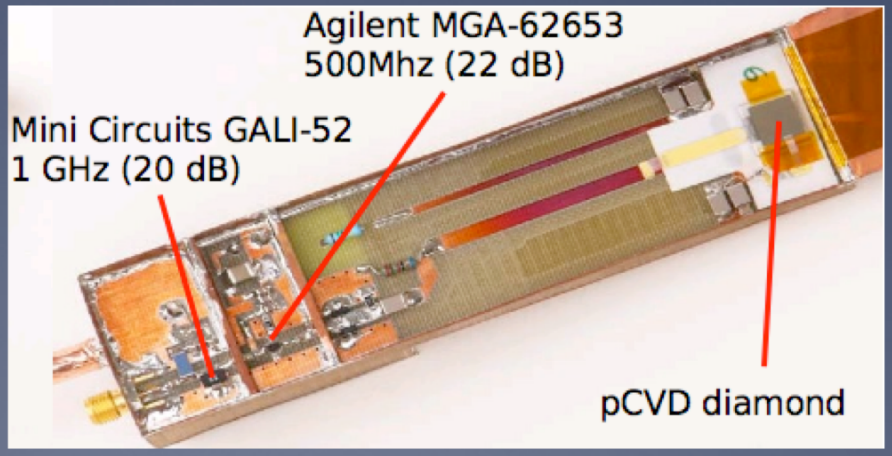
Kyungpook Univ.: DongHa Kah

Tata institute: K. Kameswara Rao

Monitor (Stanic)

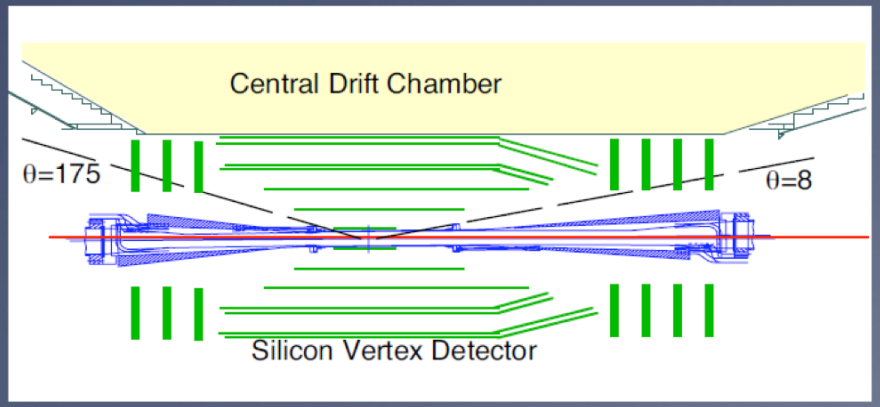
- RADFETs are useful in the present SVD
  - Are RADFET chips still available?
  - Total dose can be estimated using sensor damage.
- Diamond sensor for radiation measurement and : In SVD3, we discussed to install several chips to silicon ladder.
- Temperature sensors are also
- Position monitor?

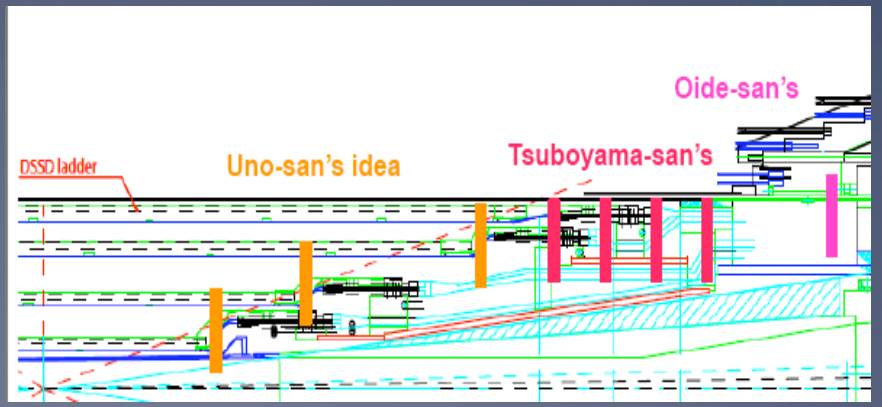




Foraward detector (Iwasaki)

- Purpose
  1. Extend the Belle acceptance to improve physics potential.
  2. Measure the e+ or e- which is generated in the e+e- interaction and scattered by beam. Then the beam size measurement becomes possible.
- For 2, random triggered data should be used.
- If enough space is not available, we must consider to extend the angular acceptance of SVD





TASK LIST

Software

- Online:
  - Cluster finding and time reconstruction
  - Calibration
  - Performance monitor
    - Data quality monitor
    - Quality assurance monitor
- Offline
  - Calibration / Database
  - Alignment
    - For physics study, much better svd/pixel alignment and reliable tracking (CDC+SVD+PIXEL) is necessary
  - Tracking
    - CDC track extrapolation
    - Local SVD/Pixel tracking
  - Simulations
    - Detector optimization

DSSD production

- No news from HPK
- Test production by other companies (Talk by Bergauer)
- R&D in Tata institute (Talk by K. Rao)
- R&D in Kyunphook Univ. (Talk by Kah)
- Mass production
  - Sensor characterization.
  - Quality control

Readout

- APV25 hybrid
  - Normal and Origami
  - Production
  - Quality control --- Test
- Repeater
  - Mechanical and Electric design
  - Mass production
- Backend
  - COPPER/FINNESSE – How many crates are necessary?
  - Mass production
- DAQ software
  - Slow control

Mechanics

- Support
  - Joint work with IR/DEPFET/Strip design is necessary
  - Connection to CDC/IR/DEPFET
  - Design: Cooling of normal hybrids
  - Construction
- Ladder production
  - Design
  - DSSD test
  - Hybrid test
  - Assembly
  - Storage
  - Booking
  - Ladder test

Infrastructures

- Monitor
  - Radiation and Beam abort
  - Temperature
- Cooling
  - Chiller/coolant
  - tubing
  - Special consideration of Origami cooling tubes
- Cables
  - Power supply / signal / control /
- Power supply
  - Design, construction (purchase)
  - Place
  - 3 times larger system than the present SVD
  - DEPFET group need a big power supply system, also.
- Readout
  - Crates

System integration

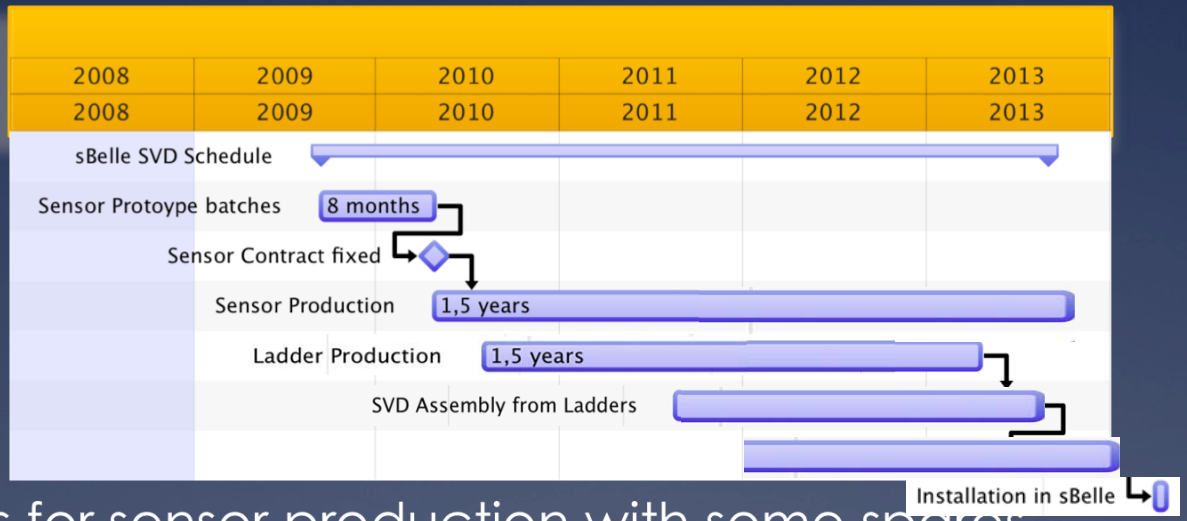
- Definition of Integration strategy.
- Ladder mount
- Test with source /laser (?)
- Debugging hardware and software
- Calibration
- Cosmic ray test
- Commissioning Pixel + SVD should be done together.

Forward detector

- Talk by Iwasaki
- Purpose
  - Improve physics performance
  - Beam size measurement
- Design should be done in parallel to the SVD design.
- How about just extend the acceptance of the SVD.

Production schedule

- Thomas's chart (modified) in a previous meeting.



- 3 years for sensor production with some spares.
- Final ladder production will be done in 2013.
- 0.5-1 year system test before installation.
- SVD and DEPFET installation should be done after we understand background conditions, e.g., 0.5 years.
  - Super BEAST team is necessary

Production speed

- 100-150 DSSD per year * 3 years.
- 24 ladders per year * 3 years.
- 72 ladders installation in the last year.
- DSSD production hopefully starts at end of 2009.